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Technical Tip Sheet For
2026 IEEE International Electron Devices Meeting (IEEE IEDM)

Sponsored by the IEEE Electron Devices Society, the 2026 IEEE International Electron Devices Meeting (IEDM) is the world's premier forum for presenting breakthroughs in semiconductor devices, process technologies, device physics, and emerging computing architectures. The theme of the 72nd annual IEEE IEDM is *"Devices at the Heart of the Intelligence Revolution."* The conference will be held December 12-16, 2026 at the Hilton San Francisco Union Square hotel, with online access to recorded content available after the conference. This Tip Sheet highlights some of the most newsworthy sessions and papers.[1]

A) Focus Sessions

This year's technical program includes two Focus Sessions dedicated to critical emerging technologies:

System-Level Optimization Combining Logic, Memory, and Packaging (Session #39) – As physical scaling slows, unlocking next-generation AI and high-performance computing (HPC) performance demands a radical, cross-domain co-design from silicon to rack-scale architecture. In this Focus Session, industry and academic experts from IBM, Intel, Nvidia, Marvell, SK hynix, and UCLA will present holistic system-level optimizations designed to break memory and thermal limits. These invited presentations will span system-level architectural innovations, integration of optical interconnects for scalable computing, and the critical thermal-mechanical strategies to manage extreme power densities and structural stress in advanced heterogeneous packages.

- *Architecting IBM Power's System Architecture: Composable Compute & Memory from Chiplets to Multi-Rack Pods*, William Starke, IBM
- *Memory Optimizations for Datacenter Agentic AI,* Rajat Agrawal, Intel
- *System-Level Co-Optimization of Compute, Memory, and Advanced Packaging for AI GPUs,* Mahmut Sinangil, Nvidia
- *Photonic Interconnect for Scalable Memory in Accelerated Computing,* Dan Oh, Marvell
- *Addressing Thermal and Mechanical Challenges in Advanced Packaging for High Bandwidth Memory,* Jaesik Lee, SK hynix America
- *Advanced Thermal Management for Next-Generation Logic, Memory, and Packaging Integration: Multi-Scale Modeling, Materials, and Cooling Technologies,* Tiwei Wei, University of California Los Angeles

Semiconductors for Quantum Computing (Session #17) – This Focus Session addresses the manufacturing path to large-scale quantum processors, with invited presentations from the Fraunhofer Institute for Photonic

[1] Definitions and explanations of acronyms and technical terms begin on page 7.

Microsystems, ST Microelectronics, SemiQon, Sandia National Labs, Korea Institute of Science & Technology, and HRL Laboratories. The session will include discussions on 300mm CMOS qubit fabrication and yield, cryogenic CMOS control, and superconducting packaging. Quantum computing scaling is now limited by materials, interconnects, and footprint mismatch rather than qubit physics, making industrial integration the decisive bottleneck.

- *Scalable Quantum Computing in CMOS: Materials and Integration Perspectives,* Benjamin Lilienthal-Uhlig, Fraunhofer Institute for Photonic Microsystems
- *FD-SOI Based Qubit/Logic 300mm Platform for Quantum Processor Unit Chip Compatible with Volume Manufacturing,* Franck Arnaud, ST Microelectronics
- *Cryo-optimized CMOS for Ultra-low Temperature Applications,* Janne Lehtinen, SemiQon
- *Type II InAs/GaSb Heterostructures a Promising Material Platform for Quantum Computing,* Wei Pan, Sandia National Labs
- *Programmable Electro-Optic Quantum Photonic Circuits for Hybrid Quantum Simulation*, Hyounghan Kwon, Center for Quantum Technology, Korea Institute of Science & Technology
- *Qubit-Device Yield & Validation for a Silicon Exchange-Only Quantum Processing Unit,* Clayton Jackson, HRL Laboratories

B) Advanced Logic Technologies

Late News! TSMC's A14 CMOS NanoFlex™ Pro Platform Technology: TSMC will introduce an industry-leading A14 CMOS platform technology featuring the NanoFlex™ Pro architecture, which is on track for volume production in 2028. The technology is further complemented by scaled TSVs, high-performance BEOL metal-insulator-metal (MIM) capacitors, and an innovative Cu-RDL process that enables a 4.5μm SoIC bonding pitch. Supported by robust yield and reliability that accelerates its time-to-market, the A14 platform technology is uniquely positioned to drive next-generation technological innovations across future mobile SoC and HPC/AI applications. (***Paper #3.2 "A14 CMOS NanoFlex™ Pro Platform Technology with 2nd Gen. Nano-sheet and Full Node PPA Benefits for HPC/AI and Mobile SoC Applications,"*** **Shien-Yang Wu, *et al.,* TSMC**)

Intel's Ge-channel PMOS for CFET Hybrid Channel Integration: Intel researchers will present for the first time significant results for germanium channel integration that provides manufacturable solutions to a known Ge-channel integration barrier – the tradeoff between aggressive equivalent oxide thickness (EOT) scaling and gate-stack reliability. Leveraging an ultra-thin germanium oxynitride (GeON)-based gate stack, the work achieves an industry-leading combination of record EOT scaling (4.8 - 8.7Å), high hole mobility (~230cm²/V·s in nanoribbon (NR) architecture), and reliability exceeding Si benchmarks (40% of the iso-field negative bias temperature instability (NBTI) degradation of Si NR devices). Intel will demonstrate optimized Ge PMOS gate stack solutions in Ge p-MOSCAP devices and apply them to Ge nanoribbon transistors, achieving high-mobility and reliability superior to Si. These results establish a credible path for integrating high-mobility Ge channels into future hybrid-channel CFET architectures, removing a key technology barrier to continued CMOS scaling and next-generation power-performance optimization. (***Paper #33.1, "Germanium Nanoribbon PMOS with Reliable and Scaled Gate Stack for Low-Voltage CMOS Technology,"*** **W. Mortelmans et al, Intel**)

High Numerical Aperture Single Patterning Electrical Validation in 18nm Pitch: Researchers from imec will present a high-numerical aperture (NA) EUV single patterning technology that simplifies integration process and eliminates pitch walk. As CMOS interconnect pitches approach sub-20nm, conventional lithography requires multi-patterning, which entails substantial process complexity, longer cycle times, and higher costs. In this paper, an 18nm pitch ruthenium (Ru) direct metal etch (DME) integration is demonstrated electrically using high-NA-enabled single-exposure patterning technique, which simplifies process integration and reduces manufacturing complexity. Electrical test structures show defect-free yields at 18nm pitch over 1.2mm line lengths. The design-technology co-optimization (DTCO) approach supports continuous standard cell scaling with curvilinear layout to improve BEOL routing and pattern fidelity, while aggressively scaling line width, minimum-island, and tip-to-tip

spacing. This DTCO study demonstrates that these advanced imaging capabilities (curvilinear geometries and reduced feature areas) enhance routing efficiency to provide opportunities for optimization of interconnect stacks and continued scaling beyond sub-20nm pitch designs.
(*Paper #22.1, "DTCO-enabled Scaling via High-NA Single Patterning with Electrical Validation in 18nm pitch Ru DME,"* S. Dastidar et al, imec)

C) Memory Technology

A More Energy-Efficient FeNAND for AI: SK hynix researchers will demonstrate the first chip-level 176-layer ferroelectric NAND (FeNAND), using a poly-silicon channel-based structure compatible with established NAND manufacturing instead of relying on complex oxide semiconductor approaches. As demand for AI-compatible NAND devices increases, the requirements for higher bandwidth and lower power consumption become more stringent. Using ferroelectric switching enables significantly lower operating voltage and a reduction in the gate spacing of the X-DEC Pass transistors. By optimizing the memory-cell materials, the device supports practical block erase and reliable operation at substantially lower voltages. Reducing the read pass voltage from 6V to 3V is projected to lower read energy per bit by approximately 32%, making this technology a promising option for future high-bandwidth, power-efficient AI storage systems.
(*Paper #2.1, "Chip-Level Demonstration of 176-Layer 4D Ferroelectric NAND Towards High-Bandwidth and Ultra-Low-Power Operations,"* T. Park et al, SK hynix)

A TSV-Free 48-Die Orthogonal Memory Stack for AI Accelerators: Researchers from the University of Tokyo will present IntMOSAIC, an organic interposer-based 3D memory-on-GPU integration technology that enables massive orthogonal stacking of memory dies without through silicon vias (TSVs), hybrid bonding, or sidewall metallization. As LLM inference applications rapidly increases memory capacity/bandwidth requirements, power consumption and cost constraints have imposed limits on further scaling. In addition, the higher bandwidth requirements result in thermal management bottlenecks. Using standard memory dies mounted on organic interposers, U of Tokyo demonstrates the world's first 48-die orthogonal stack at 130μm bump pitch, achieving full connectivity across all test paths. This architecture supports an 84GB memory stack with 3.1TB/s bandwidth through 1536 parallel I/Os, while reducing access energy to 1.10pJ/bit and maintaining a peak temperature of 85°C in a GPU-integrated system. The technology offers a lower-cost path to high-capacity, high-bandwidth memory for AI workloads. **(*Paper #11.4, "48-Die TSV-Free Organic Interposer-Based Orthogonal Stacking Technology for 3D Memory-on-GPU Integration,"* Y. Mitarai, et al, U. of Tokyo)**

D) Emerging Devices for Compute Technologies & Neuromorphic Computing

Dual-sided CMOS Turns the Wafer Backside Into an Active Circuit Tier: University of Peking researchers will present the first experimental compact dual-sided monolithic 3D CMOS platform combining frontside (FS) advanced Si FinFETs with backside (BS) 2D FETs. Prior monolithic 3D technologies largely used frontside BEOL transistor/memory tiers, while backside integration was mainly driven by power delivery and passive devices. In this paper, authors will demonstrate devices with ultra-scaled contact pitch down to 65nm; inverter voltage gain of ~23V/V at V_{DD} = 1V; functional V_{DD} down to 0.2 V; with rail-to-rail 100ns input transition time. In addition, both NAND and NOR logic gates are demonstrated. A novel low-thermal-budget selenium (Se)-assisted MoS_2 transfer technique is shown, as well as a dual-sided 3D level shifter for voltage-domain matching across tiers. This work empowers future dual-sided integration, redefining the trajectory of the monolithic 3D integration.
(*Paper #6.6, "First Experimental Demonstration of Dual-sided CMOS with Frontside FinFETs and Backside 2D FETs by Backside Monolithic Integration,"* Y. Chu et al, Peking U.)

A Record-High-Voltage IGZO GAA Transistor: Researchers from imec will report the first vertical-channel gate-all-around (GAA) transistor built with an indium gallium zinc oxide (IGZO) channel instead of poly-Si for 3D-NAND Flash periphery circuits. As Flash continues to aggressively scale toward 1000+, there is a corresponding increase in word line high breakdown voltage (BV) transistors. Replacing conventional poly-Si with IGZO alone improves the OFF-state BV by ~4x, reaching a record-high BV >27V with only three word-lines at an 80nm gate pitch. Scaling the gate pitch to 45nm and engineering the drain contact boosts the ON-state current to ~100μA/μm while retaining a BV of ~18V. The research points to a path to new architectures for next-generation high-density, high-bandwidth 3D NAND periphery scaling through CMOS-bonded-to-array (CBA) for tighter coupling with control logic; and array stacking/staircase scaling for better latency and efficiency. Future work is planned for comprehensive reliability studies and evaluation of system-level performance.
(*Paper #38.2, "Ultra-small Footprint Vertically Stacked IGZO-based GAA High-Voltage Device for Future 3D-NAND Flash and High Bandwidth Storage Periphery,"* S. Mukherjee et al, imec)

A Flexible Analog Compute-in-Memory Array for Wearable AI: Fudan University researchers will demonstrate the first highly robust flexible 32×32 analog compute-in-memory (CiM) array based on lanthanum-doped indium zinc oxide (Ln-IZO) DRAM cells, designed to maintain accurate computation even when mechanically bent. With the rapid expansion of edge artificial intelligence (AI) and sensors, flexible processors for efficient neural network acceleration have become increasingly imperative. Compute-in-memory has emerged as a paradigm for next-generation flexible AI processing cores, enabling massively parallel matrix computations within memory arrays, but these DRAM cells face challenges when implemented with thin film transistors. A ratio-coded 4T1C structure suppresses errors from both device variation and bending, enabling stable vector-matrix multiplication (VMM) down to a 5mm bending radius across 20 - 60°C. The flexible CiM array achieves 92.1% electromyography (EMG) recognition accuracy under bending, demonstrating a practical path toward reliable wearable edge-AI hardware.
(*Paper #5.6, "Flexible Ln-IZO DRAM-Based Analog Compute-in-Memory Array with Computing Accuracy Robust to Mechanical Strain and Temperature,"* T. Lan et al, Fudan U.)

On-chip learning in a ReRAM chip: Researchers from University of Paris-Saclay will demonstrate the first experimental realization of in-situ Metropolis-adjusted Langevin algorithm (MALA) training with ReRAM to employ device randomness with conditional sampling, allowing hardware to learn while capturing uncertainty. To provide reliable operation, near-sensor neural networks are required to identify unfamiliar inputs for which predictions may be unreliable. Employing fully on-chip conditional ReRAM-to-ReRAM sampling, the 32×64 ReRAM array uses its natural programming randomness directly for learning, avoiding repeated program-and-verify operations. This path does not require digitization of the source conductance, or computer-in-the-loop generation of the target programming condition. The fabricated two-transistor, one-resistor (2T1R) system achieves 96.8% ensemble accuracy on identifying four bird classifications and an out-of-distribution (OOD) area under receiver operating characteristic curve (AUROC) of 0.94 out of distribution metric with only 1.6 programming events per device. These results establish a variability-native route to adaptive, uncertainty-aware ReRAM systems.
(*Paper #31.4, "Experimental Metropolis-Adjusted Langevin Learning with Fully On-Chip ReRAM-to-ReRAM Sampling,"* B. W. Walker et al, University of Paris-Saclay)

E) Advances in High-Frequency and Power Devices

Record-Breaking GaN RF Transistors: Researchers from Xidian University will present a 0.25μm gallium nitride/aluminum nitride-on-silicon carbide (GaN/AlN-on-SiC) transistor that achieves a record X-band power with a density (P_{OUT}) of 59.8W/mm alongside a peak power-added efficiency (PAE) of 50.7% at 10GHz. This work identifies the current collapse at high drain bias (V_{DS}) as the dominant factor in P_{OUT} upscaling limitation and introduces distinct device pathways to overcome it. Representing the highest output ever reported for any GaN RF transistor, this milestone delivers an impressive 50% improvement over the previous state-of-the-art. The breakthrough was driven by an enhanced AlN buffer layer with reduced thermal boundary resistance,

demonstrated by narrowed rocking-curve widths, co-optimized with a silicon nitride (SiN) advanced passivation scheme that significantly suppresses current collapse. These results provide a robust technological foundation for next-generation high-power microwave applications.
(*Paper #19.7, "GaN RF HEMTs with Record P_{out} of 59.8W/mm at 10GHz,"* K. Zhang et al, Xidian University, Dynax Semiconductor, & University of Hong Kong)

Advanced Optically Driven GaN Power Devices: Researchers from Peking University will demonstrate a 1200V GaN power complementary optically triggered (COT) switch. While optically triggered power switches have shown promise for high-voltage conversion systems, providing isolation between low-voltage control signals and high-voltage signals, previous generations of these devices had slower switching speeds, inferior on-resistance and breakdown voltage (*BV*) compared to their electrically driven counterparts. In this paper, researchers describe an optically triggered lateral GaN switch that combines a high electron mobility transistor (HEMT) and a photo diode driven by complementary ultraviolet (UV) and infrared (IR) optical signals. The device achieves a breakdown voltage (BV) of 1945V and a specific on-state resistance (R_{SP}) of 4.1mΩ•cm^2 – comparable to electrically driven GaN switches. The switch shows a turn-on time of 58µs and a turn-off time of 1.2µs, representing best-in-class turn-off speed among high-voltage optically triggered GaN switches**.**
***(Paper #28.2, "Complementary Optically Triggered 1200-V Lateral GaN Switch with RSP-BV Performance Comparable to Electrically Driven Switches,"* J. Yang et al, Peking University)**

F) Advances in Sensing and Imaging

A Compact MEMS Magnetometer in Standard CMOS: National Tsing Hua University researchers will present a Lorentz-force magnetometer fabricated entirely in a standard TSMC 0.35µm two polysilicon layer / four metal layer (2P4M) CMOS process without the need for magnetic materials. Microelectromechanical systems (MEMS) have emerged as a promising alternative to conventional inertial measurement unit (IMU) technologies, such as Hall effect, magnetoresistive, and flux-gate sensors, offering compact size, low power consumption, and process compatibility with semiconductor technologies. The device features a stacked spiral coil embedded in the resonating plate that recirculates the drive current to multiply the Lorentz-force torque, while the suspension beams are shaped to concentrate the resulting stress onto piezoresistive sensors, amplifying the electrical signal without enlarging the device. The device occupies just 0.032mm^2, with 83nT/√Hz resolution, a sensitivity of 0.25Vrms/T, and a ±49mT full-scale range within 1% nonlinearity.
(*Paper #22.3, "An 83nT/√Hz 0.032mm² CMOS-MEMS Lorentz Force Magnetometer with ±49mT Full-Scale Range,"* W. Fan & M. Li et al, National Tsing Hua University)

Monolithic 3D Integrated Quantum Sensing for Epilepsy Detection: A team from the University of Hong Kong will introduce a monolithically 3D-integrated intelligent diamond quantum sensor designed to overcome the severe latency and data-transmission bottlenecks of conventional frame-based systems. Built on a 180nm CMOS platform, the architecture integrates an optical filter, a programmable-responsivity phototransistor array for in-sensor spatiotemporal signal processing, and a tantalum oxide (TaO_x) resistive random access memory (RRAM) crossbar for near-sensor in-memory classification. By processing sensing data on-chip, the device accelerates magnetic resonance measurements by 14x and significantly reduces energy consumption. Coupled with an RRAM perceptron, the device decodes neural signals for dynamic responsive neurostimulation (RNS) epilepsy detection with 98.3% accuracy. With future integration with other components, this technology points toward a self-contained edge quantum sensor.
(*Paper #4.6, "Monolithic 3D Integration of Optical Filter, Phototransistor, and RRAM for In-/Near-Sensor Computing in Diamond NV Quantum Sensing,"* Z. Du et al, University of Hong Kong)

Energy Optimized Optical Networking for AI Backplanes: Researchers from Samsung will present a fully integrated 32Gb/s/λ, 8λ dense wavelength division multiplexing (DWDM) optical engine: a 4nm FinFET CMOS

IC is assembled using fine-pitch thermo-compression bonding to a photonic IC (PIC) implemented on a 300mm platform. The PIC integrates eight cascaded micro-ring modulators (MRMs) along a transmit (TX) bus, and eight micro-ring filters (MRFs) with germanium (Ge) photodetectors long a receive (RX) bus on a 200GHz DWDM grid; the logic adopts a source-forwarded-clock architecture that eliminates power-hungry per-lane clock-and-data recovery. Total engine energy, including the external laser and MRM/MRF resonance tracking, is 3.85pJ per payload bit, including external laser power and MRM/MRF resonance tracking. All the component technologies in this device were designed, fabricated, assembled, and tested on production-grade lines, establishing a manufacturing foundation for turnkey AI optical engines.
(*Paper #8.4, "A 32-Gb/s/λ, 8-λ Fully Integrated DWDM Optical Engine for Co-Packaged Optics,"* S. Yun et al, Samsung Electronics)

Advanced Chip-on-Wafer Stacking: Researchers from Sony Semiconductor will detail a multi-chip CMOS image sensor architecture utilizing advanced hybrid Cu-Cu chip-on-wafer (CoW) stacking technology. Three-dimensional (3D) stacking technology that integrates logic, memory ICs, and sensors has emerged as a promising solution for fabricating next-generation devices with high performance, multi-functionality, and low power consumption. In this paper, Sony will describe key enabling developments toward this goal, including a new leakage suppression technology for ultra-thin 3μm-thick logic chips layer, and wafer-level gap-fill planarization with the bonding-surface topography down to 200nm. Using these technologies, a prototype device combining two stacked logic chips with 6μm pitch hybrid Cu-Cu bonding was demonstrated. This architecture integrates multiple logic chips on the backside of the sensor wafer, enabling functional enhancement without increasing the sensor-chip area. These results demonstrate that the proposed CoW technology provides an effective platform for realizing scalable heterogeneous integration and flexible functional scaling toward future high-functionality compute-in-sensor (CIS) architectures.
(*Paper #36.1, "Scalable CMOS Image Sensor Architecture Utilizing Advanced Chip-on-Wafer Stacking,"* Y. Nonaka et al, Sony Semiconductor)

G) Thermal Simulation & Device Reliability

Reliability of Next Generation Transistors: Researchers from imec will present the first BTI reliability study of monolayer p-type tungsten diselenide (WSe_2) FETs fabricated on standard 300mm wafers with a scaled 50nm contacted gate pitch (CGP). The paper describes data from applying maximum overdrive voltage $|V_{ov}|$ of 1.1V/25°C and 0.41V/125°C for an extrapolated lifetime of 10 years – a first for fully manufacturable 2D-channel technology. Negative bias temperature instability (NBTI) stress induces a negative threshold voltage (V_{th}) shift, identifying hole trapping in the gate dielectric stack as the dominant mechanism. At low voltages relevant to normal operation, reversible aging from hole trapping dominates the V_t shift and 10-year lifetimes are enabled. At high stress voltages, non-reversible aging emerges due to bulk and interface trap formation, indicating the need to quantify reliability lifetimes at appropriate voltage conditions. These results define the safe-bias window for scaled WSe_2 pFETs, underlining BTI as a critical reliability factor for manufacturable 2D-channel technologies.
(*Paper #41.2, "First BTI Investigation of 300mm Integrated 50nm-CGP Monolayer WSe_2-Channel pFET Devices*," M. Ouaicha et al, imec)

3D Integrated Active BSPDN with Thermal-Reliability Co-Design: KAIST researchers will demonstrate the first vertically integrated active power-delivery platform combining CMOS, GaN power switches, and 3D pillar capacitors for active backside power delivery networks (BSPDNs) with system- and device-level optimization. System-level thermal measurements reveal capacitor operating temperatures up to 160°C, motivating a dual heat-spreading-layer solution that lowers capacitor temperature by 33°C and decreases thermal resistance from 7.50K to 3.60K•mm/W. Through aluminum-doped hafnium zirconium oxide (Al-HZAO) dielectric engineering and optimized pillar geometry, the resulting 3D capacitor achieves 138fF/μm² capacitance density and a nearly 20-year projected lifetime at the actual operating temperature. These results establish that system-level thermal analysis and management, together with temperature-aware device reliability design can enable practical 3D-integrated active power delivery for AI and HPC chips.

(*Paper #27.5, "System-Level Thermal Management and Capacitor Reliability Enhancement in Heterogeneous 3D Integrated Power Delivery System*," M. Lee et al, KAIST)

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Here are definitions of some important technical terms you may find useful:

- **Back-End/BEOL** and **Front-End/FEOL** -- In integrated circuit manufacturing, transistors and other active devices are built first (at the front end of the manufacturing line or FEOL), while the interconnect, or the wiring, is built afterward, at the "back end" of the manufacturing line (BEOL). The BEOL imposes a much lower thermal budget than the FEOL which includes doping activation and gate stack anneals.
- **Carbon nanotube (CNT) –** A cylinder made of carbon atoms, measured in nanometers (nm). Depending on its chirality it may possess metallic or semiconducting properties
- **CMOS/MOSFET/FET**-- Most transistors today are FETs, or field-effect transistors. CMOS (complementary metal oxide semiconductor) technology requires FET devices of both polarities (n-FETs and p-FETs) which turn on at the application of a positive or negative gate bias, respectively. Generically they are called MOSFETs, or sometimes MOS transistors.
- **CFET, or complementary FET** – A developing transistor architecture where p-FET and n-FET devices are built on top of one other instead of side-by-side. This vertical stacking makes CFET-based architectures potentially suitable for future highly integrated and 3D devices; thus, CFETs are the subject of great research interest.
- **Compound/III-V Semiconductors** -- Most semiconductors are silicon-based, but researchers continue to investigate other semiconducting materials with higher electron or hole mobilities because they can be used to make faster devices. The tradeoff is that the materials are harder to work with than silicon. Compound semiconductors are made of two or more elements (e.g. GaAs, InP, GaN, etc.) that are generally found in groups III and V of the periodic table of the elements.
- **Depletion-mode MOSFET** – A MOSFET transistor which is normally "on" at zero gate voltage.
- **DHBT** – Double heterojunction bipolar transistor
- **DIBL** -- Drain-induced barrier lowering is a parasitic short-channel effect in MOSFETs that influences threshold voltage.
- **E-mode (enhancement-mode) MOSFET** – A MOSFET transistor which is normally "off" at zero gate voltage,.
- **Electromigration** -- A serious reliability issue. At tiny dimensions some materials tend to physically move when current flows through them, leading to voids, gaps or outright breaks in what should be a uniform material.
- **Electron mobility** -- A measure of the velocity of electrons in a semiconductor. The corresponding measure for positive charge, or holes, is termed hole mobility.
- **FinFET** -- A transistor whose shape resembles a fin, usually with multiple gates surrounding it for better on/off control.
- $\mathbf{f_T}$ -- a measure of transistor speed known as unity current gain cutoff frequency, above which the device loses its amplifying capability.
- $\mathbf{f_{max}}$ -- a measure of transistor speed denoting its maximum oscillation frequency
- **Gate-all-Around (GAA) Device** – A transistor with multiple gates surrounding the channel on all sides.
- **HBT –** A type of bipolar transistor which uses different semiconductor materials for the emitter and the base, creating a heterojunction. HBTs are high-frequency devices, used in applications such as radio frequency (RF) systems and where high power efficiency is required, such as RF power amplifiers in cellular phones.
- **HEMT** -- A HEMT, or high-electron-mobility transistor, is a field-effect transistor with a channel built from a sandwich of two materials with different energy band gaps, instead of a channel built from a semiconductor and separated from the gate electrode by an insulating oxide, as is the case with MOSFETs. HEMTs operate at higher frequencies than ordinary transistors, up to millimeter-wave frequencies, and are used in high-frequency products such as cell phones, satellite television receivers, voltage converters, and radar equipment.
- **High-*k* Dielectrics/Metal Gates (HKMG)** -- A dielectric is an insulator, and "*k*" is relative permittivity, a measure of how high capacitance will be under the same physical thickness. A higher numerical value for "*k*" leads to a better insulating performance without increased physical thickness of the insulating layer. For the gate of a transistor, which turns it on and off, a high-*k* dielectric is critical because if current leaks through the gate, the transistor won't work properly. In the past gates were usually made of polysilicon with an oxide dielectric, but these

are not scalable to meet the needs of the latest technology generations. Other good dielectrics exist but they aren't compatible with polysilicon gates. The latest generations of MOSFETs use metal gates with high-*k* dielectrics to enable continued scaling and higher device performance.

- **III-V** -- see Compound/III-V Semiconductors
- **Integrated Circuit** -- A tiny electrical circuit built on a semiconducting substrate.
- **Internet of Things (IoT)** -- The idea of giving everyday objects network connectivity, allowing them to send and receive data.
- **Lithography/Photolithography/EUV Lithography** -- Transistors are built on chips using photolithography, a process by which light is shone through a patterned photomask onto a chip's surface. The light transfers a copy of the image on the mask to a light-sensitive layer on the chip's surface, in much the same way the image on a photographic negative is transferred onto photo paper. The chip's surface is then engraved with chemical etches and other treatments in order to build the patterned devices and circuits. Right now various tricks and tweaks enable us to build transistors smaller than the wavelength of light used to pattern them. But for future technology generations of ultra-small transistors, the shorter wavelengths of extreme ultraviolet light (EUV) may be needed. Researchers are working to develop cost-effective, high-throughput EUV systems.
- **Low-*k* Dielectrics/Interconnect** -- Interconnect refers to the copper lines that connect devices on a chip. The tiny widths and close proximity of adjacent lines introduce resistance and capacitance delays that can hinder chip performance. Here a low-*k* dielectric is needed, to insulate the copper lines while minimizing capacitance increase, but these materials are fragile and pose many challenges.
- **MEMS/NEMS** -- A micro-electromechanical system/nano-electromechanical system, containing micrometer-scale moving parts (the former) or nanometer-scale moving parts (the latter).
- **MRAM** – Magnetoresistive Random Access Memory, a type of non-volatile memory that stores data not as an electrical charge, but as a magnetic state. See STT-MRAM.
- **Multi-chip Modules** -- An electronic package containing multiple ICs, other semiconductors and/or other chip modules.
- **Moore's Law** -- An observation made in 1965 by Intel's Gordon Moore, who said that the number of transistors which can be placed on an integrated circuit doubles about every two years. Subsequent events have proved him correct but it's getting harder to do.
- **Negative capacitance** – A mathematical measure of the momentary change in capacitance of a ferroelectric device during switching, which can aid in the design of more energy-efficient ferroelectrics. A ferroelectric material switches its polarization when a critical voltage is applied. In some cases that voltage causes a large electrical charge to build suddenly on the material's surface. That surface charge may quickly grow to exceed the magnitude of the charge already being supplied to the device from an external power supply. If at that moment a resistance is introduced between the device's electrodes and the charge from the power supply is reduced, then the voltage would decrease even as the overall level of charge in the ferroelectric material is still increasing because of the surface accumulation. Because capacitance is charge divided by voltage, it would have a negative value at that moment.
- **n-FET/p-FET or n-channel/p-channel** -- All MOSFETs come in two varieties that work together in a complementary fashion, N and P. These act like switches which turn on at a positive and a negative gate bias, respectively.
- **Phase-Change Memory/PCM** -- Phase-change materials have crystalline and non-crystalline states that are used to represent the digits "0" or "1," the basis of computer memories. Electrical current is used to toggle between the two states – heat from the current melts the material to change its state.
- **PPAC/Scaling/Integration** -- Scaling is making transistors and other circuit elements smaller so that more will fit on a chip. Integration is combining different circuit elements onto a chip to add more functions. These effects lead to chips that offer greater PPAC benefits (performance, power, area and cost).
- **Self-Assembly/"Bottom Up"** -- A manufacturing method used at the nanometer scale, making use of the fact many biological systems automatically self-assemble into various molecular or other structures. Self-assembly techniques imitate these strategies by encoding a desired structure into the shape and properties of the molecules that are used. This compares to traditional lithography, where the structure is carved out of a block of matter. Self-assembly is thus referred to as a 'bottom-up' manufacturing technique, as compared to lithography, a "top-down" technique.
- **Semiconductor** -- A material that can be made to conduct or to block the passage of electrical signals, giving the ability to store and process data.
- **Si, SiGe and SOI –** Si is silicon, while SiGe is silicon-germanium. SiGe allows CMOS logic to be integrated with heterojunction bipolar transistors to make mixed-signal integrated circuits for use in radio frequency and other high-

speed, low-power applications. SOI refers to a silicon-on-insulator substrate, used to reduce parasitic capacitance and thereby improve performance.

- **SOC/System on a Chip** – An integrated circuit that integrates all or most components of a computer or other electronic system. These components almost always include a central processing unit, memory, input/output ports and secondary storage, all on a single substrate, typically for embedded applications.
- **Strained silicon & SiGe stressors** -- Silicon is said to be "strained" when its atoms are pulled farther apart or closer together than normal. Doing so alters the structure of the material and, hence, the atomic forces that govern the flow of electrons through the silicon, enabling transistors built with it to operate faster and /or at lower power. The external **stressors** which impart strain are materials with slightly different atomic structures than silicon. For example, a common way to strain silicon is to build a silicon layer on top of a silicon-germanium (**SiGe**) layer. The silicon atoms will align with the atoms of the SiGe layer, which lie farther apart.
- **SRAM** -- A type of computer memory (static random access memory) that uses six transistors to store each bit of information. It can be written to and read from very quickly.
- **SS, Subthreshold Swing or Inverse Subthreshold Slope** -- A measure of a MOSFET transistor's current/voltage characteristics. The steeper it is, the more abruptly the device can turn on and off, which is desirable.
- **STT-MRAM** -- Spin-Transfer Torque Magnetoresistive RAM, an advanced type of MRAM that offers fast write speeds, the potential for very high density, low-power operation, and long endurance.
- **Technology Generations/Nodes** -- Production of 7nm/10nm devices by leading companies is established; the transition to 3nm/5nm is well under way with the first 3nm devices now in production; and 2nm technology is under development.
- **Transconductance (Gm)** -- A measure of transistor performance. Transistors with higher levels of transconductance can amplify signals more efficiently than low-transconductance devices can. Technically, in a transistor it is the ratio of change in output current to change in input voltage.
- **Transistor** -- A tiny electrical switch that makes electronic systems possible. It has no moving parts and is made from semiconductors, usually silicon. Transistors can be ganged together by the millions on chips and programmed to sense inputs, to process information and to deliver outputs.
- **TSV** – Through-silicon via, a vertical electrical connection (i.e. a "via") that passes through a silicon wafer or die. TSVs are used to create 3D integrated circuits and packages of stacked microchips.