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# *The 2026 IEEE International Electron Devices Meeting To Feature the Theme "Devices at the Heart of the Intelligence Revolution" and Showcase the Latest Microelectronics Technology*

- *Late News! A14 CMOS NanoFlex™ Pro platform technology from TSMC*
- *First Germanium nanoribbon for CFET hybrid channel integration from Intel*
- *Record high-voltage IGZO vertically stacked GAA transistor from imec*
- *First 48-die TSV-free organic interposer stacking technology by The University of Tokyo*
- *Record-breaking GaN RF HEMTs with X-band power of 59.8W/mm at 10GHz by Xidian U.*
- *First demonstration of dual-sided CMOS (frontside FinFETs & backside 2D FETS) by Peking U.*
- *Scalable CMOS image sensor using advanced hybrid chip-on-wafer stacking by Sony*
- *First chip-level 176-layer 4D Ferroelectric NAND by SK hynix*
- *Two Focus Sessions on topics of next-generation emerging technologies:*
    - *Semiconductors for Quantum Computing*
    - *System-Level Optimization Combining Logic, Memory, & Packaging*

SAN FRANCISCO, CA (November 5, 2026) – The 2026 IEEE International Electron Devices Meeting (IEDM) will bring together scientists and engineers in the world's premier technical conference to present the latest R&D work in semiconductor devices, microelectronic technologies, and emerging computer architectures. Researchers from industry, academia, and government will present the latest innovations shaping the future of electronics. The 72nd annual IEEE IEDM conference will be held December 12-16, 2026 at the Hilton San Francisco Union Square hotel, with online access to recorded content available afterward.

Highlighting the theme *"Devices at the Heart of the Intelligence Revolution,"* the IEDM technical program will feature 280 presentations, along with Focus Sessions, Tutorials, Short Courses, an evening panel, a career luncheon, supplier exhibit, and IEEE/EDS award presentations.

"We are seeing again many efforts across industry and research teams to especially address the unique challenges posed by AI. This spans memory performance and density, including 3D developments, logic technology, and more emerging approaches with 2D materials and in-memory computing. The system level integration and co-design is also front and center," said John Paul Strachan, IEDM 2026 Publicity Chair, Director of Peter Grünberg Institute, Forschungszentrum Jülich, and Professor at RWTH Aachen University (Germany).

"While these traditional computing paradigms continue progress, IEDM also has its eyes on future technologies such as quantum computing."

"The defining trend of the year is that technological breakthroughs are no longer limited to individual devices or isolated fields," said Sandy Liao, IEDM 2026 Publicity Co-Chair and Director at TSMC. "Progress increasingly depends on co-optimizing materials, transistor architectures, memory, interconnects and packaging as an integrated system. The breadth of work at IEDM 2026 shows how the semiconductor community is redefining scaling for the intelligent-computing era."

Here are details of the 2026 IEEE International Electron Devices Meeting program:

## Plenary Session Presentations – Monday, Dec. 14

*"AI Driven Semiconductor Paradigm Shift: Optimizing the Semiconductor Industry from Device Scaling to System Integration,"* by Naga Chandrasekaran, Executive Vice President – Chief Technology & Operations Officer – General Manager, Intel Foundry
Artificial intelligence is transforming how we live, work, and innovate, while reshaping semiconductor technology. Meeting AI's extraordinary demands for performance, bandwidth, efficiency, and reliability requires innovation across the full technology stack—from materials and devices to architectures, packaging, and manufacturing. This accelerating transformation is driving unprecedented advances in semiconductor technology roadmaps and capabilities.

*"Driving AI Memory Innovation: From Device Technology to AI Memory Platform,"* by Yunik Son, Vice President of Device Technology Solution, SK hynix
As AI workloads scale, memory performance is becoming critical to overall system efficiency. Advances in 3D architectures, wafer bonding, and memory-optimized transistor technologies are enabling greater bandwidth, power efficiency, and reliability. AI-native design methodologies spanning devices, circuits, packages, and systems are transforming memory into a strategic enabler of AI innovation.

*"Technology Trends in the IDM Semiconductor Business,"* by Fabio Gualandris, President, Quality, Manufacturing & Technology, STMicroelectronics
ST is advancing the future of intelligent manufacturing through fab digitalization and advanced packaging, enabling faster innovation, greater system flexibility and heterogeneous integration. Building on these capabilities, ST is expanding silicon photonics, next-generation computing, and sensing and actuation technologies. Automation, robotics and virtual R&D further accelerate design-to-manufacturing optimization across its diverse technology portfolio.

## Tutorial Sessions – Saturday, Dec. 12

Presented by experts in the field to bridge the gap between textbook-level knowledge and leading-edge current research, the Saturday tutorial sessions on emerging technologies introduce attendees to new fields of interest. There are three time slots, each with two tutorials running in parallel:

**1:30 p.m. - 2:50 p.m.**

- *Evolution of the Transistor from Planar to Nanosheet and Beyond,* Larry Bair, AMD
- *Chiplet, Heterogeneous Integration, 3D Stacking Technologies Principles and State of the Art*, Oliver Noblanc, ST Micro

**3:05 p.m. - 4:25 p.m.**

- *Memory Technologies and System Co-Optimization in the AI Era: Past, Present and Future*, Fatih Hamzaoglu, Intel
- *AI in Physics-based Semiconductor Modeling: From PDE-constrained Learning to Agentic TCAD/DTCO Workflows,* Pratheep Balasingam, Synopsys

**4:40 p.m. - 6:00 p.m.**

- *Diverse Memory Technologies for Adaptive Computing: From Device Physics to Cooperative Architectures*, Elisa Vianello, Leti
- *Advanced Optical Devices & Wafer-Scale Assembly for Next-Generation CPO and Optical I/O*, Joris Vancampenhout

## Short Courses – Sunday, Dec. 13

Two full-day Short Courses are each focused on different aspects of a single technical topic, providing an opportunity for attendees to learn about important developments, and to network with global experts.

**Short Course 1: Logic and System Innovations Powering the AI Era**, organized by Marko Radosavljević

- *Distributed Network Design for AI: Evolution, Scaling, and System Implications*, Brad Beckmann
- *Advanced Logic Transistor Scaling & 3D Architectures in the Angstrom Era*, Seung Hoon Sung, Intel
- *Edge Device Performance/Power Enhancement in Mobile SOC Platform Through Device to DTCO to STCO*, Jun Yuan, Qualcomm
- *Atomic Layer Processing: Applications in Advanced Semiconductor Devices*, Thorsten Lill, Lam Research
- *Reliability Challenges in Advanced Packaging and System-Level Interaction*, Yao-Chun Chuang, TSMC
- *Cryogenic electronics for quantum computing*, Loïc Le Guevel, Google

**Short Course 2: Powering Next-Generation AI and HPC with Advanced Memory Technologies**, organized by Nanbo Gong, IBM

- *Memory-Centric Computing for the Generative AI Era*, Damien Querlioz, Universite Paris-Saclay
- *HBM Design and Technology Challenges for AI Generation*, HyunBae Lee, SK hynix
- *Oxide-Semiconductor Channel Transistor DRAM (OCTRAM): High-Density and Low-Power Consumption DRAM Technology for Sub-10nm Nodes & Beyond*, Keiji Ikeda, Kioxia
- *The Evolving Role of NAND: Technology and System Scaling from Traditional Storage to Memory-Storage Convergence*, Kishore Muchherla and Akira Goda, Micron
- *Spintronics for MRAM and Beyond*, Shunsuke Fukami, Tohoku University
- *Chiplet & Advanced Packaging Technologies for AI & HPC Systems*, John Knickerbocker

## Evening Panel Session – Tuesday evening, Dec. 15

The IEDM evening panel is held as an interactive forum where experts give their views on important industry topics, and is designed to foster an open exchange of ideas, with audience participation encouraged. This year's panel will be moderated by Dr. Ian Cutress, CEO and chief analyst at More than Moore. It will focus on the theme, "*Rewriting the Rules of Semiconductor Manufacturing: Why the Old Manufacturing Model May Not Be Enough."*

Topics for the panel will include:

- Speed, Scale, and the Cost of Faster Learning
- The Foundry Model Meets a More Specialized Future
- Transistors, Tools, and the Factory Model
- The Capital Reality Behind Manufacturing Disruption
- Low Volume, High Value, and the Rise of Specialized Manufacturing
- The 450mm Warning for Every "Obvious" Manufacturing Shift

The panelists will include:

- Ben Sell (Vice President and GM of Logic Technology Development, Intel)
- Kazunari Ishimaru (Chief Technology Officer, Rapidus)
- Nicholas Kelez (CEO and Chief Technology Officer, xLight)

## Vendor Exhibition

A vendor exhibition will be held as part of IEDM from December 14 – 16.

**Further information about IEDM**
For registration and other information, visit www.ieee-iedm.org.

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