72nd International Electron Devices Meeting

Devices at the Heart of the Intelligence Revolution

2026 International Electron Devices Meeting

December 12-16, 2026

Hilton San Francisco Union Square
San Francisco, CA

IEDM is pleased to announce increased technical focus in the area of:

ADVANCED LOGIC TECHNOLOGY (ALT)

Topics

Papers are solicited in the following themes of interest:

- CMOS platform technologies & opportunities
- Logic device performance and circuit design challenges
- Advanced, novel process integration schemes and (applications-driven) scaling approaches
- Innovations and advances in process control and metrology.
- Design technology co-optimization (DTCO), System technology co-optimization (STCO)

New or trending areas include:

- GAA (Gate-All-Around) nanosheet-based devices and circuits; novel channel materials.
- Sequential, monolithic 3D integration, heterogenous chiplets, 2.5/3D integration, thermal management
- Logic for memory
- Interconnects (BEOL, Backside power delivery)
- BEOL compatible transistors

Paper Submission

Deadline: July 16th

Single submission of final, four-page paper

Electron Devices Society

IEEE

For More Information

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