70th International Electron Devices Meeting

2024 IEDM Conference Proceedings

Shaping Tomorrow's Semiconductor Technology

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Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

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Topics of Interest

ADVANCED LOGIC TECHNOLOGY (ALT)

Papers are solicited in the areas of CMOS platform technologies and applications (e.g., HPC, LOP, mobile, automotive, low-temperature CMOS, etc.), logic devices and circuits, process integration schemes for advanced nodes, innovations in material, process and metrology techniques, and design technology co-optimization (DTCO) and system technology co-optimization (STCO). Platform technologies include state-of-the-art Si and beyond-Si channel devices, gate-all-around devices, stacked devices with different polarity transistors, advanced interconnect, novel power distribution integration schemes, heterogenous 2.5D/3D integration schemes, and BEOL compatible transistors. Device architecture, device design and analysis, process integration, module advancements in process and patterning, metrology, physical layout effects, techniques for reduced variability, yield, methodologies and solutions for DTCO/STCO in the solicited areas are of high interest.

EMERGING DEVICE and COMPUTE TECHNOLOGY (EDT)

Papers are solicited on emerging nanoelectronic devices and physics. This includes devices based on novel transport and control mechanisms such as tunnel FET, negative capacitance FET, topological materials and devices, phase transitions, ferroelectrics and quantum effects. Devices based on low-dimensional systems including 2D materials, CNTs, nanowires, and quantum dots are welcomed. Devices with novel device functions and/or novel materials for neuromorphic compute, approximate and analog compute, and non-charge-based logic such as spintronics are key topics. Furthermore, emerging state machines and time dynamical compute systems are also of interest. Qubit devices as well as devices and systems designed to enable quantum computing, quantum simulation and quantum annealing are of high interest. Papers in EDT focus primarily on device physics, innovative transistor structures, and novel concepts; more mature "platform candidate" papers, such as based on established two-terminal resistive memories, should be submitted to ALT and MT. Reliability assessment of emerging devices are also solicited here, while assessments for more mature devices should be submitted to RSD.

MEMORY TECHNOLOGY (MT)

Papers are solicited in the areas related to embedded and standalone memory technology. This includes advances in both conventional memories including SRAM, DRAM and Flash, and emerging memories including ReRAM, MRAM, PCRAM, ferroelectric memory, crosspoint memory and selectors, organic memory and NEMS-based memory, as well as their applications in the areas of compute-in-memory, and machine learning. Topics span from demonstration of novel device concepts to fully integrated memory arrays, and from product prototyping to manufacturing related challenges and solutions. Demonstrations of manufacturing maturity of emerging memories are of high interest. Submission of papers on novel device concepts and demonstrations, novel integration schemes, novel circuit design schemes, and novel memory architectures that enhance memory performance or improve system level performance in compute-in-memory and AI applications is strongly encouraged.

MICROWAVE, MILLIMETER WAVE and ANALOG TECHNOLOGY (MAT)

Papers are solicited in the areas of high frequency device technology, device physics as well as high frequency circuit applications in the micro, mm-wave and THz frequency spectrum. Device physics and technology include based on Si, SiGe, wide bandgap compound semiconductors like III-Vs, III-nitrides, gallium oxide and silicon carbide. Circuit aspects covers analog front ends, filters, beam formers, switches, LNAs, PAs, tunable passives, antenna arrays, SAW/BAW and RF devices for mixed signal, energy harvesting circuit and IoTs, circuit and device interaction for higher system integrity, readout IC targeting quantum computing in the micro and mm-wave domain.

MODELING and SIMULATION (MS)

Papers are solicited on theoretical approaches to electronic devices, including logic devices, memory devices, optical devices, interconnects and (bio)sensors. Theoretical approaches include analytical, numerical and statistical approaches applied to structures with dimensions ranging from atomistic over device dimensions to full-chip dimensions, including physics-based compact modeling. Key to submissions is, that the device innovation is central, either through predictive insight in the potential of novel device concepts, predictive analysis revealing significant improvement to devices, breakthroughs in the theoretical understanding of the device operation, breakthroughs in the understanding of device processing enabling improved device performance, novel insights in variability, reliability and yield issues, breakthrough in device optimization based on DTCO. Topics also include neuromorphic computing, quantum computing, spintronics, low-dimensional devices, ferroelectrics, thermal modeling, 3D/heterogeneous integration, electro-chemical/mechanical devices. Comparison with experimental data, model calibration and multi-scale simulation chains are highly encouraged.

Program

See the Appendix for all abstracts and speaker bios.

Tutorials

The tutorials are in their fifteenth year and are standalone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields and facilitate

understanding of the technical sessions. In contrast, the traditional short courses are focused on a single technical topic.

Tutorials

Saturday, Dec. 7
1:30 PM – 6:00 PM

T1 | Scaling with Wafer Level Integration Technologies
1:30 PM – 2:50 PM
Continental 6 – 9
Chih Hang Tung, Deputy Director at TSMC

The role of System integration and packaging in semiconductor industry has transformed in recent years. Driven by markets diversification and front-end transistor scaling challenges, wafer Level System Integration enables system scaling complementing Moore's Law transistor scaling. This tutorial focus on technologies enablement by chip stacking and Wafer level interconnection. Technologies and challenges from electrical, structural, and to thermal are discussed. Industry solutions are covered. Novel and new heterogeneous integration of non-CMOS components, including photonics are also discussed for their potential future roles in system Power, Performance, Area, and Cost (PPAC) scaling.

T2 | Advances in CMOS Technologies and Future Directions for Cell Height scaling
1:30 PM – 2:50 PM
Continental Ballroom 1-5
Anupama Bowonder, Principal Engineer, Process Technology Development at Intel

Artificial intelligence has evolved over the decades from facial recognition and language translation to the exciting era of synthesizing knowledge. AI can now compose artwork, diagnose diseases and write computer code and even design integrated circuits. Along with advances in machine learning algorithms and large volumes of data to train on, AI is heavily influenced by chips that can enable large volumes of parallel, energy efficient computation. These faster, more power efficient chips capable of more computational power still rely heavily on advances in CMOS transistor innovation coupled with other enhanced cell scaling technologies.
After a decade of successfully utilizing multi-generation FinFET technology, the industry is preparing to shift to a new architecture for nanosheet field-effect transistors (NSFET), commonly known as gate-all-around (GAA). Nano sheet performance can be very easily extended by hetero channels which use silicon sheets for NMOS and SiGe sheets for PMOS. Heavily being explored as the natural extension of GAA transistors are Fork Sheet transistors using a dielectric wall between N and P transistors are being explored to reduce cell heights by minimizing N-P spacing. Designers could use extra space to shrink logic cells or use extra room to build wider nano sheets for high performance.
And finally stacking N and P nano sheets atop each other (CFETs) would be enable the ultimate in area scaling by cutting the size of some circuits in half. CFETs remove the N-P spacing from the cell height considerations. Vertical stacking comes with tremendous fabrication challenges which will need innovation. Monolithic and sequential integration approaches will be discussed and addressed. Last but not the least to enable more computation chips also need efficient power delivery. CMOS innovations are being coupled with backside power delivery for signal integrity and reduced routing congestion. Backside

power delivery options will be reviewed along with the needs for innovation in thinning the backside silicon to deliver direct and low resistance connections.

T3 | Co-packaged photonics for improved energy efficiency and performance of AI applications
3:05 PM – 4:25 PM
Continental 6 – 9
Clint Schow, University of California Santa Barbara

The integration of high-speed optical interfaces into first-level chip packages, often referred to as co-packaged optics (CPO), has been an active area of research for decades. In the last several years, the technology has moved to a phase of product development and deployment, initially motivated by the need to efficiently scale bandwidth in datacenter networks. More recently, AI has eclipsed other applications, driving explosive growth in both computing power and optical interconnect bandwidth. CPO is a natural fit for AI applications due to the potential to efficiently transport more bandwidth between compute nodes. This tutorial will explore the bandwidth and power demands of AI applications that motivate the future proliferation of CPO and survey the current landscape of CPO integration strategies and products. Achieving large-scale electronic/photonic convergence can deliver significant dividends by maximizing efficiency and performance, but raises significant challenges that provide fertile ground for innovation.

T4 | Current understanding and future challenges of gate dielectric breakdown reliability
3:05 PM – 4:25 PM
Continental Ballroom 1 – 5
Ernest Wu, IBM

Dielectric reliability has faced new challenges with the increasing complexities of new device structures such as the gate-all-around (GAA) nanosheet (NS) devices and the introduction of new materials such as two-dimensional (2D) gate dielectrics due to technology scaling. Meanwhile, the requirements become more urgent than ever for breakdown evaluation and qualification to maintain the same or more stringent reliability specifications. These demands require a thorough understanding of failure statistics and a detailed knowledge of failure mechanisms in dielectric breakdown (BD). This tutorial will describe and summarize fundamental BD phenomena found on various gate dielectrics over a wide range of dielectric thicknesses across multiple technology nodes. I will review defect generation processes and the associated statistical descriptions at different stages such as stress-induced leakage current (SILC), onset of soft BD (SBD) events, and post-BD (PBD) events, which eventually lead to device and/or circuit failures. In addition, several voltage acceleration models, especially the power-law model, widely used in BD reliability assessment, will be discussed along with the status of microscopic BD physics. Concerning technology qualifications, we will highlight the impact of acceleration models and post-BD methodologies, recently adopted by JEDEC standards https://www.jedec.org/system/files/docs/JESD263.pdf for the global microelectronics industry. A full technology qualification encompasses not only intrinsic reliability but also variability attributes. Thus, methodologies to mitigate these variability issues will be provided in this tutorial. Moreover, I will review the traditional percolative statistics in terms of thickness- and area- scaling of BD phenomena in light of new reports based on Markov modeling work. On the other hand, I will discuss new area scaling phenomena such as reverse area scaling recently reported in HfO2 as well as the latest development for TDDB reliability of 2D gate dielectrics including layer-by-layer BD effect found in hexagonal boron-nitrides (h-BN). Finally, future opportunities for research and development works in areas of dielectric breakdown will be outlined.

T5 | EUV Lithography for the Age of AI
4:40 PM – 6:00 PM
Continental 6 – 9
Anthony Yen, ASML

EUV lithography entered the high-volume production of semiconductor chips in 2019, at the 7-nm node of logic integrated circuits, and enabled the continuation of Moore's Law. Since then, EUV lithography has been an essential technology in the production and research and development of advanced logic devices. It is now also heavily used in the production of DRAM chips. Capability and flexibility of the newly released high-numerical-aperture EUV exposure systems will no doubt enable the patterning of more sophisticated logic devices, DRAM chips, and perhaps new-type memories of the future.
I will start this tutorial by giving an update on the status of EUV lithography, followed by a review of the principles of projection lithography in general: how imaging takes place near the resolution limit of the exposure tool, including how water immersion extends the resolution of 193-nm optical lithography. Next, I will discuss resolution enhancement: how resolution is extended in practice via techniques such as source-mask optimization and optical proximity correction. Feature-size reduction also means minimizing the overlay errors of these features, including those on the back side of the wafer, and having resolution-matching photoresists. Here precision metrology tools are also essential. Finally, I will delve into the resolution metric: the k_1-factor. While 193-nm immersion lithography can pattern the 76-nm-pitch logic metal lines in single shots, close to the k_1=0.25 resolution limit, we are currently working with k_1>0.35 in EUV lithography. I will discuss k_1-lowering technologies such as metal-oxide resists, new mask materials, and advanced computational lithographic techniques.

T6 | Magneto-Ionics for Energy-Efficient and Reconfigurable Nanonelectronics
4:40 PM – 6:00 PM
Continental Ballroom 1 – 5
Kai Liu, Professor and McDevitt Chain in Physics at Georgetown University

The energy efficiency in today's electronics has become a key bottleneck, leading to the coming end of the iconic Moore's law. To address such a grand challenge, many spin-based approaches are being keenly pursued, including the use of electric field to control magnetism, in contrast to the conventional charge current and the associated Joule heating effects. In this tutorial I will discuss magneto-ionics (MIs), an emerging frontier of spintronics. Solid state MIs represents atomic scale control of interfaces via ionic motion, either electrostatically or electrochemically. The MI handle has been used to manipulate a wide variety of magnetic functionalities, including magnetic anisotropy, ferromagnetism, ferrimagnetism, antiferromagnetism, superconductivity, exchange bias, Dzyaloshinskii-Moriya interaction, interlayer exchange coupling, and spin textures, etc. Various ionic species have been explored, such as hydrogen, nitrogen, lithium, and hydroxide, besides the traditional oxygen. Device performance metrics have also improved significantly over recent years, in terms of switching speed, endurance, and switching energy. These progresses are highly promising for future energy-efficient nanoelectronics: 1) MIs can be used to manipulate essentially all magnetic functionalities; 2) Extremely large effect sizes can be realized by MI means, as compared to conventional methods; 3) MIs has shown excellent energy efficiency, approaching sub-attoJoule level energy cost for switching; 4) MIs is compatible with 3-dimensional (3D) integration; 5) MIs can transform the all-important interfaces under external stimuli such as an electric field, thus enabling reconfigurable nanoelectronics and adding a whole new degree of freedom to spintronics. These

exciting developments with be discussed and compared with other spintronic approaches, together with current challenges and opportunities.

Short Courses

IEEE IEDM will offer two short courses with in-depth coverage of highly relevant topics from world experts. All short courses will be held on Sunday, December 8th.

Sunday, Dec. 8

SC1 | Technology Innovations Shaping the Roadmap in the Era of AI
9:00 AM – 6:00 PM, Continental Ballroom 1 – 5
Co-chairs**:** Sandy Liao, Director of R&D Pathfinding at TSMC and Anabela Veloso, imec

9:00 AM
SC1-1 | Sailing into the Future of the Semiconductor Industry, Lipen Yuan, Taiwan Semiconductor Manufacturing Company

The semiconductor industry is embarking on a major transformation as Artificial Intelligence (AI) permeates into every aspect of our lives through innovations in products and services. High Performance Computing (HPC) is at the forefront of this revolution, with advancements in processors, interconnects, storage, and re-shaping of data centers for AI workloads. Mobile devices are incorporating AI capabilities and evolving into personal assistants, aided by enhanced wireless connectivity. In the automotive sector, advancements in architecture such as Software-Defined Vehicle and Zonal control, as well as features like In-Vehicle Infotainment and Advanced Driver Assistance Systems (ADAS), are underpinning the development of greener, safer, and smarter vehicles. The Internet of Things (IoT) is transitioning to AIoT with built-in intelligence for more convenience and better user experience. Energy efficiency, memory bandwidth, enriched feature set and smaller form factor are common product requirements to be addressed by a portfolio of technologies in order to enable the system-level innovations that will in turn shape the future of the industry.

10:30 AM
SC1-2 | Into the Multidimensional World of Advance Logic Technology, Yu-Lin Chao, Intel Corporation

The ubiquity and ever demanding computation of electronics in personal devices to mega data centers, coinciding with the limit of raw silicon scaling, has led to the advent of multidimensional logic technology. On transistor level, the industry has moved from planar FET to FinFET, and now gate-all-around (GAA) transistors, whereas low-dimensional materials have been intensively studied for future 3-D integration. For backend interconnect, introduction of backside power delivery networks (PDN) and relentless design technology co-optimization (DTCO) efforts enable continuing area scaling. The diverging scaling factors of various intellectual property (IP) and numerous system level applications may be answered by heterogeneous integration at package level. In this talk, physics and technology enablers associated with these geometrical changes will be discussed. Other aspects of technology consideration, from local layout effect (LLE), variation, reliability, to passive circuit components, will also be highlighted to provide a multidimensional view of this paradigm shift.

12:45 PM

SC1-3 | Evolution of Memory Technologies for Advanced Nodes via the third Dimension, Jeonghoon Oh, Samsung Electronics

The world is rapidly changing to the AI era. It has been so far, but the AI era is demanding more and more density and speed in memory. However, the current memory process is reaching its limit. DRAM is nearing the lateral shrink limit in the scheme referred to as BCAT(Buried Channel Array Transistor), and VNAND flash memory is nearing the limit in forming the channel hole narrower and deeper. Now memory is preparing to evolve into another level, 3rd dimension. Based on the recent development of wafer to wafer(WF-to-WF) bonding technology, we are developing Integration technology that fairly attaches Array cells and Logic circuits as separate Wafers. In particular, DRAM is designing a new cell array scheme based on this technology. In the near future, we will face DRAM that utilizes VCT(Vertical Channel Transistor) or GAA(Gate All Around) transistor as cell array transistor. This short course briefly introduces not only VCT and GAA, but also devices that have been studied as cell array candidates since then. Meanwhile, WF-to-WF bonding technology has also given freedom to transistors in the Memory periphery circuit area. By eliminating the constraints caused by doing the same with the cell process, it can be redesigned as a process to fully boost the transistor characteristics. Logic translator's various technologies and device forms will be the future, and this short course will also introduce these technologies.

2:00 PM

SC1-4 | The System Revolution enabled by 2.5D and 3D Technologies, Muhannad Bakir, Georgia Institute of Technology

In recent years, the field of advanced packaging has taken center stage as the semiconductor industry pursues ever more energy efficient, high-performance, and low-cost electronic systems. While the field of advanced packaging is undergoing revolutionary technology advances today, there is little doubt that advanced packaging in the new era of Moore’s Law will offer extreme levels of die integration/bonding and begin to blur the boundary between on- and off-chip connectivity due to ever denser physical I/O interfaces/bonds. First, we present the motivations to chiplet based architectures and design considerations. Next, we present a survey of recent advanced packaging technologies covering 2.5D and 3D technologies. Further, emerging HI technologies based on glass-core packaging and their motivation will also be discussed. Thermal and power delivery considerations for emerging packaging technologies will also be presented.

3:30 PM

SC1-5 | Advanced Metrology for Next Generations of Stacked Devices/Systems: Challenges and Opportunities, Etienne de Poortere, ASML

As device and system architectures become more complex and venture into the third dimension, metrology tools need corresponding improvements along the dual axes of resolution and probing depth. In logic applications, the stacked-FET or complementary FET (CFET), currently under development as a next-generation device enabling further scaling of the transistor density, requires processes capable of handling aspect ratios as high as 30:1 in geometries with lateral dimensions smaller than 20nm. In order to

create a manufacturable device, the full 3D profile of features in these geometries needs to be characterized, and, ideally, correlated to performance and yield metrics. In memory applications, 3D DRAM, which is being explored as a successor to current 2D DRAM technologies, requires both vertical and lateral etches through hundreds of superlattice layers, resulting in an unparalleled level of processing complexity that cannot be achieved without improved metrology. Advanced nodes will also include fine- or intermediate-pitch interconnects on the wafer backside - e.g. for backside power distribution. In this process, wafers are flipped and attached to a carrier wafer, resulting in distortions that need to be measured densely, and compensated for, during backside patterning. Finally, in advanced packaging, hybrid bonding provides a new and challenging use case for high-resolution defect metrology at the buried interface. In this short course, we will review how current and future metrology techniques based on, e.g., optical, electron, X-ray, or acoustic beams, attempt to address those needs, and continue to support manufacturable processes into the 3D era.

4:45 PM
SC1-6 | Multiscale Thermal Challenges and Modelling Frameworks for Advanced Device Technologies and Systems, Bjorn Vermeersch, imec

Thermal management and modelling of electronic systems are challenging yet fascinating multi-disciplinary fields at the forefront of keeping the power wall at bay. As technologies continue to scale down, power density tends to rise, rendering device self-heating a perpetual concern. Backside power delivery schemes (BS-PDN) with extreme wafer thinning or full removal of the silicon substrate and 3D device stacking further amplify thermal challenges.
In this Short Course, we first cover some heat diffusion fundamentals that reveal interplays across orders of magnitudes of length scales. Counterintuitively, most heating inside a typical device is caused by other parts of the circuit, and the vast majority of temperature rise inside a transistor channel can be induced by passive system layers far away from the active die. At the same time, hotspots do remain sensitive to the topology and thermal properties of their immediate surroundings. These complex interactions illustrate a growing need for holistic simulation approaches that form the focus of the remainder of the Course. We discuss state of the art developments towards thermal modelling frameworks with truly multiscale awareness stretching from nanoscale transport inside individual logic cells to cm-range cross-heating between different parts of packaged systems-on-a-chip (SOCs). Concrete case studies will showcase the thermal impacts of technology scaling from nanosheet to CFET, transistor contact schemes and BS-PDN scenarios, and the strong non-uniformity of circuit powers.
Jointly, these methodologies bring thermal awareness into the power-performance-area-cost (PPAC) assessment cycle and enable system/technology co-optimisation (STCO) workflows that can help detect and possibly mitigate self-heating issues already during the design phase.

SC2 | AI Systems and the Next Leap Forward
9:00 AM – 6:00 PM, Continental Ballroom 6 – 9
Co-chairs: Sandy Liao, Director of R&D Pathfinding at TSMC and Andy Wei, Intel

9:00 AM
SC2-1 | Evolution of AI Hardware: Past, Present and Future, Anand Joshi, TechInsights

The AI semiconductor market emerged in 2016 when Nvidia announced the first accelerator products. The AI algorithms and applications have evolved since. The neural network architecture has gone through major changes with MLPs being replaced by CNNs, which are now being replaced by transformer-based models. Multi-modal applications have emerged that combine sensor data, pictures, video, text, and promise to open up amazing use cases. The gap between the performance needs for neural networks and what semiconductors can offer is wider than ever. Start-ups, cloud providers, hyperscalers, and semiconductor companies have introduced their products targeting the AI acceleration market.
This talk will discuss the evolution of AI in its latest incarnation and how the semiconductor industry has responded. We'll analyze the evolving nature of the neural networks and how that maps to hardware acceleration needs. We'll look at the popular use cases, available acceleration solutions and why some work while others don't. The talk will discuss use cases and trends driving the needs today, and the way forward. The talk will also include an analysis of the current market landscape and how it might look in the future.

10:30 AM
SC2-1 | AI Accelerator Hardware and Research Directions, Brucek Khailany, NVIDIA
Artificial Intelligence (AI) and Machine Learning (ML) has transformed many aspects of hardware systems over the last decade. In the last few years, Generative AI (GenAI) and Large Language Models (LLMs) have enabled new AI applications and captured the imagination of users across multiple industries. The high compute demands and real-time requirements of many GenAI-based applications requires innovations across the hardware stack, including devices, circuits, packaging, architecture, software, and datacenter. In this talk, we will first provide an overview of how GPUs accelerate the training and inference of these AI models, using LLMs as a driving example. We will also highlight recent work from NVIDIA Research on energy-efficient LLM inference, including optimized accelerator micro-architectures and software/hardware co-design for low-precision quantization. Finally, we will describe challenges and open research problems for continuing to scale AI performance with future VLSI technology.

12:45 PM
SC2-3 | Memory Requirements and Solutions for AI Accelerators and HPC, Emanuele Confalonieri, Micron

Memory systems are pivotal to High-Performance Computing (HPC) and Artificial Intelligence (AI) and are quickly evolving. This course will navigate the complexities of memory systems and envision the future of HPC/AI technologies by exploring a range of topics, starting with an overview of HPC/AI applications and benchmarks, and their influence on system performance requirements such as memory bandwidth and latency. The course will further look at the growing demands for memory capacity driven by parallel computing and networking needs, as well as the increasing necessity for memory reliability. A review of current memory systems like DDR5 and HBM will provide a nuanced understanding of today's HPC/AI memory infrastructure. The session will culminate with a forward-looking discussion on the next generation of memory solutions including CXL and NMP.
- ♣ HPC/AI: Applications & Benchmarks
- ♣ System Performance Needs
- ♣ Memory Capacity Needs
- ♣ Memory Reliability Needs
- ♣ Memory Systems for HPC/AI – Today
- ♣ Memory Systems for HPC/AI – Tomorrow?

2:00 PM
SC2-4 | 3DIC STCO for AI Systems, Victor Moroz, Synopsys

AI system design is taking the industry by storm. To satisfy requirements of the AI systems, it is necessary to go beyond limitations of 2D SoC's into multi-chiplet 3DIC systems that provide huge benefits in terms of logic-to-memory connection bandwidth, power consumption, and manufacturing cost. However, there are a number of new challenges that have to be addressed to make 3DIC solutions successful. First, we look at the bigger picture of diverse STCO factors that have to be resolved, and then focus on the interplay of four effects that play a key role in 3DIC designs: thermal, power, timing, and stress, and show their interplay. Careful analysis and balance of all four major factors are necessary to meet the PPA (Power-Performance-Area) spec. To pull off a successful 3DIC system, it is necessary to go beyond traditional PPA optimization, and consider CtE (Cost, cycle time, and Environmental impact). We provide an example of PPACtE gains for transition from 2D SoC to a 3DIC AI system.

3:30 PM
SC2-5 | Developing Modern Scalable 3DIC Systems and Next Generation EDA, Vivek Rajan, Sr Principal Engineer at Intel Corporation

Rapidly emerging new workloads & disruptive architectures have accentuated the usage of Advanced Packaging and 3DIC Technology. 2D Scaling of Moore's law and ASIC design Methodology has pushed the boundaries of Electronic Design Automation (EDA) in the last 40 years. The next few decades are going to be propelled by System Technology Co-optimization (STCO), where EDA scales to multi-physics based early analysis, construction, and co-optimization across boundaries of Silicon, Package, Board and Systems. In this course, we deep-dive on the key topics around: a) technology, b) future of EDA solutions and its roadmap, and c) design-workflows of build scalable systems.

4:45 PM
SC2-6 | Leveraging AI to Revolutionize Semiconductor Manufacturing, Brett Schroeder, Sr Dir AIx Products at Applied Materials

In the rapidly evolving field of semiconductor manufacturing, the integration of artificial intelligence (AI) has become pivotal in driving innovation and efficiency. The semiconductor industry is at an inflection point where the complexity of semiconductor process technology has become so extreme that we can no longer make progress based on human insights alone. This complexity spans everything from atomic-scale materials, to devices, to wafers, to process chambers and all the way up to the entire fab. This course will explore the transformative potential of using AI to design and optimize the very systems and materials that are instrumental to the manufacturing of modern semiconductor devices. Real world case-studies will be used to demonstrate how AI can assist in the development of new materials, design of new process equipment, optimize process recipes, be embedded in digital twins, improve defect detection and more. By leveraging AI to build AI, we are not only redefining the boundaries of semiconductor manufacturing technology but also paving the way for the next generation of intelligent devices.

Welcome and Awards Presentations

Monday, Dec. 9
1 | Keynote
9:00 AM – 12:00 PM, Grand Ballroom B
Elif Balkas, Wolfspeed, Mark Fuselier, AMD, Jan Hoentschel, GLOBALFOUNDRIES, Yuh-Jier Mii, TSMC, Kirsten Moselund, Paul Scherrer Institute (PSI) / EPFL

Welcome and awards.

9:00 AM
1-0 | IEDM, IEEE and EDS Awards

9:45 AM
1-1 | Semiconductor Industry Outlook and New Technology Frontiers, Yuh-Jier Mii, TSMC

The semiconductor industry is a dynamic landscape of innovation, where new materials, advanced processing techniques, and cutting-edge design converge to shape the future of technology. Powered by the principle of technology scaling, this field continues to push boundaries, enabling transformative applications in AI, HPC, 5G/6G, autonomous driving, IoT, and more. As we progress through time, scaling evolves, unlocking new levels of chip efficiency and performance. The horizon shines bright with the promise of breakthroughs in EUV lithography, new device architectures like CFETs, novel low-dimensional channel materials, and the strategic synergy of DTCO, paving the way for exciting new technology eras. Additionally, advanced packaging techniques enhance system-level performance, blending computational power to surpass current limitations. The growth in specialty technology segments such as RF, non-volatile memory, power management, CMOS image sensors, and Si photonics expands the range of innovative devices. This keynote paper will explore the latest advancements and emerging trends in the semiconductor industry, offering insights into how these cutting-edge frontiers will drive smart technology integration and create a brighter future for society.

10:30 AM
1-2 | Advancing AI with Energy-Efficient Architectures: Innovations in Fab Process, Packaging, and System Integration, Mark Fuselier, AMD

Energy-efficient AI architectures have become paramount for continued scaling of AI performance, necessitating innovative approaches that reduce energy per operation while improving performance. Prioritizing performance per Watt is essential for advancing AI, where energy efficiency translates into larger deployments, reduced cooling requirements, and faster, more efficient model training and inference generation. This level of optimization demands that the industry push the limits of fab process technology, advanced packaging, system interconnect, and thermal solutions. More performant accelerators intrinsically improve datacenter-level efficiency with fewer nodes for a given performance level, reducing networking and system overhead. Leveraging new fab process optimizations, compute and memory chip-lets enables delivery of more performance on a single package. Advanced packaging techniques integrate these components, enabling higher interconnect density, improved thermal management, and better overall performance. These innovations collectively address the growing needs of AI and high-

performance computing, promising substantial improvements in energy efficiency, scalability, and integration.

11:15 AM
1-3 | Revolutionizing Power Electronics with Silicon Carbide to Pioneer Sustainable Solutions, Elif Balkas, Wolfspeed

The power semiconductor industry is driven by the increasing demand for efficient, clean and sustainable energy solutions which increased the attention on advanced materials. Among these, silicon carbide (SiC) has emerged as a game-changer providing such benefits over traditional silicon-based devices. SiC offers the combination of unique properties, such as high thermal conductivity, high breakdown electric field and a large bandgap making it ideal for high-power and high-frequency applications with greater efficiencies. In this keynote, we will explore SiC's impact across various applications, from electric vehicles and renewable energy systems to industrial power supplies to highlight its pivotal role in revolutionizing power electronics. Commercial adoption of SiC technology requires continuous attention to materials defects, device reliability and related packaging technologies. In this keynote, we aim to provide researchers and professionals practical knowledge on how SiC can bring highly efficient and dependable solutions to the power semiconductor industry

2024 Roger A. Haken Best Student Paper Award
Awarded to Shuhan Liu
For the paper entitled, “Edge Continual Training and Inference with RRAM-Gain Cell Memory Integrated on Si CMOS”

2024 IEEE/EDS Fellows
**This is a complete listing of the 2023 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2023 IEDM*

Massood Zandi Atashbar - for contributions to flexible hybrid electronics
Joseph Bardin - for contributions to cryogenic microwave circuits
Premjeet Chahal - for contributions to additive manufacturing and materials characterization
Ke-horng Chen - for contributions to power management integrated circuits and system design
Srabanti Chowdhury - for contributions to wide bandgap semiconductor devices and technology
Dirk Englund - for contributions to semiconductor quantum photonics and machine learning
Oliver Faynot - for leadership in CMOS technology development
Aaron Franklin -for contributions to transistor scaling and carbon nanotubes applications in electronics
Sergiu Goma - for contributions to hardware implementation of image processing for color cameras in mobile phones
Thomas Hall - for leadership in engineering technology education
Francesca Iacopi - for contributions to integration strategies of nanomaterials in silicon technologies
Debdeep Jena - for contributions to distributed polarization doping in the III-V semiconductor family
Mario Lanza - for contributions to nanoelectronics metrology of ultra-scaled materials and devices
Di Liang - for contributions to photonic integration in optical communication, computing, and volume production
Marko Loncar - for contributions to thin film lithium nanophotonics
Ionut Radu - for contributions to silicon-on-insulator materials for semiconductor devices

Li Ran - for contributions to the modeling of power electronic devices
Michael Ropp - for contributions to distributed energy resources integration in power systems
Atif Shamim - for contributions in the field of antenna-on-chip and antenna-in-package
Volker Sorger - for contributions to the optoelectronic devices and photonicelectronic ASICs
Vladimir Stojanovic - for contributions to electronic-photonic design and system-onchip integration
Yukiharu Uraoka - for contributions to reliability evaluation technology for thin film devices
Alberto Valdes-garcia - for contributions to millimeter-wave circuits and systems for communications
Barry Bing-ruey Wu - for contributions to enhancement and commercialization of InPbased ultra-high-speed DHBT IC technology
John Yeow - for contributions to the understanding and applications of nanostructures and nanocomposites
Shimeng Yu - for contributions to non-volatile memories and in-memory computing
Jim Zheng - for contributions to energy storage technologies

Technical Sessions

10 | EDT | Novel Platforms for Computing
1:30 PM – 4:30 PM, Imperial B
Co-chairs: David Michalak, TNO and Maud Vinet, CEO at Quobly

This session includes 6 papers in new areas of computing and thermalization. The 2 first papers focus on carbon nanotube devices. The first paper, which was chosen as an IEDM EDT Highlight, is from Yi-Fan Liu from the Key Laboratory at Peking University and presents a record transconductance of 3.7 mS/um. The second paper, by Shengman Li from Stanford University, presents the iso-performance of dense arrays of carbon nanotube in nFET and pFET configurations. The third paper by Junrui Lyu from Stanford University demonstrates the 3D integration of diamond-based thermal scaffolding for enhanced chip cooling. The last three papers focus on use of FD-SOI for quantum computing applications. Specifically, the fourth paper by Fabio Bersano from EPFL presents a thorough study of three different micromagnet geometries onto an FD-SOI spin qubit platform. The fifth paper by Hiroshi Oka from the National Institute of Advanced Industrial Science and Technology (AIST) investigates the long-period instability of silicon SOI fin-type quantum dots. The last paper by Bruna Cardoso-Paz from Quobly presents recent advances on FD-SOI platform including electron and hole based spin qubit co-integrated with control electronics.

1:30 PM
10-0 | Welcome

1:35 PM – 2:00 PM
10-1 | High-Performance Aligned Carbon Nanotube FETs with Record Transconductance of 3.7mS/µm, Yifan Liu, Peking university|Zipeng Pan, Peking university|Sujuan Ding, Zhejiang Univerity, Zhejiang university|Weili Li, University of Electronic Science and Technology of China|yanning zhang, University of Electronic Science and Technology of China|yumeng ze, Peking university|chuanhong Jin, Zhejiang Univerity|Li Ding, Peking university|Lian-Mao Peng, Peking university|Zhiyong Zhang, Peking university

High-performance field-effect transistors (FETs) are fabricated based on high-density aligned carbon nanotube (A-CNT) arrays with low interface state density (D_{it}) of 8.1×10^{11} cm^{-2}/eV mainly through improving the quality of gate stack. The champion A-CNT FET with gate length (L_G) of 100 nm exhibits a saturated on-state current (I_{on}) of 2.45 mA/μm, a peak transconductance (g_m) of 3.7 mS/μm, and a g_m/I_{on} ratio >1.5, which sets a record for ultrathin channel transistors and even exceeds the maximum g_m of Si planar FETs for the first time. The typical FET with L_G of 50 nm exhibits an extrinsic cut-off frequency of 302 GHz, far surpassing that of Si MOSFETs with the similar L_G. There is still huge room for improvement in device performance through further optimization of the gate stack in A-CNT FETs.

2:00 PM

10-2 | Iso-performance N-type and P-type MOSFETs on densely aligned CNT array enabled by self-aligned extension doping with barrier booster, Shengman Li, Stanford University, Stanford University|Donglai Zhong, Taiwan Semiconductor Manufacturing Company Limited, San Jose, USA|Carlo Gilardi, Taiwan Semiconductor Manufacturing Company Limited, San Jose, USA|Nathaniel Safron, Taiwan Semiconductor Manufacturing Company Limited, San Jose, USA|Tzu-Ang Chao, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Gilad Zeevi, Stanford University|Samantha Rijs, Stanford University|Andrew Bechdolt, Stanford University|Matthias Passlack, Taiwan Semiconductor Manufacturing Company Limited, San Jose, USA|Gregory Pitner, Taiwan Semiconductor Manufacturing Company Limited, San Jose, USA|Iuliana Radu, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|H.-S. Philip Wong, Stanford University, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Subhasish Mitra, Stanford University

In this work, we achieve $I_D$greater than 300μA/μm at +/-1V V_{DS} (iso-performance) for bothN-type and P-type MOSFETs with 100nm gate length (L_G) ondensely aligned CNT array by self-aligned extension doping witha barrier booster.We also present the firstexperimental validation of tunable doping strength, mobility lossminimization, and leakage reduction capabilities of the barrierbooster method, studied for top-gate CNT N-type MOSFET in thispaper.Using this method, we achieve the best performance to datefor N-type MOSFET on densely aligned CNT array, withI_D>200μA/μm and Imax/Imin exceeding 10^4 simultaneously at 1VV_{DS} and 500nm L_G.

2:25 PM

10-3 | Diamond 3D Thermal Scaffolding for Ultra-Dense 3D integrated Circuits, Junrui Lyu, Stanford University|Mohamadali Malakoutian, Stanford University|Dennis Rich, Stanford University|Anna Kasperovich, Stanford University|Rohith Soman, Stanford University|Janelle Mabrey, Stanford University|Jeongkyu Kim, Stanford University|Kelly Woo, Stanford University|Zhengliang Bian, Stanford University|Subhasish Mitra, Stanford University|Srabanti Chowdhury, Stanford University

For the first time, we fabricated 3D thermal scaffolding, a cooling technique targeting ultra-dense 3D ICs (e.g., <100 nm pitch 3D connections). Our fabricated structures incorporate the first BEOL-compatible polycrystalline diamond thermal vias to form thermal pathways to the heatsink. 3D thermal scaffolding was characterized using a 3D thermal platform with on-chip heaters emulating hotspots in ultra-dense 3D ICs. We achieve >10× reduction in temperature rise across a wide range of heater sizes. Calibrated 3D thermal simulations in COMSOL show that 3D thermal scaffolding enables 15 ultra-dense 3D stacked AI accelerators (>1.3 kW/cm^2 overall) with peak temperature below 125℃.

3:15 PM

10-4 | Integration of Co Nanomagnets for Localized EDSR in Scalable FDSOI Spin Qubit Architectures, Fabio Bersano, EPFL|Michele Aldeghi, IBM|Niccolò Martinolli, EPFL|Victor Boureau, EPFL|Rolf Allenspach, IBM|Gian Salis, IBM|Adrian Ionescu, EPFL

This study validates the integration of thin cobalt nanomagnets in a FEOL compatible process for EDSR manipulation in Si spin qubits. We designed, fabricated and electrically characterized three compact spin qubit architectures with Co nanomagnets on Fully Depleted Silicon-on-Insulator. The gate-first integration is investigated using x-ray spectroscopy and diffraction, and high-low frequency capacitive characterization to explore key process integration parameters. Electron holography measurements confirmed the remanent magnetization of horseshoe nanomagnets as most suited for low field operation, in agreement with micromagnetic simulations. These findings demonstrate the feasibility of compact Co FEOL integration in nanowires, FinFETs, and planar spin qubit architectures.

3:40 PM

10-5 | Origin of Long-period Electrical Instability in Silicon Fin-type Quantum Dots, Hiroshi Oka, National Institute of Advanced Industrial Science and Technology (AIST)|Hidehiro Asai, National Institute of Advanced Industrial Science and Technology (AIST)|Kimihiko Kato, National Institute of Advanced Industrial Science and Technology (AIST)|Takumi Inaba, National Institute of Advanced Industrial Science and Technology (AIST)|Shunsuke Shitakata, National Institute of Advanced Industrial Science and Technology (AIST)|Shota Iizuka, National Institute of Advanced Industrial Science and Technology (AIST)|Yusuke Chiashi, National Institute of Advanced Industrial Science and Technology (AIST)|Yuika Kobayashi, National Institute of Advanced Industrial Science and Technology (AIST)|Hitoshi Yui, National Institute of Advanced Industrial Science and Technology (AIST)|Shoko Nagano, National Institute of Advanced Industrial Science and Technology (AIST)|Shigenori Murakami, National Institute of Advanced Industrial Science and Technology (AIST)|Yoshihisa Iba, National Institute of Advanced Industrial Science and Technology (AIST)|Minoru Ogura, National Institute of Advanced Industrial Science and Technology (AIST)|Takashi Nakayama, National Institute of Advanced Industrial Science and Technology (AIST)|Hanpei Koike, National Institute of Advanced Industrial Science and Technology (AIST)|Hiroshi Fuketa, National Institute of Advanced Industrial Science and Technology (AIST)|Satoshi Moriyama, Tokyo Denki University (TDU)|Takahiro Mori, National Institute of Advanced Industrial Science and Technology (AIST)

The long-period electrical instability of Si fin-type quantum dots (QDs) was investigated. This study focuses on the long-period electrical instability, which is much longer than the coherence time of Si spin qubits, but it becomes a severe problem for future practical operations including bias calibration procedure. We found long-period RTN occurs when the $E_F$is aligned to the conduction band minimum that possesses the band-edge states. We identified such long-period RTN is generated at the MOS interface around the top of the fin-type QDs, indicating the interface quality at the fin-top is key for stable operation of Si quantum computers.

4:05 PM

10-6 | FDSOI platform for quantum computing, Bruna Paz, Quobly|Giselle Elbaz, Quobly|Mathilde Ouvrier-Buffet, CNRS|Mikaël Cassé, CEA-Leti|Flavio Bergamaschi, CEA-Leti|Jean-Baptiste Filippini, CNRS|Javier Suarez Berru, CNRS|Pierre-Louis Julliard, Quobly|Biel Martinez I Diaz, CEA-Leti|Bernhard Klemt, CNRS|Victor El-Homsy, CNRS|Victor Champain, CEA-IRIG|Victor Millory, CEA-IRIG|Renan Lethiecq,

Quobly|Valentin Labracherie, CEA-Leti|Gregoire Roussely, CEA-Leti|Benoit Bertrand, CEA-Leti|Heimanu Niebojewski, CEA-Leti|Franck Badets, CEA-Leti|Matias Urdampilleta, CNRS|Silvano De Franceschi, CEA-IRIG|Tristan Meunier, Quobly|Maud Vinet, Quobly

Si-based qubits are considered the most promising experimental system for scaling quantum computing. For the first time, FDSOI CMOS technology is demonstrated as the platform to co-integrate hole and electron spin qubits with cryo-electronics. For cryo-control, we show voltage gain as high as 75dB for long devices, noise of $10^{-11}V^2{\cdot}\mu m^2/Hz$ and 1.29mV·μm threshold voltage variability. We propose a standard cell for two-qubit gates on commercial 22FDX® and show double quantum dot features. Finally, we demonstrate hole and electron qubits on the same FDSOI technology with a manipulation time below 1μs and coherence time of 40μs (Hahn echo), respectively.

3 | Focus Session | AI Memory: Technology and Architecture
1:30 PM – 4:30 PM, Grand Ballroom B
Co-chairs: Wei-Chih Chien, Project Department Manager at Macronix and Shimeng Yu, Georgia Tech

In this session on “AI Memory: Technology and Architecture,” we will explore the latest innovations at the intersection of memory technology and artificial intelligence. The presentations will cover diverse approaches, including the accelerator-in-memory architecture for large language model inference, and PCM-based analog in-memory computing. We will also delve into the prospects of integrating computation with flash memories, recent advances in processing-in-DRAM, and novel compute-with-memory techniques. Additionally, insights into on-device AI applications for AR/VR systems will be discussed, highlighting how these advancements are transforming the landscape of AI and memory integration. This session will provide a comprehensive overview of the cutting-edge technologies driving the future of memory-centric compute.

1:30 PM
3-0 | Welcome

1:35 PM
3-1 | AiMX: Accelerator-in Memory Based Accelerator for Cost-effective Large Language Model Inference (Invited), Haerang Choi, SK hynix|Guhyun Kim, SK hynix|Woojae Shin, SK hynix|Jongsoon Won, SK hynix|Changhyun Kim, SK hynix|Hyunha Joo, SK hynix|Byeongju An, SK hynix|Gyeongcheol Shin, SK hynix|Jeongbin Kim, SK hynix|Dayeon Yun, SK hynix|Jaehan Park, SK hynix|Yosub Song, SK hynix|Byeongsu Yang, SK hynix|Hyeongdeok Lee, SK hynix|Seungyeong Park, SK hynix|Wonjun Lee, SK hynix|Seonghun Kim, SK hynix|Yonghoon Park, SK hynix|Yousub Jung, SK hynix|Ilkon Kim, SK hynix|Gi-Ho Park, Sejong University|Euicheol Lim, SK Hynix

We presented an Accelerator-in-Memory (AiM) device and AiM-based LLM inference acceleration system. LLM inference can be divided into prompt phase and response phase. Considering the characteristics of LLM inference, we proposed a disaggregated inference system where the prompt phase is executed on high-throughput GPUs or NPUs, and the response phase is executed on AiM. Using AiM for single GEMV operations can ideally achieve up to 16 times the performance. The measured performance of the prototype AiM-based Accelerator is 1.7 times higher than that of a comparable GPU, and the expected performance at the highest data rate is 11.7 times higher.

2:00 PM

3-2 | Heterogeneous Embedded Neural Processing Units Utilizing PCM-based Analog in-Memory Computing (invited), Irem Boybat, IBM Research - Zurich|Thomas Boesch, STMicroelectronics|Mario Allegra, STMicroelectronics|Matteo Baldo, STMicroelectronics|Jacopo Bertolini-Agnoletto, STMicroelectronics|Geoffrey W. Burr, IBM Research - Almaden|Alessandro Buschini, STMicroelectronics|Alessandro Cabrini, University of Pavia|Emanuela Calvetti, STMicroelectronics|Carmine Cappetta, STMicroelectronics|Francesco Conti, University of Bologna|Elena Ferro, IBM Research - Zurich|Eleonora Franchi Scarselli, University of Bologna|Angelo Garofalo, ETH Zurich|Francesca Girardi, STMicroelectronics|Gamze Islamoglu, ETH Zurich|Vara Prasad Jonnalagadda, IBM Research - Zurich|Geethan Karunaratne, IBM Research - Zurich|Corey Lammie, IBM Research - Zurich|Manuel Le Gallo, IBM Research - Zurich|Chen Li, King's College London|Riccardo Massa, STMicroelectronics|Andrea Carlo Ornstein, STMicroelectronics|Hong Pang, ETH Zurich|Marco Pasotti, STMicroelectronics|Bipin Rajendran, King's College London|Andrea Redaelli, STMicroelectronics|Irem Sanli, IBM Research - Zurich|Wililam Andrew Simon, IBM Research - Zurich|Abhairaj Singh, IBM Research - Zurich|Surinder-Pal Singh, STMicroelectronics|Giulio Urlini, STMicroelectronics|Athanasios Vasilopoulos, IBM Research - Zurich|Riccardo Zurla, STMicroelectronics|Giuseppe Desoli, STMicroelectronics|Abu Sebastian, IBM Research - Zurich

We propose an embedded Neural Processing Unit (NPU) architecture for deep learning inference to address the stringent energy, area, and cost requirements of edge AI. This heterogeneous architecture integrates a variety of digital and analog accelerator nodesto cater to diverse operation types and precision requirements. To achieve high energy efficiency while maintaining substantial non-volatile on-chip weight capacity, we utilize Analog In-Memory Computing (AIMC) tiles based on Phase-Change Memory (PCM) for MatrixVector Multiplications (MVMs). Additionally, a digital data path and a programmable software cluster facilitate end-to-end inference across multiple precision levels. The NPU is projected to deliver competitive throughput for transformer Neural Networks (NNs), rivaling high-end System-on-Chips (SoCs) for mobile devices and edge accelerators fabricated at more advanced technology nodes.

2:25 PM

3-3 | Prospects of Computing in or Near Flash Memories (Invited), Hang-Ting Lue, Macronix International Co., Ltd.|Chun-Hsiung Hung, Macronix International Co., Ltd.|Keh-Chung Wang, Macronix International Co., Ltd.|Chih-Yuan Lu, Macronix International Co., Ltd.

This is an invited paper for Focus Session in IEDM 2024. The paper tile is "Prospects of Computing in or near Flash Memories". Two topics are introduced: 3D NOR high-bandwidth digital computing in memory (HB dCIM) for LLM inference accelerator; 3D NAND in-memory search accelerator for approximate nearest neighbor search in data retrieval.

3:15 PM

3-4 | Memory-Centric Computing: Recent Advances in Processing-in-DRAM (Invited), Onur Mutlu, ETH Zurich|Ataberk Olgun, ETH Zurich|Geraldo Oliveira Jr., ETH Zurich|Ismail Yuksel, ETH Zurich

Memory-centric computing aims to enable computation capability in and near all places where data is generated and stored. As such, it can greatly reduce the large negative performance and energy impact of data access and data movement, by 1) fundamentally avoiding data movement, 2) reducing data access

latency & energy, and 3) exploiting large parallelism of memory arrays. Many recent studies show that memory-centric computing can largely improve system performance & energy efficiency. Major industrial vendors and startup companies have recently introduced memory chips with sophisticated computation capabilities. Going forward, both hardware and software stack should be revisited and designed carefully to take advantage of memory-centric computing.This work describes several major recent advances inmemory-centric computing, specifically in Processing-in-DRAM, a paradigm where the operational characteristicsof a DRAM chip are exploited and enhanced to performcomputation on data stored in DRAM. Specifically, we describe 1) new techniques that slightly modify DRAM chips to enable both enhanced computation capability and easier programmability, 2) new experimental studies that demonstrate the functionally-complete bulk-bitwise computational capability of real commercial off-the-shelf DRAM chips, without any modifications to the DRAM chip or the interface, and 3) new DRAM designs that improve access granularity & efficiency,unleashing the true potential of Processing-in-DRAM.

3:40 PM
3-5 | Future of Memory: Massive, Diverse, Tightly Integrated with Compute – From Device to Software (Invited), Shuhan Liu1, Robert Radway1, Xinxin Wang1, Jimin Kwon2, Caroline Trippel1, Phil Levis1, Subhasish Mitra1, H.S. Philip Wong1
1Stanford University, 2UNIST

4:05 PM
3-6 | On-device AI and LLM approaches for AR /VR systems (Invited), Edith Beigne, Meta|Daniel Morris, Meta
Speakers: Huichu Liu

On-device AI and LLM approaches for AR /VR systems

8 | ODI | Advanced Optoelectronic Devices
1:30 PM – 4:30 PM, Continental 7 – 9
Co-chairs: Jamie Phillips, University of Deleware and Susanna Thon, John Hopkins University

This session chairs 6 papers describing advanced optoelectronic devices for photodetection and other photonic applications. The first paper by the University of Grenoble Alpes describes an integrated phase-modulating sensor combining interferometric phase measurement and liquid crystal-based phase modulation in a single device. The second paper from Sony demonstrates a two-layer pixel technology that reduces cathode capacitance in a single photon avalanche photodiode with reduced dead time. The third paper from KAIST describes a chip-based free-standing TiO2/Ti bolometer on a Ge-on-insulator platform operating out to 13 microns as a mid-IR spectrometer. The fourth paper from IBM Research and collaborators tested InP/InGaAs/InP photodetectors at temperatures from 5K-300K, demonstrating the first cryogenic measurements of scaled waveguide-coupled III-V photodetectors integrated onto SOI with improved performance variability. The fifth paper from USTC employed a novel effect, quantum-confined-traps-assisted carrier multiplication, to achieve high responsivity and detectivity in an alpha-GaOxNy/GaN-based photodetector. The final paper in the session from the National University of Singapore demonstrated a photonic convolutional accelerator capable of calculating parallel dot products using ferroelectric microring resonators with impacts in photonic computing.

1:30 PM

8-0 | Welcome

1:35 PM
8-1 | A 58x60 π/2-Resolved Integrated Phase Modulator And Sensor With Intra-Pixel Processing, Arnaud Verdant, CEA Leti|Pierre Joly, CEA Leti|Benoît Racine, CEA Leti|Olivier Haon, CEA Leti|Sébastien Martin, CEA Leti|Guillaume Moritz, CEA Leti

This paper presents an integrated device combining a Liquid Crystal (LC) cell with a 58×60 CMOS image sensor dedicated to Digital Optical Phase Conjugation (DOPC) applications. Each pixel performs a π/2-resolved phase measurement of the incoming light, and a reflective electrode biases the LC based on the retrieved phase, to induce a phase modulation leading to the focalization of the reflected light. An experiment using the component to compensate the phase of a defocused 780-nm beam, and focus it on a reference target beam, is presented. The integrated device produced is scalable, compact and offers intrinsic optical alignment.

2:00 PM
8-2 | A 2.1-ns Dead Time 5-μm Single Photon Avalanche Diode with 2-layer Transistor Pixel Technology, Jun Ogi, Sony Semiconductor Solutions Corporation|Shota Kitamura, Sony Semiconductor Solutions Corporation|Fumitaka Sugaya, Sony Semiconductor Solutions Corporation|Junki Suzuki, Sony Semiconductor Solutions Corporation|Aoi Magori, Sony Semiconductor Solutions Corporation|Tomonori Matsui, Sony Semiconductor Solutions Corporation|Kei Sumita, Sony Semiconductor Solutions Corporation|Yuki Ushiku, Sony Semiconductor Solutions Corporation|Koji Moriyama, Sony Semiconductor Manufacturing Corporation|Kenji Toshima, Sony Semiconductor Manufacturing Corporation|Tomohiro Namise, Sony Semiconductor Solutions Corporation|Hideki Ozawa, Sony Semiconductor Solutions Corporation|Yasunori Tsukuda, Sony Semiconductor Solutions Corporation|Yusuke Otake, Sony Semiconductor Solutions Corporation|Hiroki Hiyama, Sony Semiconductor Solutions Corporation|Shizunori Matsumoto, Sony Semiconductor Solutions Corporation|Atsushi Suzuki, Sony Semiconductor Solutions Corporation|Fumihiko Koga, Sony Semiconductor Solutions Corporation

A 2.1 ns dead time 5-μm-pitch single photon avalanche diode (SPAD) with 2-layer transistor pixel technology is reported. The dead time is 1/3 times smaller than conventional three-dimensional-stacked SPAD pixels because the 2-layer pixel technology reduces cathode capacitance. The other pixel characteristics is maintained comparable to the state-of-the-art SPAD pixels.

2:25 PM
8-3 | Highly-Sensitive Free-Standing Waveguide-Integrated Bolometer on Germanium-on-Insulator Platform for Mid-Infrared on-Chip Spectroscopy, Inki Kim, KAIST|Joonsup Shim, KAIST|Jinha Lim, KAIST|Jaeyong Jeong, KAIST|Bong Ho Kim, KAIST|SangHyeon Kim, KAIST

Mid-IR on-chip spectroscopy offers a promising alternative to bulky optical gas sensors but faces challenges due to short light paths impacting detection limits. We introduce a high-sensitivity, free-standing waveguide-integrated bolometer on a germanium-on-insulator platform. Utilizing an air trench for enhanced thermal isolation, it achieves a sensitivity of -1.789%/μW and low resistance noise at room temperature. By employing free-carrier absorption and Ti/TiO_2 materials within CMOS-compatible processes, our design supports a mid-IR on-chip spectrometer with a wide wavelength range up to 13 μm.

3:15 PM

8-4 | Ultra-Low Temperature Characterization of Fully-Integrated III-V Photodetectors for Quantum Networks, Simone Iadanza, Paul Scherrer Institute|Myriam Rihani, IBM Research|Cristina Martinez-Oliver, IBM Research|Markus Scherrer, Paul Scherrer Institute|Heinz Schmid, IBM Research|Vihar Georgiev, University of Glasgow|Kirsten Moselund, Paul Scherrer Institute

We present the first low temperature (5K-300K) characterization of scalable, waveguide-coupled III-V photodetectors integrated on silicon photonics platform. We also explore for the first time the excitation of traps in the heterojunction via both electrical and optical power. A reliability challenge is facet control in conventional Si <100> oriented wafers, so we also develop comparable photodetectors on SOI with <110> crystal orientation. This allows us to further scale the active region to ~λ^3/1550 maintaining responsivity ~40% down to 5K and improve performance variability by ~1000. This work shows the strong promise of this technology for future quantum optical links.

3:40 PM

8-5 | Quantum-confined-traps-assisted Carrier-multiplication-enabled Photodetector and Arrays for Smart Visualization and High-quality Imaging, Dongyang Luo, School of Microelectronics, University of Science and Technology of China, School of Microelectronics, University of Science and Technology of China|Yong Yan, School of Microelectronics, University of Science and Technology of China|Xin Liu, School of Microelectronics, University of Science and Technology of China|Huabin Yu, School of Microelectronics, University of Science and Technology of China|Yang Kang , School of Microelectronics, University of Science and Technology of China|Yuanmin Luo, School of Microelectronics, University of Science and Technology of China|Wei Chen, School of Microelectronics, University of Science and Technology of China|Zhixiang Gao, School of Microelectronics, University of Science and Technology of China|Haiding Sun, School of Microelectronics, University of Science and Technology of China

We proposed and verified the quantum-confined-traps-assisted carrier-multiplication effect to amplify photoresponsivity in photodetectors based on amorphous-gallium oxynitride/gallium nitride heterostrucutre. Remarkably, the responsivity of the device was increased by 10^4 times while maintaining the dark current at fA level. We further implentmented them in ultraviolet visualizaiton and real-time imaging systems.

4:05 PM

8-6 | Parallel In-memory Dot Product Engine Using Non-volatile Ferroelectric Microring Resonator Weight Band for High-throughput Parallel Photonic convolutional Accelerator, Yue Chen, National University of Singapore|Rui Shao, National University of Singapore|Gong Zhang, National University of Singapore|Leming Jiao, National University of Singapore|Xuanqi Chen, National University of Singapore|Kaizhen Han, National University of Singapore|Zijie Zheng, National University of Singapore|Zuopu Zhou, National University of Singapore|Chen Sun, National University of Singapore|Jishen Zhang, National University of Singapore|Qiwen Kong, National University of Singapore|Xiao Gong, National University of Singapore

For the first time, we experimentally demonstrated a parallel in-memory dot product engine using non-volatile phase modulators—ferroelectric microring resonators as weight bank. We presented non-volatile weight storage and multiply-accumulate operations using a 1×2 FE-MRR weight bank. Thanks to the periodic spectrum in FE-MRR, we further performed a proof-of-concept of parallel dot product across

three channels through WDM. Image convolution was demonstrated in multiple channels, demonstrating a high computation precision with a structural similarity index (SSIM) larger than 0.98 comparing to CPU-processed images. We further proposed a novel parallel photonic convolutional accelerator that promises significant improvements in scalability and computing throughput.

5 | NC | 3D Integration
1:30 PM – 4:55 PM, Continental 4
Co-chairs: Gina Adam, George Washington University and Seyoung Kim, POSTECH

This session covers neuromorphic devices and system-level implementations featuring novel 3D integration and stacking concepts. The first paper describes an analog accelerator based on 3D-NAND devices for high dimensional (492-bit) searching in big data domains. The second is a paper that experimentally demonstrates HfOx-based vertical resistive switching memory with multi-bit programmability for efficient matrix processing and image compression. The third paper demonstrates a monolithically integrated system with CMOS logic as a first layer, with 128kb RRAM as a second layer and IGZO/TeOx based CFET circuits as third layer for NoC applications. The fourth paper introduces a deep neural matrix equation solver using a 3D vertical ReRAM array, demonstrating high-precision compute-in-memory for scientific computing tasks with significantly better energy and area efficiency than traditional GPUs. The fifth paper experimentally demonstrates a $4F^2$ memcapacitor crossbar array using a TiN-Al2O3-Si3N4-SiO2-Si gate stack, with 4-bit multi-level operation, accurate vector-matrix multiplication, and potential for 3D stacking. The sixth paper in this session realizes a VO2-based random number generator and ReLU activation unit monolithically 3D-integrated on a 1Mb RRAM array chip to implement a fully memristive Bayesian neural network with significantly increased bandwidth and reduced hardware cost. The final paper demonstrates a monolithic 3D integrated chip by vertically stacking Si CMOS, HfO2-based RRAM array, Ta2O5-based binary RRAM and carbon nanotube-based CMOS for mixed-precision analog-digital compute-in-memory architecture.

1:30 PM
5-0 | Welcome

1:35 PM
5-1 | High Dimensional Analog Range In-3D-NAND Search Accelerator for Applications of Search in Few-Shot Learning Model and Retrieval in Retrieval Augmented Generation, Po Hao Tseng, Macronix International Co., Ltd.|Shao Yu Fang, Macronix International Co., Ltd.|Chi-Tse Huang, National Taiwan University|Hao-Wei Chiang, National Taiwan University|Feng-Ming Lee, Macronix International Co., Ltd.|Yu-Hsuan Lin, Macronix International Co., Ltd.|Jhe-Yi Liao, Macronix International Co., Ltd.|Yu-Yu Lin, Macronix International Co., Ltd.|An-Yeu Wu, National Taiwan University|Hsiang-Yun Cheng, Academia Sinica|Ming-Hsiu Lee, Macronix International Co., Ltd.|Kuang-Yeu Hsieh, Macronix International Co., Ltd.|Keh-Chung Wang, Macronix International Co., Ltd.|Chih-Yuan Lu, Macronix International Co., Ltd.

We developed a novel analog range in-memory searching technology (AR-IMS) using high dimensional serial-parallel array architecture in 3D-NAND flash chip for applications in few-shot learning (FSL) models and retrieval augmented generation (RAG). The proposed integrated system (Optimizing controller + AR-IMS accelerator) enable high performance analog computing for continuous-learning FSL AI systems. As compared to the CPU stand-alone system, the AR-IMS accelerator with CPU or GPU integration provided

high speed (57x to 258x), low power computing performance (70x to 158x) for RAG in large language model (LLM) generative process.

2:00 PM
5-2 | High-density multilevel 3D vertical resistive switching memory (VRRAM) for massively parallel in-memory computing, Davide Bridarolli, Politecnico di Milano|Carlo Zucchelli, Politecnico di Milano|Piergiulio Mannocci, Politecnico di Milano|Saverio Ricci, Politecnico di Milano|Matteo Farronato, Politecnico di Milano|Giacomo Pedretti, Hewlett Packard Enterprise|Zhong Sun, Peking University|Daniele Ielmini, Politecnico di Milano

In-memory computing (IMC) can overcome the memory bottleneck of data-intensive workloads. Scaling of IMC circuits is enabled by high-density crossbar arrays (CBAs) of 3D vertical resistive switching memory (VRRAM) in the back end of the line (BEOL). However, 3D-VRRAM capable of precise multilevel operation and accurate IMC has not been reported yet. This work demonstrates accurate IMC with multilevel 3D-VRRAM CBAs for matrix-vector multiplication and inverse/pseudoinverse matrix calculation for the first time. Energy-efficient IMC is demonstrated for real-life problems via experiments on multilevel 2D CBAs. These results support 3D-VRRAM for high-density, energy-efficient IMC in edge computing applications.

2:25 PM
5-3 | IGZO/TeOx Complementary Oxide Semiconductor based CFET for BEOL-compatible memory immersed logic, Ting Liu, Tsinghua University|Jianshi Tang, Tsinghua University|Yiwei Du, Tsinghua University|Huimin Yang, Tsinghua University|Yibei Zhang, Tsinghua University|Ziyi Liu, Tsinghua University|Zhixing Jiang, Tsinghua University|Ran An, Tsinghua University|Yue Xi, Tsinghua University|Yijun Li, Tsinghua University|Dong Wu, Tsinghua University|Bin Gao, Tsinghua University|He Qian, Tsinghua University|Huaqiang Wu, Tsinghua University

An IGZO/TeO_x OS-**C**FET is demonstrated with logic gates, implementing BEOL-compatible **m**emory-**i**mmersed **l**ogic using ultralow-leakage IGZO-NFET. **CMIL**, serving as registers, is monolithically 3D integratedwith Si CMOS logic and RRAM-CIM layers for an M3D-CMIL prototype. Compared to 2D counterparts, M3D-CMIL significantly reduces area, delay, and energy.

2:50 PM
5-4 | Demonstration of a Floating-point Deep Neural Matrix Equation Solver using 3D Vertical ReRAM with High Energy- and Area-Efficiency, Jiancong Li, huazhong university of science and technology|Shengguang Ren, huazhong university of science and technology|Yi Li, huazhong university of science and technology|Wenlong Peng, huazhong university of science and technology|Zhiwei Zhou, huazhong university of science and technology|Yibai Xue, huazhong university of science and technology|Yu Zhang, huazhong university of science and technology|Zhiwen Cao, huazhong university of science and technology|Jiayi Sun, huazhong university of science and technology|Yuhui He, huazhong university of science and technology|Xiangshui Miao, huazhong university of science and technology

In this work, we present a deep neural matrix equation solver using a 3D V-ReRAM with computing-in-memory (CIM) capabilities for the first time. The fabricated 3D V-ReRAM shows fJ-level switching energy and high integration density. This V-ReRAM-based neural solver is verified by solving a 1-D unsteady-state convection-diffusion equation with software-comparable precision (error $<10^{-15}$). The results show an energy efficiency of 11.5 TFLOPS/W and an area efficiency of 0.63TFLOPS/mm², indicating improvements

of 132× and 7.6×, respectively, compared to H100 GPU. This work paves the way for leveraging V-ReRAM with CIM features for high-precision neural scientific computing platforms beyond edge AI applications.

3:40 PM
5-5 | Vertically Stackable Memcapacitor Crossbar Array based on NAND Flash Array Structure, Junsu Yu, Seoul National University|Hwiho Hwang, Hanyang University|Hyungjin Kim, Hanyang University|Woo Young Choi, Seoul National University

In this work, a vertically stackable $4F^2$ memcapacitor crossbar array based on CTF is experimentally demonstrated with a TANOS gate stack. 4-bit multi-level operation of the fabricated 24×48 array is verified with more than 10 years of retention and no read/write disturbance. Also, VMM operations with an error of 0.227 % are validated, along with read operations using a sensing circuit. The capability of performing read/write operations with a vertically stacked 3-D structure is verified through TCAD simulations. A weight transfer procedure is also provided to enhance VMM accuracy in a scaled-down vertical structure, resulting in significantly suppressed VMM errors.

4:05 PM
5-6 | Monolithically 3D Integrated Memristive Bayesian Neural Network for Intelligent Motion Planning, Linbo Shan, Peking University|Lindong Wu, Peking University|Zongwei Wang, Peking University|Ruiqing Xie, Peking University|Chaoyi Ban, Peking University|Gaoqi Yang, Peking University|Qishen Wang, Peking University|Yuan Li, Beijing University of Technology|He Ma, Beijing University of Technology|Lin Bao, Peking University|Ling Liang, Peking University|Yuan Wang, Peking University|Yimao Cai, Peking University|Ru Huang, Peking University

This paper introduces a novel back-end-of-line (BEOL) compatible VO_2-based standard normal distribution random number generator (SD-RNG) unit and spiking neural ReLU activation (SNRA) unit. These are integrated monolithically in 3D on a 1M RRAM array chip using a 40 nm process, creating a fully memristive Bayesian neural network. This integration overcomes data transmission bandwidth bottlenecks and reduces hardware costs by 2.41×. Autonomous driving tasks show that the M3D-BNN chip matches software accuracy, improves uncertainty prediction by 2.47×, uses 19.9× less energy, and runs 2.1× faster than its 2D counterpart. This demonstrates the M3D-BNN chip's significant potential in intelligent applications.

4:30 PM
5-7 | Monolithic 3D Integration of Multi-layer CNT-CMOS/RRAM Macros for Mixed-Precision Analog-Digital Computing-in-Memory Architecture, Yibei Zhang1, Jianshi Tang2, Yijun Li2, Ningfei Gao3, Lei Gao3, Haitao Xu3,4, Ran An2, Huimin Yang2, Zhengwu Liu2, Chenglei Guo5, Weihai Bu5, Dong Wu2, Bin Gao2, He Qian2, Huaqiang Wu2, 1Tsinghua University, 2Tsinghua Univercity, 3Beijing Institute of Carbon-based Integrated Circuits, 4Institute of Carbon-based Thin Film Electronics, 5STIC

In this work, for the first time, we present M3D-MP4, a Monolithic 3Dintegration chip featuring Mixed-Precision analog-digital CIM architecturewith 4functional layers:the1stlayer of Si CMOS, the 2ndlayer of 128k-bit HfO_2-based analog RRAM array for A-CIM, the 3rdand 4thlayers of Ta_2O_5-based binary RRAM and carbon nanotube (CNT) CMOS for vertically stacked pseudo-digital CIM (PD-CIM)as well as cache and router arrays. System-level benchmarks show that the M3D-MP4architecture could achieve 118.74× speed-up compared to its 2D counterpart and 16.92× lower energy than GPU.

6 | MT | DRAM with Oxide Semiconductor Channel
1:30 PM – 4:55 PM, Continental 5
Co-chairs: Seiyon Kim, SK Hynix and Hongmei Wang, Micron

DRAM utilizing oxide semiconductor (OS) channel cell transistor has been an interesting topic since OS channel provides promising device properties such as high current and low leakage, as well as great scalability and future extendability for 3-dimensional DRAM structures. In this session, seven papers focusing on the recent progress in DRAM with OS channel will be presented. In the first paper, Kioxia demonstrates the 4F2 gate-all-around OS channel transistor integrated IGZO vertical channel transistor on top of a high aspect ratio capacitor. Second paper from Semiconductor Energy Laboratory prototyped a V-FET that includes In2O3 as a channel material and has a gate electrode with a pulled-up structure. In the third paper, Key Laboratory of Fabrication Technologies for Integrated Circuits demonstrates the 4-layer stacked P-CAA IGZO FETs for 1T1C 3D DRAM with the one-step fabrication process. Next paper from Shanghai Jiao Tong University shows transient characteristics during the multi-bit writing operation of the 2T0C DRAM by ALD IGZO transistors with fast I-V measurement. Next three papers are on a gain cell using monolithically integrated OS NFET/PFET. Tsinghua University demonstrates the fully integrated TeOx/IGZO complementary OS-based 2T0C DRAM macro with CFET peripheral circuits. The paper from Stanford University demonstrates N-P Oxide OS using IGZO as a NFET and SnO as a PFET. The last paper of the session, researchers from Key Lab of Fabrication Technologies for Integrated Circuits demonstrates 4F2 vertical-channel IGZO multi-bit dual-gate (DG) 2T0C DRAM with self-aligned single step process.

1:30 PM
6-0 | Welcome

1:35 PM
6-1 | Oxide-semiconductor Channel Transistor DRAM (OCTRAM) with 4F2 Architecture, Shosuke Fujii, Kioxia Corporation|Tseng Fu Lu, Nanya Technology Corporation|Keiji Ikeda, Kioxia Corporation|Szu Yao Chang, Nanya Technology Corporation|Kei Sakamoto, Kioxia Corporation|Lu Wei Chung, Nanya Technology Corporation|Mutsumi Okajima, Kioxia Corporation|Jhen-Yu Tsai, Nanya Technology Corporation|Toshifumi Kuroda, Kioxia Corporation|Chung Peng Hao, Nanya Technology Corporation|Shinji Miyano, Kioxia Corporation|Mei Chuan Peng, Nanya Technology Corporation|Kimitoshi Okano, Kioxia Corporation|Martin Sillero, Nanya Technology Corporation|Akihiro Kajita, Kioxia Corporation|Chung Lin Huang, Nanya Technology Corporation|Takeshi Fujimaki, Kioxia Corporation|Chiang-Lin Shih, Nanya Technology Corporation

We demonstrated the world's first $4F^2$ gate-all-around Oxide-semiconductor Channel Transistor DRAM (OCTRAM). The InGaZnO VCT achieved Ion=15uA/cell (Vg=2V) and Ioff=1aA/cell (Vg=-1V). A 275Mbit OCTRAM array was fabricated with WL 54nm/BL 63nm pitches and showed successful operation in the designed voltage range, making it a breakthrough technology for future $4F^2$ DRAM.

2:00 PM

6-2 | Vertical-channel Crystalline in2o3 FET with a Pulled-up Gate, Monolithically Stack on Si CMOS, Achieving 112.2 μA/μm On-state Current, Shoki Miyata, Semiconductor Energy Laboratory Co., Ltd.|Kazuma Furutani, Semiconductor Energy Laboratory Co., Ltd.|Yusuke Komura, Semiconductor Energy Laboratory Co., Ltd.|Yoshinori Ando, Semiconductor Energy Laboratory Co., Ltd.|Satoru Saito, Semiconductor Energy Laboratory Co., Ltd.|Takeya Hirose, Semiconductor Energy Laboratory Co., Ltd.|Fumito Isaka, Semiconductor Energy Laboratory Co., Ltd.|Hidekazu Miyairi, Semiconductor Energy Laboratory Co., Ltd.|Hiroki Komagata, Semiconductor Energy Laboratory Co., Ltd.|Haruki Katagiri, Semiconductor Energy Laboratory Co., Ltd.|Takanori Matsuzaki, Semiconductor Energy Laboratory Co., Ltd.|Tatsuya Onuki, Semiconductor Energy Laboratory Co., Ltd.|Shunpei Yamazaki, Semiconductor Energy Laboratory Co., Ltd.

The prototyped Vertical-channel FET (VFET) reduces gate resistance and capacitance by pulling up its gate electrode, and exhibits high on-state current characteristics by employing a crystalline indium oxide as its channel material. A 1T1C DRAM including the VFET monolithically stacked on Si CMOS achieves high-speed access and long-term retention.

2:25 PM

6-3 | First Demonstration of 4-layer Stacked Planar Channel-All-Around (P-CAA) IGZO FETs with Cost-effective Process for High-density 1T1C 3D DRAM, Weiwei Li, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Xuezheng Ai, Beijing Superstring Academy of Memory Technology|Chen Gu, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Chuanke Chen, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Congyan Lu, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|xinlv Duan, Beijing Superstring Academy of Memory Technology|Jianqi Chen, Beijing Superstring Academy of Memory Technology|Xiangsheng Wang, Beijing Superstring Academy of Memory Technology|Kaiping Zhang, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Jin Dai, Beijing Superstring Academy of Memory Technology|Mingxu Liu, Beijing Superstring Academy of Memory Technology|Jiebin Niu, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Chuanhui Huang, Beijing Superstring Academy of Memory Technology|Jinjuan Xiang, Beijing Superstring Academy of Memory Technology|Yong Yu, Beijing Superstring Academy of Memory Technology|Feng Shao, Beijing Superstring Academy of Memory Technology|Guanhua Yang, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Yu Liu, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Xiaomeng Liu, Beijing Superstring Academy of Memory Technology|Shaohua Wang, Beijing Superstring Academy of Memory Technology|Bok-Moon Kang, Beijing Superstring Academy of Memory Technology|Gengfei Li, Beijing Superstring Academy of Memory Technology|Shenjie Zhao, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Nianduan Lu, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Di Geng, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences|Guilei Wang, Beijing Superstring Academy of Memory Technology|Chao Zhao, Beijing Superstring Academy of Memory Technology|Ling Li, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of

Microelectronics, Chinese Academy of Sciences|Ming Liu, State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences

We demonstrated the first 4-layer stacked planar channel-all-around (P-CAA) IGZO FETs for cost-effective and high-density 3D DRAM, which addresses the scaling limitation encountered by planar 2D device. This innovative architecture involves a sequential deposition of all planar layers in the cell array. Then, an efficient one-step fabrication process is proposed to manufacture transistors on all layers. The proposed approach tackles the problem of low fabrication efficiency encountered by the conventional layer by layer stacked 3D DRAM. Leveraging the remarkably low leakage current characteristics of the IGZO FETs, the device can have long data retention time.

2:50 PM

6-4 | First Demonstration on the Transient Writing Characteristics of Multi-bit ALD IGZO 2T0C DRAM by Fast I-V Measurement, Liankai Zheng, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University|Ziheng Wang, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University|Zhiyu Lin, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University|Mengwei Si, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University

We investigate the transient characteristics during the multi-bit writing operation of the 2T0C DRAM by ALD IGZO transistors. There are three main mechanisms that contribute to the transient voltage drop on storage node after data writing, including capacitive coupling, mobile charge sharing and trapped charge releasing. The data crosstalk caused by trapped charge releasing effect is identified as the major challenge for the multi-bit IGZO 2T0C DRAM. By optimizing the interface of gate insulator and IGZO, and adopting a proposed writing strategy, the 4-bit 2T0C DRAM without data crosstalk is achieved with low standard deviation on read current.

3:40 PM

6-5 | Complementary Oxide Semiconductor-based 2T0C DRAM Macro with CFET peripherals using TeOx-PFET/IGZO-NFET for 3D Memory Integration, Yanbo Su, School of Integrated Circuits, Tsinghua University, SAMT|Ting Liu, School of Integrated Circuits, Tsinghua University|Jianshi Tang, School of Integrated Circuits, Tsinghua University|Yijun Li, School of Integrated Circuits, Tsinghua University|Ran An, School of Integrated Circuits, Tsinghua University|Yiwei Du, School of Integrated Circuits, Tsinghua University|Zhidong Tang, School of Integrated Circuits, Tsinghua University|Yibei Zhang, School of Integrated Circuits, Tsinghua University|Yijia Fan, School of Integrated Circuits, Tsinghua University|Yuan He, School of Integrated Circuits, Tsinghua University|Mingcheng Shi, School of Integrated Circuits, Tsinghua University|Huimin Yang, School of Integrated Circuits, Tsinghua University|Tao Huang, School of Integrated Circuits, Tsinghua University|Jing Zhang, SAMT|Zhengyong Zhu, SAMT|Guilei Wang, SAMT|Chao Zhao, SAMT|Chen Wang, School of Materials Science and Engineering, Tsinghua University|Liyang Pan, School of Integrated Circuits, Tsinghua University|Peng Yao, School of Integrated Circuits, Tsinghua University|Dong Wu, School of Integrated Circuits, Tsinghua University|Bin Gao, School of Integrated Circuits, Tsinghua University|He Qian, School of Integrated Circuits, Tsinghua University|Huaqiang Wu, School of Integrated Circuits, Tsinghua University

To meet the increasing demand for on-chip memory to handle high-bandwidth data transfer, we present the first fully integrated complementary oxide semiconductor (OS)-based 2T0C DRAM macro with CFET peripherals. This was accomplished using top-gate TeO_x-PFET and back-gate IGZO-NFET via an ultra-low-temperature (≤150 °C) backend-of-the-line (BEOL) process. By integrating IGZO-NFET as the write transistor and TeO_x-PFET as the read transistor, a 4×4 array of hybrid-polarity 2T0C DRAM cells was demonstrated, achieving 2-bit/cell capacity and a decent retention. In addition, the proper functionality of theOS-based CFET peripherals was validated. This work presents a viable DRAM macro for future 3D memory integration.

4:05 PM

6-6 | First Demonstration of a N-P Oxide Semiconductor Complementary Gain Cell Memory, Fabia Farlin Athena, Stanford University|Elia Ambrosi, Taiwan Semiconductor Manufacturing Company|Koustav Jana, Stanford University|Cheng-Hsien Wu, Taiwan Semiconductor Manufacturing Company|Jonathan Hartanto, Stanford University|Yuan-Mau Lee, Stanford University|C. C. Kuo, Taiwan Semiconductor Manufacturing Company|Shuhan Liu, Stanford University|Balreen Saini, Stanford University|C. C. Wang, Taiwan Semiconductor Manufacturing Company|Chen-Feng Hsu, Taiwan Semiconductor Manufacturing Company|Gilad Zeevi, Stanford University|Xinxin Wang, Stanford University|Jimin Kang, Stanford University|Eric Pop, Stanford University|T. Y. Lee, Taiwan Semiconductor Manufacturing Company|Paul C. McIntyre, Stanford University|H.-S. Philip Wong, Stanford University|Xinyu Y. Bao, Taiwan Semiconductor Manufacturing Company

This work presents the first experimental demonstration of a Complementary Gain Cell (CGC) memory utilizing an n-type oxide semiconductor transistor (OSFET) as the write and a p-type OSFET as the read transistor. Complementary polarities mitigate capacitive coupling utilizing voltage sensing. The ALD IWO nFET has a positive V_{TH}~1.15 V and SS ~80 mV/dec and SnO pFET has an $I_{on}/I_{off} > 5\times10^4$. The CGC achieves a retention of 10000 seconds and can mitigate WL capacitive coupling. The n-type and p-type OSFETs for the 2T gain cell enable multilayer monolithic 3D integrated memory, paving the way for future “chip city” developments.

4:30 PM

6-7 | Novel 4F2 Multi-bit Dual-gate 2T0C for High-density DRAM with Improved Vertical-channel IGZO TFTs by Self-aligned Single-step Process, Fuxi Liao, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China|Zhengyong Zhu, Bejing Superstring Academy of Memory Technology, Beijing 100176, China|Guanhua Yang, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China|Arokia Nathan, Darwin College, Cambridge University|Ling Li, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China|Ming Liu, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China

For the first time, we propose and experimentally demonstrate one novel $4F^2$ vertical-channel IGZO multi-bit dual-gate (DG) 2T0C. Contrary to the sequential integration in single-gate (SG) $4F^2$ 2T0C, vertical-channel IGZO DG write and read transistors in $4F^2$ 2T0C are integrated simultaneously by adopting self-aligned single-step (SASS) process. This integration process is not only cost-effective but also releases the typical misalignment, thermal cycling and contamination issues.

9 | PMA | High Performance III-V and WBG RF FETs
1:30 PM – 4:55 PM, Imperial A
Co-chairs: Colombo Bolognesi, ETH Zurich and Vibhor Jain, Globalfoundries

The session includes 7 papers focusing on high speed and high performance RF FETs based on III-V and WBG material system. The session covers a broad variety of wide bandgap materials including InP, GaN, Ga2O3 and diamond. The first paper by Siddharth Sinha from IMEC showcases initial results for a RF Silicon Interposer with 3 thick metal RDL and an InP chiplet integration above 100 GHz. The second paper is an invited talk by Prof Erik Lind of Lund University providing an overview of planar and non-planar III-V MOSFETs for RF. The paper will cover topics on RF FET models, cryogenic applications, QW and nanowire mosfet RF devices. The next paper will be presented by Han Wui Then of Intel Foundry Technology Research highlighting an industry first 30nm Channel-Length E-Mode GaN MOSHEMTs on a 300mm GaN-on-TRSOI Engineered Substrate. The paper showcases a RF switch with Ron x Coff of 80fs and an e-mode source field plate HEMT with fmax>500GHz. Continuing with GaN RF switches, the next paper will be presented by Luca Lucci from CEA Leti covering GaN-on-Si HEMTs for high-power RF switch applications demonstrating Pmax of 36dBm and Ron x Coff below 200fs. The fifth paper by Thai Son Nguyen from Cornell University demonstrates strain-balanced AlScN/GaN HEMTs and characterizes the effect of gate scaling on device performance. The shortest gate length of 40 nm yields an fT/fMAX performance of 173/321 GHz. Moving to UWBG material systems, the next paper by Tiancheng Zhao from Chinese Academy of Sciences demonstrates Ga2O3 MOSFETs on diamond substrates with a record non-deembedded fmax of 61 GHz. Finally, the last paper by Xinxin Yu of the Nanjing Electronic Devices Institute reports a 2DHG based diamond RF MOSFET with the high-k HfO2 gate and passivation dielectric having fT/fMAX of 90/164 GHz for an 80-nm gate length.

1:30 PM
9-0 | Welcome

1:35 PM
9-1 | Hetero-Integration of InP Chiplets on a 300 mm RF Silicon Interposer for mm-wave Applications, Siddhartha Sinha, IMEC|Hamideh Jafarpoorchekab, IMEC|Nelson Pinho, IMEC|Damien Leech, IMEC|Koen Kennes, IMEC|Francois Chancerel, IMEC|Angel Uruena, IMEC|Ehsan Shafahian, IMEC|Melina Lofrano, IMEC|Andy Miller, IMEC|Eric Beyne, IMEC|Nadine Collaert, IMEC|Xiao Sun, IMEC

Hetero-Integration of InP Chiplets on a 300 mm RF Silicon Interposer is reported with interposer line loss of 0.23-0.3 dB/mm, flip-chip interconnect loss of 0.1 dB both at 140 GHz. Hetero-integrated PA has16.3 dB small-signal gain, 116-148 GHz bandwidth, P1dB of 13-15 dBm and 15-28 % PAE.

2:00 PM
9-2 | III-V MOSFETs for RF Applications (Invited), Erik Lind, Lund University

Integration of high quality oxides on III-V materials allows for versatile design of electronic devices, suitable for RF and power applications. We here present an overview of our results of planar and non-planar III-V MOSFETs for RF electronics, highlighting possibilities and challenges.

2:25 PM

9-3 | 30nm Channel-Length Enhancement-Mode GaN MOSHEMT Transistors on a 300mm GaN-on-TRSOI Engineered Substrate, Han Wui Then, Intel Corporation|Pratik Koirala, Intel Corporation|Leo Varghese, Intel Corporation|Ahmad Zubair, Intel Corporation|Samuel Bader, Intel Corporation|Michael Beumer, Intel Corporation|Heli Vora, Intel Corporation|Prafful Golani, Intel Corporation|Jason Peck, Intel Corporation|Thomas Hoff, Intel Corporation|Curtis Hoffman, Intel Corporation|Wesley Harrison, Intel Corporation|Marko Radosavljevic, Intel Corporation

We demonstrate for the first time, 30nm GaN MOSHEMTs fabricated on 300mm TRSOI engineered-substrate, and show that superior performance due to scaling of GaN MOSHEMT can be replicated on such a novel substrate. Advanced engineered-substrates improve RF and power electronics performanceby reducing signal loss and achieving better signal linearity.

2:50 PM
9-4 | CMOS compatible 200 mm GaN-on-Si HEMTs for RF switch applications with 36 dBm CW power handling and 200 fs RonCoff, Luca Lucci, CEA Leti, université Grenoble-Alpes|Ismael Charlet, CEA Leti|Yveline Gobil, CEA Leti|Fanny Morisot, CEA Leti|Julien Delprato, CEA Leti|Simon Ruel, CEA Leti|Khatia Benotmane, CEA Leti, CEA Leti|Fabien Laulagnet, CEA Leti|Romain Bon, CEA Leti|pattamon Dezest, CEA Leti|Arnaud Anotta, CEA Leti|Thierry Billon, CEA Leti|Blandine Duriez, CEA Leti|Erwan Morvan, CEA Leti

We present a study on GaN-on-Silicon high-electron-mobility transistors (HEMTs) designed for high-power RF switch applications. These devices are manufactured using a fully CMOS-compatible 200 mm process and feature a 100nm channel length, a recessed gate and an AlN spacer for enhanced performance, and low-temperature Ohmic contacts. The most robust device demonstrate power handling exceeding the measurement setup ceiling of 37 dBm. The top-performing HEMT achieves 35 dBm on a single shunt device with a 200 fs RonCoff. We also report excellent linearity for second and third harmonics of a 925 MHz fundamental.

3:40 PM
9-5 | Strain-balanced AlScN/GaN HEMTs with fT/fMAX of 173/321 GHz, Thai Son Nguyen, Cornell University|Kazuki Nomoto, Cornell University|Wenwen Zhao, Cornell University|Chandrashekhar Savant, Cornell University|Huili (Grace) Xing, Cornell University|Debdeep Jena, Cornell University

We report performance of novel strain-balanced AlScN/GaN HEMTs on SiC with n^+GaNregrown contacts and gate length scaling to 40 nm.The 40 nm AlScN/GaN HEMTs exhibit ON resistance of0.83 Ω·mm, maximum drain current of 2.8 A/mm, peak transconductance of 0.55 S/mm, and record high f_T/f_{MAX} of 173/321 GHz.

4:05 PM
9-6 | First Demonstration of Wafer-level Arrayed β-Ga2O3 Thin Films and MOSFETs on Diamond by Transfer Printing Technology, Tiancheng Zhao, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China|Xinxin Yu, CETC Key Laboratory of Carbon-based Electronics, Nanjing Electronic Devices Institute, Nanjing 210016, China|Wenhui Xu, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China|Yang He, School of Science and Ministry of Industry and Information Technology Key

Laboratory of Micro-Nano Optoelectronic Information System, Harbin Institute of Technology, Shenzhen 518055, China|Zhenyu Qu, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China|Rui Shen, National Key Laboratory of Solid-State Microwave Devices and Circuits, Nanjing 210016, China|Ruize Wang, National Key Laboratory of Solid-State Microwave Devices and Circuits, Nanjing 210016, China|Huaixin Guo, National Key Laboratory of Solid-State Microwave Devices and Circuits, Nanjing 210016, China|Huarui Sun, School of Science and Ministry of Industry and Information Technology Key Laboratory of Micro-Nano Optoelectronic Information System, Harbin Institute of Technology, Shenzhen 518055, China|Zhonghui Li, CETC Key Laboratory of Carbon-based Electronics, Nanjing Electronic Devices Institute, Nanjing 210016, China|Min Zhou, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China|Tiangui You, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China|Xin Ou, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China

1-inch diamond-based β-Ga_2O_3 single-crystal thin films with exceptional quality are fabricated via transfer printing technique for the first time. Heterogeneous integration with diamond significantly enhances β-Ga_2O_3 RF device performance and thermal dissipation, paving the way for high-power and RF applications.

4:30 PM

9-7 | High-k/Diamond RF MOSFETs with Record High fT/fmax of 90/164 GHz and First Demonstration of a Diamond MMIC, Xinxin Yu, CETC Key Laboratory of Carbon-based Electronics, Nanjing Electronic Devices Institute|Bin Qiao, CETC Key Laboratory of Carbon-based Electronics, Nanjing Electronic Devices Institute|Yan Sun, National Key Laboratory of Solid-State Microwave Devices and Circuits|Ran Tao, CETC Key Laboratory of Carbon-based Electronics, Nanjing Electronic Devices Institute|Ruize Wang, National Key Laboratory of Solid-State Microwave Devices and Circuits|Jianjun Zhou, National Key Laboratory of Solid-State Microwave Devices and Circuits|Huaixin Guo, National Key Laboratory of Solid-State Microwave Devices and Circuits|Zhonghui Li, CETC Key Laboratory of Carbon-based Electronics, Nanjing Electronic Devices Institute, National Key Laboratory of Solid-State Microwave Devices and Circuits|Haiyan Lu, National Key Laboratory of Solid-State Microwave Devices and Circuits|Hehe Gong, School of Electronic Science and Engineering, Nanjing University, Virginia Tech|Zhengyi Cao, CETC Key Laboratory of Carbon-based Electronics, Nanjing Electronic Devices Institute|Yuhao Zhang, Virginia Tech|Jiandong Ye, School of Electronic Science and Engineering, Nanjing University|Yuechan Kong, National Key Laboratory of Solid-State Microwave Devices and Circuits|Tangsheng Chen, National Key Laboratory of Solid-State Microwave Devices and Circuits

We present a hydrogenated diamond RF MOSFET with a high-k HfO_2 gate and passivation dielectric, offering high performance for RF applications. HfO_2 enhances transconductance (g_m), suppresses the short-channel effect, and maintains thermal stability. Two devices were fabricated: an 80 nm device achieving recordf_T/f_{max} of 90/164 GHz and $g_m$of 251 mS/mm, and a 1 μm L_G device achieving output power densities of 3.3 W/mm@6 GHz and 4.16 W/mm@2 GHz. The channel temperature rise is 32% of a GaN HEMT. A diamond MMIC demonstrated 117 mW output power at 10 GHz, highlighting the potential for high-k/diamond devices in RF applications.

2 | ALT | Gate-All-Around and 3D Stacked Transistors
1:30 PM – 5:20 PM, Grand Ballroom A
Co-Chairs: Chung-Hsun Lin, Intel and Maureen Wang, TSMC

As FinFET scaling reaches it's limits in the 3nm node, the gate-all-around (GAA) transistor is the most pragmatic device architecture in the near term to enable incremental contact-poly pitch and gate length scaling because of its limited perturbation to a conventional FinFET process integration and design flows. Backside power delivery and 3D stacking Complementary CFET technology brings additional cell level area scaling and performance benefit as well as heterogeneous integration benefit for high mobility channel enablement. This session covers recent advances in gate-all-around (GAA) and 3D stacked transistor technology to further extend Moore's law, consisting of eight papers both from industry and academia. The first three papers highlight GAA device topics ranging from commercial platform offering readiness to critical GAA scaling enablers. These are followed by CFET related papers addressing CFET DTCO, at-pitch process integration demonstration, and key CFET building blocks in the area of metal gate stack and direct backside contact to stepped channels.

1:30 PM
2-0 | Welcome

1:35 PM
2-1 | 2nm Platform Technology featuring Energy-efficient Nanosheet Transistors and Interconnects co-optimized with 3DIC for AI, HPC and Mobile SoC applications (Late News), Geoffrey Yeap, TSMC|SS Lin, TSMC|HL Shang, TSMC|HC Lin, TSMC|YC Peng, TSMC|M Wang, TSMC|PW Wang, TSMC|CP Lin, TSMC|CP Lin, TSMC|KF Yu, TSMC|WY Lee, TSMC|HK Chen, TSMC|DW Lin, TSMC|BR Yang, TSMC|CC Yeh, TSMC|C-T Chan, TSMC|JM Kuo, TSMC|C-M Liu, TSMC|T-H Chiu, TSMC|M-C Wen, TSMC|TL Lee, TSMC|CY Chang, TSMC|R Chen, TSMC|P-H Huang, TSMC|CS Hou, TSMC|YK Lin, TSMC|FK Yang, TSMC|J Wang, TSMC|S Fung, TSMC|Ryan Chen, TSMC|CH Lee, TSMC|TL Lee, TSMC|W Chang, TSMC|DY Lee, TSMC|CY Ting, TSMC|T Chang, TSMC|HC Huang, TSMC|HJ Lin, TSMC|C Tseng, TSMC|CW Chang, TSMC|KB Haung, TSMC|YC Lu, TSMC|C-H Chen, TSMC|CO Chui, TSMC|KW Chen, TSMC|MH Tsai, TSMC|CC Chen, TSMC|N. Wu, TSMC|HT Chiang, TSMC|XM Chen, TSMC|SH Sun, TSMC|JT Tzeng, TSMC|K wang, TSMC|YC Peng, TSMC|HJ Liao, TSMC|T Chen, TSMC|YK Cheng, TSMC|J Chang, TSMC|K Hsieh, TSMC|A Chang, TSMC|G Liu, TSMC|A Chen, TSMC|HT Lin, TSMC|KC Chiang, TSMC|CW Tsai, TSMC|H Wang, TSMC|W Sheu, TSMC|J Yeh, TSMC|YM Chen, TSMC|CK Lin, TSMC|J Wu, TSMC|M Cao, TSMC|LS Juang, TSMC|F Lai, TSMC|Y Ku, TSMC|SM Jang, TSMC|LC Lu, TSMC

This industry-leading N2 logic technology features energy- efficient gate-all-around nanosheet transistors, middle-of- line and backend-of-line interconnects with densest SRAM macro of ~38Mb/mm2. N2 delivers a full node benefit in offering 15% speed gain or 30% power reduction with 1.15x chip density increase. N2 successfully met wafer-level reliability requirements and passed 1000hrs HTOL qual with high yielding 256Mb HC/HD SRAM, and logic test chip (>3B gates) consisting of CPU/GPU/ SoC blocks. Currently in risk production, N2 platform technology is scheduled for mass production in 2H'25.

2:00 PM

2-2 | Silicon RibbonFET CMOS at 6nm Gate Length, Ashish Agrawal, Intel Corporation|Wriddhi Chakraborty, Intel Corporation|Wenshen Li, Intel Corporation|Hojoon Ryu, Intel Corporation|Brian Markman, Intel Corporation|Seung Hoon Sung, Intel Corporation|Rajat Paul, Intel Corporation|Cheng-Ying Huang, Intel Corporation|Su-Min Choi, Intel Corporation|Kyeong Rho, Intel Corporation|Andrew Shu, Intel Corporation|Raul Iglesias, Intel Corporation|Patrick Wallace, Intel Corporation|Susmita Ghose, Intel Corporation|Joshua Hockel, Intel Corporation|Kai Loon Cheong, Intel Corporation|Rachel Thorman, Intel Corporation|Lukas Baumgartel, Intel Corporation|Leah Shoer, Intel Corporation|Varun Mishra, Intel Corporation|Salim Berrada, Intel Corporation|Cory Weber, Intel Corporation|Borna Obradovic, Intel Corporation|Adedapo Oni, Intel Corporation|A Ashita, Intel Corporation|Zachary Brooks, Intel Corporation|Noel Franco, Intel Corporation|Jack Kavalieros, Intel Corporation|Gilbert Dewey, Intel Corporation

Gate-all-around Silicon RibbonFET CMOS transistors at gate length (LG) of 6nm are demonstrated and comprehensively characterized. Nanoribbon Tsi scaling demonstrated to improve short channel effect without penalty to performance down to 3nm. Effective workfunction engineering is performed to reduce threshold voltage at highly scaled gate length and compensate for threshold voltage increase due to quantum confinement at scaled Tsi. Injection velocity of 1.13x10^7 cm/s at LG=6nm with no degradation down to Tsi=3nm is demonstrated. These key highlights pave the path for continued gate length scaling which is one of the key foundational cornerstones of Moore's law.

2:25 PM

2-3 | Advanced Multi-Vt Enabled by Selective Layer Reductions for 2nm Nanosheet Technology and Beyond, Ruqiang Bao, IBM Research|Yusuke Oniki, Rapidus US, LLC|Xiaoli He, IBM Research|Yasuhiro Isobe, Rapidus US, LLC|Prateek Hundekar, IBM Research|Seiji Matsuyama, Rapidus US, LLC|Sylvie Mignot, IBM Research|Alma Ramirez, IBM Research|Shohei Kawamoto, Rapidus US, LLC|Hiroshi Abe, Rapidus US, LLC|Anthony Chou, IBM Research|Will Parkin, IBM Research|Tatsufumi Hamada, Rapidus US, LLC|Muthumanickam Sankarapandian, IBM Research|Paul Jamison, IBM Research|Alexander Reznicek, IBM Research|Sriharsha Sudhindra, IBM Research|Yuji Murakami, Rapidus US, LLC|Trevor McDonough , IBM Research|Sushant Kumar, IBM Research|Wayne Zhao, IBM Research|HUIMEI ZHOU , IBM Research|Juntao Li, IBM Research|Govind Bajpai, IBM Research|ERIC MILLER , IBM Research|INDIRA SESHADRI, IBM Research|Liqiao Qin, IBM Research|Charlotte Adams, IBM Research|Miaomiao Wang, IBM Research|Yu Zhu, IBM Research|BROWN PEETHALA , IBM Research|DK Sohn, IBM Research|Mark Lagus, IBM Research|Kai Zhao, IBM Research|Renee Mo, IBM Research|Effendi Leobandung, IBM Research|Dechao Guo, IBM Research|Yuzo Fukuzaki, Rapidus US, LLC|Huiming Bu, IBM Research

We demonstrated several new approaches to enable multiple threshold voltage (multi-Vt) solutions for 2nm high-performance nanosheet technology and beyond. Selective layer reduction 1 (SLR1) is proposed to control N/P boundary by solving the undercut of thin layer patterning on top of Tsus pinchoff scheme. A new etch process is also developed to solve plasma damage for thin layer integration. Selective layer reduction 2 (SLR2) is used to control N/P boundary of thick work function metal (WFM) integration to offer low Vt device. With improved dual-dipoles integration, 4 pairs of Vts are enabled for 2 nm high-performance NS technology and beyond.

3:15 PM

2-4 | Double-Row CFET: Design Technology Co-Optimization for Area Efficient A7 Technology Node, Halil Kukner, imec|Gioele Mirabelli, imec|Sheng Yang, imec|Lynn Verschueren, imec|Juergen Boemmels,

imec|Ji-Yung Lin, imec|Dawit Abdi, imec|Anita Farokhnejad, imec|Odysseas Zografos, imec|Naoto Horiguchi, imec|Marie Garcia Bardon, imec|Geert Hellings, imec|Julien Ryckaert, imec

Complementary FET (CFET) device architecture with stacked n-/p-FETs promises power, performance, area scalability in the post-FinFET era. Among several options, the double-row CFET architecture leads to reduced process complexity in the middle-of-line, and gains in logic and SRAM area. Projections show ~40% area and ~12% power scaling potential.

3:40 PM

2-5 | First Demonstration of Monolithic CFET Inverter at 48nm Gate Pitch Toward Future Logic Technology Scaling, Szuya Liao, Taiwan Semiconductor Manufacturing Company|Lu Yang, Taiwan Semiconductor Manufacturing Company|Wei-Xiang You, Taiwan Semiconductor Manufacturing Company|Ting-Yun Wu, Taiwan Semiconductor Manufacturing Company|Yi-Che Lee, Taiwan Semiconductor Manufacturing Company|Tsung-Kai Chiu, Taiwan Semiconductor Manufacturing Company|James Hsu, Taiwan Semiconductor Manufacturing Company|Wei-Der Ho, Taiwan Semiconductor Manufacturing Company|Yuan-Chi Yang, Taiwan Semiconductor Manufacturing Company|Ming-Chang Tsai, Taiwan Semiconductor Manufacturing Company|Hsin Yang Hung, Taiwan Semiconductor Manufacturing Company|Rui-Fu Chen, Taiwan Semiconductor Manufacturing Company|Yi-Hsuan Li, Taiwan Semiconductor Manufacturing Company|Shao-Tse Huang, Taiwan Semiconductor Manufacturing Company|Ching Yen Lee, Taiwan Semiconductor Manufacturing Company|Ku-Feng Yang, Taiwan Semiconductor Manufacturing Company|Kuan-Kan Hu, Taiwan Semiconductor Manufacturing Company|Yu-Hsien Chiang, Taiwan Semiconductor Manufacturing Company|Hung-Kun Lo, Taiwan Semiconductor Manufacturing Company|Shih-Jung Ho, Taiwan Semiconductor Manufacturing Company|Chu-Hsuan Sha, Taiwan Semiconductor Manufacturing Company|Jin-Hao Jhang, Taiwan Semiconductor Manufacturing Company|Guan-Ren Wang, Taiwan Semiconductor Manufacturing Company|Chun-Yu Liu, Taiwan Semiconductor Manufacturing Company|Wei-Yen Woon, Taiwan Semiconductor Manufacturing Company|Cheng-Ming Lin, Taiwan Semiconductor Manufacturing Company|Szu-Hua Chen, Taiwan Semiconductor Manufacturing Company|Kai-Chieh Yang, Taiwan Semiconductor Manufacturing Company|Je-Ruei Wen, Taiwan Semiconductor Manufacturing Company|Chia-Min Chang, Taiwan Semiconductor Manufacturing Company|Yu-Tien Shen, Taiwan Semiconductor Manufacturing Company|Pinyen Lin, Taiwan Semiconductor Manufacturing Company|Chi-Ming Yang, Taiwan Semiconductor Manufacturing Company|Wei-Yip Loh, Taiwan Semiconductor Manufacturing Company|Gene Tsai, Taiwan Semiconductor Manufacturing Company|Chih Hung Chen, Taiwan Semiconductor Manufacturing Company|Richard Chen, Taiwan Semiconductor Manufacturing Company|Min Cao, Taiwan Semiconductor Manufacturing Company

This study presents the first functional advanced CFET inverter with an industry-leading 48nm gate pitch, exhibiting well-balanced voltage transfer characteristics up to 1.2V. In this paper, we elaborate on the advancements in our nanosheet-based monolithic complementary field-effect transistor (mCFET) process architecture, which builds upon our previous work. Key developments include integration of vertical dipole patterning, vertical metallized drain local interconnects, and backside middle-of-line contacts and interconnects. The successful demonstration of fully operational mCFET inverters marks an important milestone in the pioneering of CFET technology, paving the way for future logic technology scaling and the advancement of PPAC.

4:05 PM

2-6 | WNxCyVT Tuning of Split Gate Nanosheet CFETs with Dual Work Function Metals Achieving 0.93 VT Match/ Improved 0.24V Noise Margin/ Record Gain of 61V/V, Bo-Wei Huang, Graduate Institute of Electronics Engineering, National Taiwan University |Chun-Yi Cheng, Graduate Institute of Electronics Engineering, National Taiwan University|Wan-Hsuan Hsieh, Graduate Institute of Electronics Engineering, National Taiwan University|Yu-Rui Chen, Graduate Institute of Electronics Engineering, National Taiwan University|Wei-Jen Chen, Graduate Institute of Electronics Engineering, National Taiwan University|Yi-Chun Liu, Graduate Institute of Electronics Engineering, National Taiwan University |Min-Kuan Lin, Graduate School of Advanced Technology, National Taiwan University|Ying-Qi Liu, Graduate School of Advanced Technology, National Taiwan University|Hao-Yi Lu, Graduate School of Advanced Technology, National Taiwan University|Yi Huang, Graduate Institute of Photonics and Optoelectronics, National Taiwan University|Ding-Wei Lin, Graduate Institute of Electronics Engineering, National Taiwan University|Chee Wee Liu, Graduate Institute of Electronics Engineering, National Taiwan University, Graduate School of Advanced Technology, National Taiwan University, Graduate Institute of Photonics and Optoelectronics, National Taiwan University

The epitaxial growth and device fabrication of dual-WFM split-gate CFETs are demonstrated for the first time. The effective work function of WN_xC_y can be tuned during the PEALD process. The WN_xC_y are integrated into GeSi CFET to show the pFET V_T tunability of 500mV. The dual-WFM split-gate CFETs can provide matched V_T for n/pFETs. The noise margin of SRAM is expected to be 0.24V at V_{DD}=0.75V. The voltage transfer curve of a CFET inverter has a record gain of 61V/V among monolithic nanosheet CFETs. The WN_xC_y V_T tuning is also demonstrated for the nFET V_T tuning of 300mV.

4:30 PM

2-7 | Monolithic-CFET with Direct Backside Contact to Source/Drain and Backside Dielectric Isolation, Anne Vandooren, imec|Karen Stiers, imec|Cassie Sheng, imec|Camila Toledo de Carvalho Cavalcante, imec|Maryam Hosseini, imec|Dmitry Batuk, imec|Andy Peng, imec|Daisy Zhou, imec|Hans Mertens, imec|Anabela Veloso, imec|Andrea Mingardi, imec|Sujan Sarkar Kumar, imec|Rajendra Kumar Saroj, imec|Koen D'havé, imec|Thomas Chiarella, imec|Juergen Bömmels, imec|Roger Loo, imec|Erik Rosseel, imec|Clement Porret, imec|Yosuke Shimura, imec|Anjani Akula, imec|Subhobroto Choudhury, imec|Vincent Brissonneau, imec|Emmanuel Dupuy, imec|Tanushree Sarkar, imec|Nathali Franchina Vergel, imec|Anthony Peter, imec|Nicolas Jourdan, imec|Jean-Philippe Soulie, imec|Kevin Vandersmissen, imec|Serena Iacovo, imec|Daniel Montero Alvarez, imec|Evi Vrancken, imec|Farid Sebaai, imec|Pallavi Puttarame Gowda, imec|Kenneth Lai, imec|Nunzio Buccheri, imec|Philippe Matagne, imec|B.T. Chan, imec|Alfonso Sepulveda Marquez, imec|Robert Langer, imec|Il Gyo Koo, imec|Efrain Altamirano Sanchez, imec|Katia Devriendt, imec|Paulina Rincon Delgadillo, imec|Frederic Lazzarino, imec|Jerome Mitard, imec|Jef. Geypen, imec|Eva Grieten, imec|Yi-Fan Chen, imec|Frederik Verbeek, imec|Hans Pollenus, imec|Jeroen Heijlen, imec|Lucas Petersen Barbosa Lima, imec|Frank Holsteyns, imec|Sujith Subramanian, imec|Naoto Horiguchi, imec|Steven Demuynck, imec|Serge Biesemans, imec

This work reports on demonstration of monolithic complementary field effect (CFET) transistors using direct backside (BS) contact (DBC) to source and drain (SD) of the bottom PMOS device. We compare two integration options to avoid shorts between DBC and gate and/or Si substrate relying either on the use of an offset spacer or on formation of bottom dielectric isolation from the backside (BS-BDI). Both integration options result in functional bottom (pFET) and top (nFET) CMOS devices on a common gate at 60 nm gate pitch.

4:55 PM

2-8 | Monolithic Stacked FET with Stepped Channels for Future Logic Technologies, Chen Zhang, IBM Research|SeungMin Song, Samsung Electronics|Jay Strane, IBM Research|Lijuan Zou, IBM Research|Seungchan Yun, Samsung Electronics|Keumseok Park, Samsung Electronics|Abir Shadman, IBM Research|Jaehong Lee, Samsung Electronics|WuKang Kim, IBM Research|Utkarsh Bajpai, IBM Research|Larry Zhuang, IBM Research|Shahrukh Khan, IBM Research|Wai Kin Li, IBM Research|Shogo Mochizuki, IBM Research|Takashi Ando, IBM Research|Shay Reboh, IBM Research|Debarghya Sarkar, IBM Research|Myung Yang, Samsung Electronics|Myunghoon Jung, Samsung Electronics|Tsung-Sheng Kang, IBM Research|Ilhom Saidjafar, IBM Research|Nate Putnam, IBM Research|Shanti Pancharatnam, IBM Research|Muthumanickam Sankarapandian, IBM Research|Erik Milosevic, IBM Research|Junmo Park, Samsung Electronics|Kishwar Mashooq, IBM Research|Prabudhya Chowdhury, IBM Research|Jim Mazza, IBM Research|Nick Lanzillo, IBM Research|Sarah Chowdhury, IBM Research|Yeojin Lee, Samsung Electronics|Paul Jamison, IBM Research|Matt Malley, IBM Research|Pinlei Chu, IBM Research|Jeonghyun Hwang, IBM Research|Mohsen Nasseri, IBM Research|Kibyung Park, Samsung Electronics|Namkyu Cho, Samsung Electronics|Jongmin Shin, Samsung Electronics|Inwon Park, IBM Research|Thanh Nguyen, IBM Research|Beomjin Park, Samsung Electronics|Feng Liu, IBM Research|Shivani Kumar, IBM Research|Cliff Osborn, IBM Research|Juntao Li, IBM Research|Lukas Tierney, IBM Research|James Demarest, IBM Research|Junli Wang, IBM Research|Eric Miller, IBM Research|Susan Fan, IBM Research|Jingyun Zhang, IBM Research|Yu Zhu, IBM Research|John Arnold, IBM Research|Tenko Yamashita, IBM Research|Dan Dechene, IBM Research|Kangill Seo, Samsung Electronics|Dechao Guo, IBM Research|Huiming Bu, IBM Research

We present a monolithic stacked FET architecture featuring a stepped channel structure where the bottom FET channels are wider than the top. Such a design relieves high aspect ratio process challenges by reducing the total stack height and provides better performance as compared to its uniform channel width counterpart at the same footprint. In addition to the stepped channels, our integrated hardware work features top-bottom channel middle dielectric isolation, top-bottom source/drain isolation and dual work function metals. As the advanced technologies are facing significant power, performance and area scaling pressures, this work extends the narrowing road beyond the nanosheet architecture.

4 | RSD | Memory and Ferroelectric Material Reliability

1:30 PM – 5:20 PM, Continental 1 – 3

Co-Chairs: Kyoung Chul Jang, SK Hynix and Motoyuki Sato, Tokyo Electron Limited

In this session, we will discuss about the Memory and Ferroelectric Material Reliability. Firstly, the MIKFIS gate stack, combining ferro and non-ferroelectric HfO_2, addresses thickness and reliability issues in 3D NAND, achieving a record memory window of 12.2 V and stable 10-years retention, making it a promising solution for advanced 3D NAND technology. Secondly, Highly reliable metal-ferroelectric-metal (MFM) capacitors with β-W electrodes achieve 70 μC/cm² remnant polarization, 6.3 MV/cm breakdown field, and over 5×10^{12} cycles endurance, thanks to β-W's low lattice misfit with HZO and negligible oxygen vacancy. Thirdly, A WO_3 layer in ultra-thin HZO capacitors boosts endurance by 1000× at 125°C and reduces oxygen vacancy issues, improving performance at high temperatures and benefiting 3D memory applications. Next, they show that adding a TiO2 layer in MIFIS FeFETs improves memory window by 35% and prevents disturbances even after 10^4 stress cycles, by reducing charge trapping and enhancing polarization switching. In the fifth paper, highly reliable HZO FeRAM technology shows up to 10^{12}

endurance cycles at 85°C with ±1.2V, 100% yield for 256 kb 1T1C chips, and 20 ns operation speed, achieved through advanced nanocrystalline domain inspection, indicating improved performance and scalability. Next, they demonstrate H2 plasma treatment (HPT) significantly improves FeFET performance by reducing oxygen vacancies and interfacial traps, enhancing polarization switching, endurance, conductance, and linearity, and increasing thermal stability for FeCAM cells. Next, they investigated the physical mechanism of memory window (MW) narrowing in HZO/Si FeFETs and found that it can be mitigated by adjusting hold voltage. As a final paper, they introduce ultra-high vacuum re-annealing as a recovery strategy, showing that low-temperature re-annealing can restore Pr by up to 112%, advancing HfO-based memory technologies.

1:30 PM
4-0 | Welcome

1:35PM
4-1 | Superior QLC Retention (10 years, 85°C) and Record Memory Window (12.2 V) by Gate Stack Engineering in Ferroelectric FET: from "MIFIS" to "MIKFIS", Song-Hyeon Kuk, Korea Advanced Institute of Science and Technology|Bong Ho Kim, Korea Advanced Institute of Science and Technology|Youngkeun Park, Korea Advanced Institute of Science and Technology|Kyul Ko, Korea Institute of Science and Technology|Hyeon-Seong Hwang, Korea Advanced Institute of Science and Technology|Dahye Lee, Korea Advanced Institute of Science and Technology|Byung Jin Cho, Korea Advanced Institute of Science and Technology|Jae-Hoon Han, Korea Institute of Science and Technology|Sang-Hyeon Kim, Korea Advanced Institute of Science and Technology

We propose a novel gate stack, metal-insulator-high k-ferroelectric-insulator-semiconductor (MIKFIS) to address issues in (bandgap-engineered) MIFIS FEFETs. The main idea is that the FE-HfO2 thickness can be scaled down by partially replacing it with paraelectric (PE) HfO2, without increasing the gate stack thickness. Fabricated MIKFIS FEFETs show a record MW of 12.2 V with the Si channel, superior 10-year retention with quad-level-cell (QLC) operations at 24ºC and 85ºC. The origin of the superior retention is revealed by accurately measuring absolute polarization (P) directly from FEFETs, indicating that MIKFIS is a strong candidate for the 3D FE NAND gate stck.

2:00 PM
4-2 | Uniform and Fatigue-Free Ferroelectric HZO with Record EBD of 6.3MV/cm and Record Final 2Pr of 64μC/cm2 at Record 5E12 Endurance Using Low Lattice Misfit (2.9%) &[beta]-W, Guan-Hua Chen, Graduate Institute of Electronics Engineering, National Taiwan University|Yu-Tsung Liao, Graduate Institute of Electronics Engineering, National Taiwan University|Zefu Zhao, Graduate Institute of Electronics Engineering, National Taiwan University|Yu-Rui Chen, Graduate Institute of Electronics Engineering, National Taiwan University|Yun-Wen Chen, Graduate Institute of Electronics Engineering, National Taiwan University|Wei-Jen Chen, Graduate Institute of Electronics Engineering, National Taiwan University|Wei-Teng Hsu, Graduate Institute of Electronics Engineering, National Taiwan University|Hao-Yi Lu, Graduate School of Advanced Technology, National Taiwan University|Ming-Chang Liu, Graduate Institute of Electronics Engineering, National Taiwan University|Yu-An Chen, Graduate Institute of Electronics Engineering, National Taiwan University|C. W. Liu, Graduate Institute of Electronics Engineering, National Taiwan University, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Graduate School of Advanced Technology, National Taiwan University

Highly reliable metal-ferroelectric-metal (MFM) capacitors using β-W electrodes are demonstrated for the first time. β-W has low lattice misfit (2.9%) with respect to orthorhombic phase (o-phase) HZO. The low lattice misfit β-W favors HZO o-phase formation, and bottom β-W/HZO/top β-W capacitor reaches high remanent polarization (2Pr) of 70μC/cm2 with high uniformity. The β-W electrode has a flat surface (roughness ~0.5nm) without scavenging oxygen from HZO during annealing, leading to low oxygen vacancy (Vo2+) concentration in HZO with corresponding high breakdown field (EBD). MFM using β-W electrodes shows fatigue-free endurance due to negligible dipole pinning. The bottom β-W/HZO/top β-W capacitor reaches record EBD of 6.3MV/cm with 2Pr of 70μC/cm2 and record final 2Pr of 64μC/cm2 at record endurance larger than 5E12 cycles.

2:25 PM

4-3 | Self-Healing Ferroelectric Capacitors with ~1000x Endurance Improvement at High Temperatures (85-125°C), Nashrah Afroze1, Andrea Padovani2, Jihoon Choi3, Priyankka Gundlapudi Ravikumar1, Yu-Hsin Kuo1, Chengyang Zhang1, Taeyoung Song1, Mengkun Tian1, Eknath Sarkar1, Manifa Noor1, Prasanna Venkatesan Ravindran1, Khandker Akif Aabrar1, Bilge Yildiz4, Souvik Mahapatra5, Andrew Kummel6, Kyeongjae Cho7, Shimeng Yu1, Suman Datta1, Jun Hee Lee3, Luca Larcher8, Gaurav Thareja8, Asif Khan1, 1Georgia Institute of Technology, 2UNIMORE, 3UNIST, 4MIT, 5IIT Bombay, 6University of California San Diego, 7University of Texas Dallas, 8Applied Materials

For the first time, we demonstrate that introducing an interfacial WO_3 layer in ultra-thin ferroelectric Hf0.5Zr0.5O2 (HZO) capacitors improves endurance by 1000× at 125°C. It dramatically slows the degradation of write endurance with increasing temperature, leading to record-high endurance in a 5 nm HZO capacitor at elevated temperatures: 109 cycles at 85˚C and 108 cycles at 125˚C as well as >1012 cycles at 25˚C —all for complete polarization switching (2Pr≈40μC/cm2). Trap densities extracted from temperature- and cyclingdependent leakage currents show that the Oxygen vacancy (Vo) generation in HZO with cycling is significantly reduced in the presence of the WO3 layer. This is due to Oxygen (O) ion migration into HZO from WO3 during write pulses, which is favored by the asymmetric HZO/WO3 diffusion barrier (as calculated by Density Functional Theory-based models). Since this prevents back diffusion of O ions from HZO into WO3, there is a net migration of O ions into HZO with continued cycling, partially healing cycling-induced Vo generation. This is a thermally activated self-healing process that becomes more efficient at elevated temperatures, thereby explaining our experimental observations. This concept can be useful for ferroelectric memories (FE-RAMs and -FETs) in emerging 3D memory-on-logic architectures, where rising temperatures with increasing number of stacked dies is a major challenge.

3:15 PM

4-4 | Unveiling the Origin of Disturbance in FeFET and the Potential of Multifunctional TiO_2 as a Breakthrough for Disturb-free 3D NAND Cell: Experimental and Modeling, Giuk Kim, KAIST|Hyunjun Kang, KAIST|Sangho Lee, KAIST|Hyojun Choi, KAIST|Yangjin Jung, KAIST|Mincheol Shin, KAIST|Kwangsoo Kim, Samsung Electronics|Suhwan Lim, Samsung Electronics|Jongho Woo, Samsung Electronics|Wanki Kim, Samsung Electronics|Daewon Ha, Samsung Electronics|Jinho Ahn, Hanyang University|Sanghun Jeon, KAIST

We address the disturbance issues in MIFIS FeFETs and introduce a TiO_2 multi-functional layer for enhanced performance. Under the operation voltage below 15 V, the device with TiO_2 improves the MW by 35 % and remains disturbance-free even after 10^4 cycles of 9 V. In addition, we verify the primary driver

of disturbances by utilizing our model framework. This study highlights the potential of MIFIS FeFET for future NVM applications.

3:40 PM

4-5 | Highly Reliable and High-Yield 1.2V HfZrOx FRAM and its Physical Origin via Micrometer-Scale Nanocrystalline Domain Analysis, Yu-De Lin, Industrial Technology Research Institute|Chen-Yi Cho, National Yang Ming Chiao Tung University|Jian-Wei Su, Industrial Technology Research Institute|Yi-Hui Wei, Industrial Technology Research Institute|Li-Ying Hung, Industrial Technology Research Institute|Po-Han Chang, Industrial Technology Research Institute|Ching-Chih Hsu, Industrial Technology Research Institute|Po-Chun Yeh, Industrial Technology Research Institute|Min-Hung Lee, National Taiwan University|Tuo-Hung Hou, National Yang Ming Chiao Tung University|Shyh-Shyuan Sheu, Industrial Technology Research Institute|Wei-Chung Lo, Industrial Technology Research Institute|Shih-Chieh Chang, Industrial Technology Research Institute

A highly reliable $HfZrO_x$ FRAM technology has been achieved with the endurance of up to 10^{12} cycles at 85°C with ±1.2V. 256 kb 1T1C FRAM chips with 8nm and 6nm $HfZrO_x$ exhibit a 100% 8kb-yield without wake-up and with a 400 µs wake-up pulse, respectively. An operation speed of 20ns at ±1.2V is demonstrated in the Shmoo plot. The robust high-temperature reliability and high-yield arrays are achieved through a solid understanding of over-optimistic $2P_r$ and transmission Kikuchi diffraction (TKD) for micrometer-scale nanocrystalline crystal domain inspection. This work suggests a viable scaling path and improves the performance of $HfZrO_x$ FRAM technology.

4:05 PM

4-6 | Enhancing FeFET Performance through H2 Plasma Treatment: Improving Stability, Conductance, and Hamming Distance in FeCAM Designs, Ying-Tsan Tang, National Central University|ZiRong Huang, National Central University|Zheng Kai Chen, National Central University|Tzu Tsai Yu , National Central University|Chia Shuo Pai, National Central University|HaoMing Chen, National Central University|Sheng Tsang Huang , National Central University|Wei Ning Chang, Taiwan Semiconductor Research Institute|C.C Lin, Taiwan Semiconductor Research Institute

In this study, we demonstrate that H2 plasma treatment (HPT) enhances FeFET performance significantly by reducing oxygen vacancies (Vo) and interfacial traps (Dit) in HZO layers. This treatment lowers pinning fields, accelerates polarization switching, and reduces memory imprint effects, extending endurance to over 10^{11} cycles. HPT also enhances FeFET conductance, offering high Gmax/Gmin ratio and improved linearity, crucial for accurate neural network applications. FeCAM cells benefit from increased ON/OFF ratios, enabling more symmetrical mismatch currents and greater Hamming distances(HD). Moreover, HPT enhances thermal stability, ensuring FeCAM cells retain memory at 99.5°C for 10 years.

4:30 PM

4-7 | Unveiling memory-window narrowing mechanism after bipolar cycling in HZO/Si FeFETs: Critical role of hole trap generation and carrier de-trapping behavior, Seong-Kun Cho, The University of Tokyo|Kasidit Toprasertpong, The University of Tokyo|Mitsuru Takenaka, The University of Tokyo|Shinichi Takagi, The University of Tokyo

This study explores the memory window (*MW*) narrowing in HZO/Si FeFETs, a major reliability issue, using a new focus on hold voltage (V_{Hold}) and a method to independently measure polarization (*P*) and threshold

voltage (V_{TH}). We find that adjusting V_{Hold} can mitigate *MW* narrowing, caused by trapped electrons and holes during the hold condition. The V_{TH}-*P* relationship shows that rapid hole trap generation during cycles is crucial for *MW* narrowing, while polarization switching remains unchanged even in devices without *MW*. Suppressing trap generation through material engineering improves FeFET reliability.

4:55 PM
4-8 | Polarization degradation and recovery strategies of hafnia-based ferroelectric capacitors after thermal budget in Back-End of Line process, Yunzhe Zheng, East China Normal University|Qiwendong Zhao, East China Normal University|Zhaomeng Gao, East China Normal University|Tianjiao Xin, East China Normal University|Yilin Xu, East China Normal University|Cheng Liu, East China Normal University|Yonghui Zheng, East China Normal University|Yan Cheng, East China Normal University

By addressing the issue of polarization degradationof hafnia-based FEmemory after BEOL process, we reveal a close correlation between Prlossand alterations in oxygen levels, proposingstrategies for recovery. (1) Oxygen migration into FeCAPs during Furnaceintroduces domain pinning, which diminishes Pr and decelerates switching speed; (2) The recovery strategy of ultra-high vacuum ReRTAto extract oxygen is demonstrated for the first time; (3) Low-temperature ReRTA(350℃) in10^{-2}Pa with sufficient time (30 min) can make Pr recover up to 112%. These results provide insights into the mechanisms underlying thermal degradation and restorability of hafnia-based memory technologies.

7 | MS | Compact Modeling and DTCO
1:30 PM – 5:20 PM, Continental 6
Co-Chairs: Lado Filipovic, TU Wien and Jing Wang, NVIDIA

This session includes 8 papers that describe recent advances in compact modeling and the application of design-technology co-optimization (DTCO). The first paper, by Passlack from TSMC, covers statistical modeling of Carbon Nanotube MOS capacitors. The second paper, by Vermeersch from imec, discusses the multiple-scale thermal impact of backside power delivery networks (BSPDNs). The third paper, by Pal from Applied Materials, presents logic and SRAM interconnect design for advanced Complementary FETs (CFETs). It is followed by the fourth paper, by Lu from National Taiwan University, which covers conflict-free and area-efficient 4N4P CFET 8T SRAM design for multiple-bit compute-in-memory applications. The next three papers deal with different memory technologies. First, Chen, from Macronix International Co., Ltd., proposes a multi-wordline array transistor to minimize gate-induced drain leakage, the floating body effect, and the row hammer effect in advanced DRAM geometries. Zhang, from Beihang University, then introduces a production line level magnetic tunnel junction (MTJ) modeling framework which combines graph neural networks and deep neural networks to accurately predict MTJ parameter distribution under manufacturing variations. Thereafter, Thesberg, from Global TCAD Solutions, provides a thorough experimentally validated variability study of the performance of ferroelectric VNAND, which helps to quantify the benefit of selecting IGZO-based devices over polysilicon for a ferroelectric bit cell. The final paper in this session, by Feng from IMECAS, provides a multi-scale atomistic modeling approach for etching that involves 600,000 atoms with an almost 45-times speedup and a 4-times error reduction when compared to classical molecular dynamics.

1:30 PM
7-0 | Welcome

1:35 PM

7-1 | Statistics Based Modeling and Analysis of Ultra-Low Impedance Carbon Nanotube MOS Capacitors, Matthias Passlack, TSMC|Nathaniel Safron, TSMC|Aaryan Oberoi, TSMC|Carlo Gilardi, TSMC|Jack Zuo, TSMC|Sheng-Kai Su, TSMC|Tzu-Ang Chao, TSMC|Amin Azizi, TSMC|Shreyam Natani, UCSD|Gilad Zeevi, Stanford University|Prabhakar Bandaru, UCSD|Andrew Kummel, UCSD|H.-S. Philip Wong, TSMC|Gregory Pitner, TSMC|Iuliana Radu, TSMC

We report the first direct extraction of CNT MOSinterface metrics normalized to CNT length or CNT surfacearea using statistical impedance modeling and analysis oflateral capacitors measured between 100 and 300 K. Direct D_{it}extraction from impedance is a crucial step towards highperformance CNT MOSFETs and is enabled by (i) a statisticalapproach towards modeling of CNT impedance, (ii) a capacitorarchitecture meeting the requirements for D_{it} extraction, and(iii) the extension of impedance acquisition to below 1 fF, and (iv)rigorous treatment of surface potential fluctuations in depletion due to fixed charge and CNT diameter variations.

2:00 PM

7-2 | Multiscale Thermal Impact of BSPDN: SoC Hotspot Challenges and Partial Mitigation, Bjorn Vermeersch, imec|Subrat Mishra, imec|Moritz Brunion, imec|Odysseas Zografos, imec|Melina Lofrano, imec|Herman Oprins, imec|James Myers, imec|Zsolt Tokei, imec|Geert Hellings, imec

Realistic workload-based CPU powermaps reveal that nonuniform dissipation majorly accentuates hotspots in BSPDN-based designs. 1um-resolution temperature simulations of an 80-core server SoC show ~14°C penalties relative to FSPDN caused by interplay of extraneous thermal resistance (BEOL + wafer bonding) and BSPDN heat spreading. Mitigation strategies are proposed and quantified.

2:25 PM

7-3 | Novel Logic & SRAM Interconnect Design for Advanced Complementary FET (CFET) based Technology Nodes, Ashish Pal, Applied Materials|Pratik Vyas, Applied Materials|Sefa Dag, Applied Materials|Gregory Costrini, Applied Materials|Benjamin Colombeau, Applied Materials|Bala Haran, Applied Materials|Subi Kengeri, Applied Materials|El Mehdi Bazizi, Applied Materials

Using our MSCO™ platform, we investigate several CFET interconnect design options to mitigate parasitics associated with the super-vias to improve circuit performance. A hybrid frontside-backside (FS-BS) PDN scheme, backside signaling, and common gate architectures are proposed to eliminate NMOS VSS super-via, PMOS drain and gate supervias, resulting in 6%, 4% and 11% circuit performance benefit, respectively. A novel high density CFET SRAM cell is proposed with NMOS access transistor, unused PMOS device removal from backside and hybrid FS-BS-PDN scheme showing 60% read-delay and 24% write-delay improvement in comparison to PMOS access transistor counterpart with wordline super-via and tall bitline contact.

2:50 PM

7-4 | Conflict-Free and Area-Efficient 4N4P CFET 8T SRAM with Double-Sided Signal Routing for Multibit Compute-in-Memory in AI Edge Devices, Yu-Cheng Lu, Graduate School of Advanced Technology, National Taiwan University, Taipei|Meng-Lin Wu, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei|Vita Pi-Ho Hu, Graduate School of Advanced Technology, National Taiwan University, Taipei, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei

As balanced N/P FETs is achieved in CFET structures, logic performance is enhanced. However, it exacerbates read/write conflicts in CFET 6T SRAM, causing a tighter threshold voltage design window, and complicating chip effective integration. This study proposes a conflict-free 4N4P CFET 8T SRAM with double-sided signal routing, avoiding tall vias and redundant transistors with the same cell area as CFET 6T SRAM. The 4N4P CFET 8T SRAM with balanced N/P FETs demonstrates improvement in RSNM, read/write time, read/write power, and logic speed/power. Additionally, with improved energy efficiency, the design supports simultaneous MAC computations for data-centric AI edge device applications.

3:40 PM

7-5 | A Multi-WL Approach to Suppress Gate-Induced Drain Leakage, Floating Body Effect, and Row Hammer Effect in Array Transistor of 4F2 DRAM and 3D Stackable DRAM, Wei-Chen Chen, Macronix International Co., Ltd|Hang-Ting Lue, Macronix International Co., Ltd|Ming-Hung Wu, Macronix International Co., Ltd|Xi-Wei Lin, Synopsys|Ko-Hsin Lee, Synopsys|Po-Chou Chen, Synopsys|Salvatore Amoroso, Synopsys|Keh-Chung Wang, Macronix International Co., Ltd|Chih-Yuan Lu, Macronix International Co., Ltd

We propose a multi-wordline (preferably 2-wordline) array transistor for 1T1C DRAM to minimize gate-induced drain leakage (GIDL), floating-body effect (FBE), and row hammer effect (RHE). This concept is applicable to both $4F^2$ and 3D stackable DRAM, addressing junction and gate work function processing challenges. By inserting an auxiliary gate near the storage node, we achieve a two-order magnitude reduction in GIDL and negligible FBE. Our work, supported by experimental data and 3D TCAD simulations, demonstrates significant suppression of GIDL, FBE, and RHE, essential for DRAM scaling in smaller cell capacitance regimes.

4:05 PM

7-6 | A Production Line Level MTJ Modeling Framework: Integrating Physical Mechanisms, Experimental Data and Manufacturing Variation, Zhizhong Zhang, Beihang University, Hangzhou International Innovation Institute|Kelian Lin, Beihang University|Kaihua Cao, Beihang University|Jinkai Wang, Beihang University|Jia Yang, Beihang University|Bojun Zhang, Beihang University|Hongchao Zhang, Truth Memory Corporation|Hongxi Liu, Truth Memory Corporation|Gefei Wang, Truth Memory Corporation|Weisheng Zhao, Beihang University, Hangzhou International Innovation Institute, Hangzhou International Innovation Institute|Yue Zhang, Beihang University

We propose for the first time a hybrid neural network-based magnetic tunnel junction (MTJ) modeling framework. By combining graph neural networks (GNN) and deep neural networks (DNN), we implement precise approximation of cross-level coupled physical processes in MTJs, while employing fine-tuning techniques to address discrepancies between experimental data and physical models. The extensive GNN backbone guarantees the scalability for different types of MTJs. Incorporated with stable diffusion (SD) model, this model can accurately predict the MTJ parameter distribution in manufacturing process. Our model framework not only achieves accuracy and scalability but also uniquely reproduces parameter variations in the production line.

4:30 PM

7-7 | An Experimentally Validated TCAD Variability study of The Relative Performance of In-Ga-Zn-O (IGZO) and Poly-Si-Channel Ferroelectric VNANDs, Mischa Thesberg, Global TCAD Solutions

GmbH|Zlatan Stanojevic, Global TCAD Solutions GmbH|Franz Schanovsky, Global TCAD Solutions GmbH|Jose-Maria Gonzalez-Medina, Global TCAD Solutions GmbH|Gerhard Rzepa, Global TCAD Solutions GmbH|Ferdinand Mitterbauer, Global TCAD Solutions GmbH|Oskar Baumgartner, Global TCAD Solutions GmbH|Markus Karner, Global TCAD Solutions GmbH

VNAND structures often suffer from performance issues related to the generally poor quality of their polycrystalline silicon (poly Si) channels. IGZO has been suggested as an alternative material. In this work TCAD models are developed that model the variability of polycrystalline silicon, amorphous IGZO and polycrystalline ferroelectric HfZrO2 (HZO) thin layers. All models are validated against experimental results and a complete parameter set for the variability model is given. The models are then used to assess the impact of selecting an IGZO-based device over a poly Si device on the memory window of a ferroelectric bit cell.

4:55 PM
7-8 | First large-scale (68x25x5 nm3) atomistic modeling for accurate and efficient etching process based on machine learning molecular dynamics (MLMD), Zemeng Feng, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Ziyi Hu, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Tong Yu, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Panpan Lai, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Rui Ge, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Hua Shao, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Dashan Shang, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Zhiqiang Li, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Kui Xu, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Junjie Li, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Rui Chen, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China|Ling Li, State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

Revealing the reaction mechanism in advanced device manufacturing is crucial for improving performance at nodes below 3 nm. We present the first large-scale atomistic model using machine learning molecular dynamics (MLMD) to simulate the lateral isotropic selective etching of SiO2/Si stacks in Gate-all-around field-effect transistors (GAAFET) within F* radical plasma. Constructed with a machine learning potential function and active learning, the simulation covers 68×25×5 nm³ (over 600,000 atoms), improving etching reaction trends by 4× and achieving a runtime of 4.75 hours (~150× faster than CMD). This framework enables atom-device multi-scale process modeling for Design Technology Co-optimization (DTCO).

Coffee break with Exhibitors
2:50 PM – 3:40 PM
Yosemite

Coffee break with Exhibitors

Monday Evening Reception
6:30 PM – 8:00 PM
Grand Ballroom B

11 | MT | Embedded Memories
9:00 AM – 12:00 PM, Grand Ballroom A
Co-Chairs: Johannes Mueller, Technology Lead STT-MRAM at GlobalFoundries and Zhiqiang Wei, Avalanche Technology

This session covers advancements in embedded memory solutions based on MRAM, FRAM, RRAM and PCM in scaled CMOS nodes. The session will be kicked-off by STM demonstrating a single-ended PCM reaching a cell size of only 0.019 µm2 in 28 nm FDSOI and will be followed by a record low footprint demonstration of CEA-LETIs 16kbit HZO-based FRAM in 22 nm FDSOI. SAMSUNG will be showcasing automotive technology readiness of its 14 nm FinFET embedded STT-MRAM solution and in a second paper will give further insight on the scaling challenges of its eMRAM technology towards single digit nanometer nodes. High speed and high endurance capabilities of embedded memories beyond NOR-FLASH-replacement will be highlighted by Beihang University with the demonstration of a 128kB SOT MRAM array. Finally, reliability enhancements of MBit-sized RRAM in 28 nm node will be presented by Tsinghua University.

9:00 AM
11-0 | Welcome

9:05 AM
11-1 | Best-In-Class density Single-Ended ePCM memory array for weight storage in edge-AI applications, Andrea Redaelli, STMicroelectronics, TR&D|Anna Gandolfo, STMicroelectronics, TR&D|Paolo Mattavelli, STMicroelectronics, TR&D|Fabio Bonfiglio, STMicroelectronics, TR&D|Jeremie Jasse, STMicroelectronics, TR&D|Luca Scotti, STMicroelectronics, TR&D|Giulia Samanni, STMicroelectronics, TR&D|Antonino Conte, STMicroelectronics, MDRF|Franck Arnaud, STMicroelectronics, TR&D|Christian Bocaccio, STMicroelectronics, TR&D|Giuseppe Desoli, STMicroelectronics, SRA|Roberto Annunziata, STMicroelectronics, TR&D

The enablement of a high-density memory array in a System on Chip (SoC) is a great opportunity to overcome the Von-Neuman bottleneck in computation, especially for applications at the edge. We will show that a dense array based on 0.019 μm^2PCM cell, embedded in 18nm FD-SOI CMOS process, typically operated in differential mode, can be operated in single-ended mode for effectively storing NNweights on a wide range of mission profiles. Differently from the differential approach, single-ended is less resilient to PCM reliability mechanisms, so proper algorithm and design optimizations have been carried out to provide a reliable behavior.

9:30 AM

11-2 | Hf0.5Zr0.5O2 FeRAM scalability demonstration at 22nm FDSOI node for embedded applications, Simon MARTIN, CEA-Leti|Carine JAHAN, CEA-Leti|Liam HOSIER, CEA-Leti|Fabien GRIMAUD, CEA-Leti|Mélanie LOURO, CEA-Leti|Julie LAGUERRE, CEA-Leti|Jean COIGNUS, CEA-Leti|William VANDENDAELE, CEA-Leti|Julien BORREL, CEA-Leti|Niccolo CASTELLANI, CEA-Leti|Valentina MELI, CEA-Leti|Jean ROTTNER, CEA-Leti|Christelle BOIXADERAS, CEA-Leti|Thomas MAGIS, CEA-Leti|Antonio ROMAN, CEA-Leti|Messaoud BEDJAOUI, CEA-Leti|Julien MERCIER, CEA-Leti|Stéphane MINORET, CEA-Leti|Catherine EUVRARD, CEA-Leti|Julian STURM, CEA-Leti|Sébastien KERDILES, CEA-Leti|Mathieu OPPRECHT, CEA-Leti|Corinne COMBOROURE, CEA-Leti|Aurélie SOUHAITE, CEA-Leti|Karine JULLIAN, CEA-Leti|Jorge Pablo NACENTA MENDIVIL, CEA-Leti|Tommaso GIAMMARIA, CEA-Leti|Ludovic COUTURE, CEA-Leti|Olivier GLORIEUX, CEA-Leti|Karim AZIZI-MOURIER, CEA-Leti|Thierry BILLON, CEA-Leti|Sophie DUMONT, CEA-Leti|Olivier GUILLER, CEA-Leti|Mehdi MOUHDACH, CEA-Leti|Adrien BLOT-SABY, CEA-Leti|Denys LY, CEA-Leti|Sébastien MARTINIE, CEA-Leti|Christelle CHARPIN-NICOLLE, CEA-Leti|François ANDRIEU, CEA-Leti|Olivier BILLOINT, CEA-Leti|Laurent GRENOUILLET, CEA-Leti

7nm HZO-based 2D ferroelectric capacitors (C_{2D}) down to 0.0028µm² area were successfully integrated in the 22nm FDSOI node BEOL, with 2.Pr>10µC/cm² and extrapolated endurance >10^{13}cycles. C_{2D} exhibit a strong layout-dependent 2.Pr, consistent with biaxial stress reduction. 16kbit 1T-1C_{2D} FeRAM were designed and fabricated to assess the memory window (MW) dependence with capacitor, transistor dimensions and operating voltages. 0 bitfail up to 10^{10}cycles is demonstrated at 2.4V, with median-MW>100mV. In order to reduce FeRAM bitcell footprint, 3D-based FeCap (C_{3D}) are also demonstrated, leading to 2.Pr up to 140µC/cm² (normalization by footprint) with projected 600mV median-MW at 1.5V for 0.047µm² 1T-1C_{3D} bitcell.

9:55 AM

11-3 | World-most energy-efficient 14nm automotive eMRAM technology for high-endurance applications, Tae Young Lee, Samsung Electronics|Jong Min Lee, Samsung Electronics|Young Wan Oh, Samsung Electronics|Hong-Hyun Kim, Samsung Electronics|Bae Seong Kwon, Samsung Electronics|Kazutaka Yamane, Samsung Electronics|Min Kwan Kim, Samsung Electronics|Pyung Hwa Jang, Samsung Electronics|Dong Kyu Lee, Samsung Electronics|Ho Jin Gwak, Samsung Electronics|Byung Kweon Jang, Samsung Electronics|Hyung Keun Gweon, Samsung Electronics|Ju Sung Oh, Samsung Electronics|Gwang Seok Yang, Samsung Electronics|Jae Hyeon Park, Samsung Electronics|Gi Woong Kwon, Samsung Electronics|Ju Hyun Kim, Samsung Electronics|Young Hyun Kim, Samsung Electronics|Jeong-Heon Park, Samsung Electronics|Jaechul Shim, Samsung Electronics|Jun Ho Park, Samsung Electronics|Woochang Lim, Samsung Electronics|Seungpil Ko Ko, Samsung Electronics|Hyun Jin Shin, Samsung Electronics|Yong Sung Ji, Samsung Electronics|So Hee Hwang, Samsung Electronics|Min Kwon Cho, Samsung Electronics|Kyung Tae Nam, Samsung Electronics|Bo Young Seo, Samsung Electronics|Kiseok Suh, Samsung Electronics|Shin Hee Han, Samsung Electronics|Yoon Jong Song, Samsung Electronics|Kangho Lee, Samsung Electronics|Ja-Hum Ku, Samsung Electronics

We present a 14nm automotive eMRAM technology with the world-best write energy of 10 pJ/bit and high endurance > 1E12 cycles. We have first enhanced eFlash-type eMRAM technology with endurance of 1E6 cycles, achieving sub-ppm bit error rates across all failure modes and reliable read/write operations up to 150˚C. Furthermore, we have improved switching efficiency of MTJ devices, achieving high endurance >

1E12 cycles while supporting automotive grade-1. Based on this technology, trading off retention with endurance would allow nearly unlimited endurance. This breakthrough marks a significant step toward the adoption of eMRAM in a wide range of applications.

10:45 AM

11-4 | Key Technologies of Scaling Embedded MRAM to 8nm Logic and Beyond for Automotive Application, Seungpil Ko, Samsung Electronics|JaeChul Shim, Samsung Electronics|JunHo Park, Samsung Electronics|Woochang Lim, Samsung Electronics|HYUNSUNG JUNG, Samsung Electronics|JUNGHOON BAK, Samsung Electronics|DAEEUN JEONG, Samsung Electronics|JAEWOOK Lee, Samsung Electronics|Hyunseok Whang, Samsung Electronics|Manjin Eom, Samsung Electronics|Dongwoo Shin, Samsung Electronics|JongHyuk Lee, Samsung Electronics|Seongcheol Noh, Samsung Electronics| Jaehak Yang, Samsung Electronics|Jeong-Heon Park, Samsung Electronics|YOUNGHYUN KIM, Samsung Electronics| Cheol Kim, Samsung Electronics|JUHYUN KIM, Samsung Electronics|TaeYoung Lee, Samsung Electronics|SHINHEE HAN, Samsung Electronics|Sohee Hwang, Samsung Electronics| Kangho Lee, Samsung Electronics|Sangjin Hyun, Samsung Electronics|Yoonjong Song, Samsung Electronics|SUJIN AHN, Samsung Electronics|Jaihyuk Song, Samsung Electronics

We demonstrate successful development of an embedded MRAM (eMRAM) for automotive applications compatible with the 8nm logic node. A yield of 90% was achieved at unit cell of 0.017μm^2, which is smallest in size as known to date. The full functionality of write and read operations at temperature in the range of -40°C to 150°C was achieved along with fulfilling reliability criteria necessary for automotive applications. We also successfully decreased the rate of short failure down to 0.5ppm within the scaled cell pitch. These results suggest that our innovative technology has the potential to be extended to 5nm eMRAM technology.

11:10 AM

11-5 | Demonstration of 128 Kb SOT-MRAM chip with 5 ns write and 15 ns read speed, high endurance over 1010 and low ECC-on bit error rate, Chuanpeng Jiang, Beihang University|Shiyang Lu, Beihang University|Zhongkui Zhang, Beihang University|Xiaofei Fan, Truth Memory Corporation|Danrong Xiong, Truth Memory Corporation|Jinhao Li, Beihang University|Hongxi Liu, Truth Memory Corporation|Gefei Wang, Truth Memory Corporation|He Zhang, Beihang University|Hui Jin, Beihang University|Kaihua Cao, Beihang University|Deming Zhang, Beihang University|Zhaohao Wang, Beihang University|Weisheng Zhao, Beihang University

We demonstration the128 Kb SOT-MRAM chipfeaturingthe high write/read speed of5/15ns, as well as the excellent endurance and retention benefiting from the integration process optimization. Moreover, we propose a multi-pulse write method tominimize the write failure.Finally, based on ECC, we succeed in a 0-bit-error-rate.

11:35 AM

11-6 | A 28nm 4Mb Embedded RRAM IP with Record-High Endurance of 107 Cycles and 10years@125°C Retention through Reliability-Enhanced Design-Technology Co-Optimization, Junyang Zhang, School of Integrated Circuits, Tsinghua University, Beijing, China|Xiangchao Ma, Beijing InnoMem Technologies Co., Ltd, China, School of Integrated Circuits, Tsinghua University, Beijing, China|Yue Xi, School of Integrated Circuits, Tsinghua University, Beijing, China|Yuyao Lu, School of

Integrated Circuits, Tsinghua University, Beijing, China|Kun Wang, Beijing InnoMem Technologies Co., Ltd, China|Hanyu Ren, Beijing InnoMem Technologies Co., Ltd, China|Jianshi Tang, School of Integrated Circuits, Tsinghua University, Beijing, China|Liyang Pan, School of Integrated Circuits, Tsinghua University, Beijing, China|Lei Chen, Beijing Microelectronics Technology Institute, China|Dong Wu, School of Integrated Circuits, Tsinghua University, Beijing, China|Bin Gao, School of Integrated Circuits, Tsinghua University, Beijing, China|He Qian, School of Integrated Circuits, Tsinghua University, Beijing, China|Huaqiang Wu, School of Integrated Circuits, Tsinghua University, Beijing, China

We implement a reliability-enhanced DTCO methodology encompassing multiple device and design innovations to address scaling challenges. This results in a highly reliable 28nm 4Mb embedded RRAM IP with 4 bits/cell MLC, 10^8 read disturb immunity, >10 years@125°C retention, and record-high endurance of 10^7 cycles at 6Kb sub-macro and 10^6 cycles at the chip level.

14 | Focus Session | Emerging Neural Interface Technologies for Human Interfacing
9:00 AM – 12:00 PM, Continental 4
Co-Chairs: Xiaoting Jia, Virginia Tech and Dion Khodagholy, UC-Irvine

This focus session on "Emerging Neural Interface Technologies for Human Interfacing" will highlight significant advancements and investments shaping the future of neurotechnologies. Our invited speakers will explore cutting-edge developments, including skin-inspired sensors and integrated circuits for wearables and implantables, flexible nanoelectronics for precise in vivo neural stimulation and recording, and the Neuropixels probe, a CMOS-based platform for large-scale brain-wide recording. The session will also cover a minimally invasive brain-machine interface system, novel materials for biocompatible soft neural interfaces, and the potential of organic electronics in treating neurological disorders. Overall, the session will emphasize the rapid progress in neural interface technologies and their potential to revolutionize human interfacing for both medical and technological applications.

9:00 AM
14-0 | Welcome

9:05 AM
14-1 | Skin-Inspired Sensors and Integrated Circuits for Wearables and Implantables (Invited), Zhenan Bao, Stanford University|Can Wu, Stanford University|Weicheng Wang, Stanford University|Donglai Zhong, Stanford University

Skin-inspired bioelectronic devices, composed of soft, stretchable materials, can form natural interfaces with the human body. This opens up a new paradigm for wearable and implantable systems, by enhancing conformability and biocompatibility with biological tissues. Much progress has been made to enhance their electrical performance and fabrication processes for practical applications. In this work, we describeourrecent developments in materials, microfabrication techniques, stretchable thin-film transistors, circuit designs,and system-level integrations.

9:30 AM
14-2 | Neuropixels probe: A 130nm/55nm CMOS-based integrated Multimodal Microsystems Technology Platform for large scale Brain Wide Recording (Invited), Barundeb Dutta, IMEC|Alexandru Andrei, IMEC|Hasan Mahmud-Ul, IMEC|Matt McDonald, IMEC|Pieter Neutens, IMEC|John O'Callaghan,

IMEC|Jan Putzeys, IMEC|Bogdan Raducanu, IMEC|Chutham Sawigun, IMEC|Enrico Tonon, IMEC|Xiaolin Yang, IMEC|Simone Severi, IMEC|Marleen Welkenhuysen, IMEC|Carolina Lopez, IMEC|Harrie Tilmans, IMEC

We report on the progress in multimodal high resolution integrated neural interfaces with a focus on the Neuropixels probes. Historically, the number of neurons recorded simultaneously follows a Moore's law like behavior, with numbers doubling every 6.7 years. Traditional approaches to probe fabrication have failed to meet the needs of scaling needs of neural recording. The Neuropixels platform, is a custom 130nm/55nm CMOS wafer scale process technology that enables electrode counts beyond the 1000's, enabling system level simultaneous recording of tens of thousands of neurons with single neuron spatial precision and millisecond timing resolution. This required the utilization of multilevel BEOL technology and integrating analog and digital circuitry with the electrode array, making it a standalone integrated electrophysiological micro-system. Recently, we have added a switchable two-color visible photonics module that enables cell specific stimulation and responsive electro-physiology using opto-genetics. In addition, we have added 3D-integration modules which allows die-to-wafer attachment and have extended the platform to the 55nm node to enable higher electrode and recording density. These enable the recording of 10,000 neurons in a chronic freely moving animal and 40,000 neurons in an acute headfixed set-up.

9:55 AM
14-3 | In vivo neural stimulation and recording using flexible nanoelectronics (Invited), Jia Liu, Harvard University|Ren Liu, Harvard University|Xinhe Zhang, Harvard University

In vivo neural stimulation and recording using flexible nanoelectronics

10:20 AM
14-4 | A high quality and minimal invasive interventional brain machine interface system based on neural spiking activities (Invited), Zhengtuo Zhao, Institute of Neuroscience, Center for Excellence in Brain Science and Intelligence Technology, Chinese Academy of Sciences|Xingzhao Wang, Institute of Neuroscience, Center for Excellence in Brain Science and Intelligence Technology, Chinese Academy of Sciences|Zhigang Yang, Zhongshan Hospital; Shanghai|Chi Ren, Institute of Neuroscience, Center for Excellence in Brain Science and Intelligence Technology, Chinese Academy of Sciences|Xue Li, Institute of Neuroscience, Center for Excellence in Brain Science and Intelligence Technology, Chinese Academy of Sciences

Intracranial neural electrodes have significantly contributed to research and clinical treatment, and recent endovascular neural interfaces offer minimally invasive approaches. However, these pioneering studies demonstrate the safety, but unable to resolve single-unit activity in large animal models or human patients, impeding a broader application as neural interfaces in clinical practice.We introduce anultraflexible microelectrode arraycapable of multi-channel single-unit recording in large animals with minimal invasiveness through a novel interventional implantation strategy.

11:10 AM

14-5 | Soft, Biocompatible and High-Performance Photo-Patternable Dielectrics for High-Density and Chronically Stable Brain-Electrode Interfaces (Invited), Foad Vashahi1,Hyunsu Park 1, Xian Gong 1, Anika Parekh1, Jia Liu2, Tianyang Ye 1, Paul Le Floch1, 1Axoft, Inc., 2Harvard University

Building high-density, chronically stable probes for tissue-wide neural interfaces is important to improve the efficacy of implantable brain-computer interfaces, discover neural biomarkers for diagnostic, and develop patient-specific neuromodulation therapies. Current state-of-the-art thin-film electronics rely on rigid materials with limited chronic biocompatibility, limiting the design of scalable neural interfaces. Here, we present soft, biocompatible, high-performance dielectric materials specifically designed to overcome the typical trade-off between bandwidth and stability in implantable neural interfaces

11:35 AM
14-6 | Time Domain-Based Oscillatory Feature Extraction for High Spatiotemporal Resolution Nerophysiologic Data (Invited), Jennifer Gelinas, Columbia University | Liang Ma, Columbia, University | Tristan Sands, Columbia University Irving | Dion Khodagholy, University of California Irvine

15 | EDT | Memory and Computing Enabled by Material Innovations
9:00 AM – 12:00 PM, Continental 5
Co-Chairs: Hyejung Choi, SK Hynix and Adrian Lonescu, EPFL

This session includes 6 papers that describe recent progress memory & computing enabled by material innovations. The first paper, by Jiahui Duan of University of Notre Dame, describes a robust and energy-efficient binary and MLC FeFET-based CiM design and experimental validation. Second paper is a invited contribution by Thomas Mikolajick of NaMLab gGmbH, Germany, discusses the recent developments both with respect to applications in standard semiconductor memories as well as emerging in-memory computing and neuromorphic computing applications. The third paper, by Shuhan Liu, Department of EE, Stanford University, propose a novel RRAM-Gain Cell joint memory to facilitate efficient continual learning in edge devices. The fourth paper, by Wei Shi, Department of Electrical and Computer Engineering, National University of Singapore, reports low Ec HZLO via La capping and intercalation and 2-layer stacked 1T1C FeRAM. The fifth paper, by Saketh Ram Mamidala of IBM Research Europe, presents the cryogenic characterization of read noise in 14 nm CMOS compatible analog resistive RAMs (ReRAMs) and evaluate the efficiency of analog in memory (AIM) neural network (NN) training. The last paper by Tao Chen, The Hong Kong University of Science and Technology, introduces a reconfigurable neurotransistor based on wide-bandgap (WBG) semiconductors with tunable nonlinear information processing and memory functions.

9:00 AM
15-0 | Welcome

9:05 AM
15-1 | Variation Tolerant and Energy-Efficient Charge Domain Compute-in-Memory Array with Binary and Multi-Level Cell Ferroelectric FET, Jiahui Duan, University of Notre Dame|Yixin Xu, Pennsylvania State University|Zijian Zhao, University of Notre Dame|Anni Lu, Georgia Institute of Technology|James Read, Georgia Institute of Technology|Mohsen Imani, University of California, Irvine|Thomas Kampfe, Fraunhofer IPMS|Mike Niemier, University of Notre Dame|Xiao Gong, National

University of Singapore|Shimeng Yu, Georgia Institute of Technology|Vijaykrishnan Narayanan, Pennsylvania State University|Kai Ni, University of Notre Dame

In this work, a robust and energy-efficient binary and MLC FeFET-based CiM design is presented by leveraging charge-domain computing. The functionality of binary MAC operations and MLC MAC operations are validated by cell-level and array-level experiments. Besides, the device variation study demonstrates that this design has much better resilience against device variation resilience than conventional current-domain CiM. The macro-level benchmarking also demonstrates that our design shows higher area efficiency and higher energy efficiency over prior CiM works.

9:30 AM
15-2 | Ferroelectric materials and their applications for next-generation integrated devices (Invited), Thomas Mikolajick, TU Dresden and NaMLab|Uwe Schroeder, NaMLab gGmbH|Patrick Lomenzo, NaMLab gGmbH|Stefan Slesazeck, NaMLab gGmbH|Suzanne Lancaster, NaMLab gGmbH

Ferroelectric materials have great potential for applications in information technology. With the discovery of ferroelectricity in semiconductor process-compatible materials, the activities in both research and industry to drive ferroelectric functionalities toward commercialization have exploded. This paper will discuss the recent developments both with respect to applications in standard semiconductor memories as well as emerging in-memory computing and neuromorphic computing applications.

9:55 AM
15-3 | Edge Continual Training and Inference with RRAM-Gain Cell Memory Integrated on Si CMOS, Shuhan Liu, Stanford University|Robert Radway, Stanford University|Xinxin Wang, Stanford University|Filippo MORO , CEA-Leti|Jean-François NODIN, CEA-Leti|Koustav Jana, Stanford University|Shuting Du, Purdue University|Luke Upton, Stanford University|Wei-Chen Chen, Stanford University|Jian Chen, Stanford University|Haitong Li, Purdue University|Francois ANDRIEU, CEA-Leti|Elisa VIANELLO, CEA-Leti|Priyanka Raina, Stanford University|Subhasish Mitra, Stanford University|H.-S. Philip Wong, Stanford University

This research presents the design and experimental validation of a novel RRAM-Gain Cell joint memory. HfO2 RRAM and ITO gain-cell are monolithically integrated on 130nm Si CMOS, enabling high-speed training and low-standby-power inference for edge devices. High-bandwidth on-chip data transfer can have bandwidth that is 90× state-of-the-art HBM3E and 211× PCIe7.0, enabled by high-density monolithic-3D interconnections and high-speed transfer circuits. The ALD-ITO-FET exhibits positive VTH 0.67V, excellent SS 65mV/dec, high on-current 20μA/μm, and low off-current 5×10-18A/μm, as extracted from >5,000s retention. The joint memory macro consumes 78% less standby power and 95% less training energy for MobileBERT compared to SRAM.

10:20 AM
15-4 | Record-Low Coercive Field in ALD-Grown HZO Ferroelectric Films: Enabling Ultra-low Operation Voltage in World's First 2-Layer 3D Stacked Oxide Semiconductor 1T1C FeRAM, Wei Shi, National University of Singapore|Dong Zhang , National University of Singapore|Zijie Zheng, National University of Singapore|Zuopu Zhou, National University of Singapore|Kaizhen Han, National University of Singapore|Chen Sun, National University of Singapore|Qiwen Kong, National University of Singapore|Yang Feng, National University of Singapore|Xiao Gong, National University of Singapore

Record-low coercive field (E_c) of ~0.78 MV/cm has been achieved in this work for ALD-grown HZO-based ferroelectric (FE) thin films without sacrificing remnant polarization ($2P_r$ > 40 μC/cm²). With the assist from extensive material and electrical characterizations, oxygen vacancy (V_o) control and grain size reduction are disclosed as the key factors for E_c optimization. Additionally, we demonstrated the world's first stacked 1T1C FeRAM comprising two active layers by leveraging oxide semiconductor channel access transistors. A ultra-low operation voltage of ~1.2 V has been achieved for FE switching owing to the carefully developed FE film growth.

11:10 AM
15-5 | Cryogenic Analog 1T-ReRAM with Enhanced Dynamic Range and Suppressed Noise for Cold Neural Networks, Saketh Ram Mamidala, IBM Research Europe - Zurich|Davide Lombardo, IBM Research Europe - Zurich|Elisa Zaccaria, IBM Research Europe - Zurich|Donato Falcone, IBM Research Europe - Zurich|Tommaso Stecconi , IBM Research Europe - Zurich|Antonio La Porta, IBM Research Europe - Zurich|Marilyne Sousa, IBM Research Europe - Zurich|Steffen Reidt, IBM Research Europe - Zurich|Alberto Ferraris, IBM Research Europe - Zurich|Cezar Zota, IBM Research Europe - Zurich|Valeria Bragaglia, IBM Research Europe - Zurich|Bert Jan Offrein, IBM Research Europe - Zurich

We present the first cryogenic characterization of read-noise in 14-nm CMOS-compatible analog ReRAMs and evaluate the efficiency of analog-in-memory neural network (NN) training at 77K using the optimized Tiki-Taka algorithm (*TT*v2). Compared to standard room temperature operation, cryogenic operation suppresses the read noise by an exceptional 88% and improves the dynamic range by 2200%. The effectiveness of cryo-ReRAMs in training NNs is validated by simulations using *TT*v2 on handwritten digits yielding an accuracy of 96.5%, the highest reported to date for non-volatile memories at cryogenic temperatures. The results highlight the potential for cryo-ReRAMs in power-constrained applications such as quantum computing.

11:35 AM
15-6 | Reconfigurable Neurotransistors Based on Wide-bandgap Semiconductors for Adaptive Reservoir Computing, Tao Chen, The Hong Kong University of Science and Technology|Zheyang Zheng, The Hong Kong University of Science and Technology, University of Science and Technology of China|Sirui Feng, The Hong Kong University of Science and Technology|Li Zhang, The Hong Kong University of Science and Technology|Yan Cheng, The Hong Kong University of Science and Technology|Yat Hon Ng, The Hong Kong University of Science and Technology|Kevin Chen, The Hong Kong University of Science and Technology

We demonstrate a reconfigurable neurotransistor based on wide-bandgap semiconductors with tunable information processing and memory functions for physical reservoir computing (RC). The neurotransistor, based on gallium nitride (GaN), can be configured as volatile memory (VM) or non-volatile memory (NVM). As a VM, the device can perform adaptive information processing with gate-tunable nonlinear functions and short-term memory. As an NVM, it features multi-state storage with fast and linear weight updating, long retention time, and high endurance. We utilize the GaN-based neurotransistor to demonstrate a highly adaptive RC system with enriched nonlinear dynamics and tunable temporal responses for long-term temporal signal processing.

17 | MS | Selector-Only Memory and Ferroelectric Devices

9:00 AM – 12:00 PM, Continental 7 – 9
Co-Chairs: Tzu-Hsuan (Bruce) Hsu, Macronix and Tzer-Min Shen, TSMC

This session includes six papers that discuss selector-only memories (SOM) and ferroelectric memories. The first paper, by Ha-Jun Sung et al. from Samsung, is highlighted for introducing material screening methods for SOM using machine learning and ab initio simulations. The second paper, by S. Clima et al. from IMEC, provides insights into the operation mechanism of SOM through ab initio simulations. The third paper, by Zhouhang Jiang from the University of Notre Dame and Yi Xiao from Pennsylvania State University, demonstrates the floating body effect of FeFET in 3D NAND application. The fourth paper, by Xiaolin Wang from the National University of Singapore and Zijie Zheng from Soitec, addresses the dynamic characteristics modeling of FeFET. The fifth paper, by Leming Jiao and Zuopu Zhou from the National University of Singapore presents new insights and models of the switching dynamic of HfO2-based ferroelectric materials. The final paper, by Shan Deng from the University of Notre Dame and Yi Xiao from Pennsylvania State University, demonstrates the scalability of high-density 3D NAND using 2T-nC FeRAM.

09:00 AM
17-0 | Welcome

09:05 AM
17-1 | Ab-initio Screening of Amorphous Chalcogenides for Selector-Only Memory (SOM) through Electrical Properties and Device Reliability, Ha-Jun Sung, Samsung Electronics|Minwoo Choi, Samsung Electronics|Youngjae Kang, Samsung Electronics|Kiyeon Yang, Samsung Electronics|Bonwon Koo, Samsung Electronics|Wu Zhe, Samsung Electronics|Hwasung Chae, Samsung Electronics|Chang Seung Lee, Samsung Electronics

Amorphous chalcogenides for SOM applications have traditionally been limited to the Ge, As, and Se systems used in OTS selectors. In this study, we systematically performed Ab-initio-based screening of ternary amorphous chalcogenide materials suitable for SOM for the first time. We investigated the memory window mechanism and key parameters affecting VTH drift to establish screening criteria. The trade-off relationship between the memory window and VTH drift allows for modifications through compositional control and additional doping. Consequently, we identified 18 promising candidates out of 3888 samples for future 3D X-point memory.

09:30 AM
17-2 | Selector Only Memory: Exploring Atomic Mechanisms from First-Principles, Sergiu Clima, imec|Fabian Ducry, imec|Daniele Garbin, imec|Taras Ravsher, imec, KULeuven|Robin Degraeve , imec|Attilio Belmonte, imec|Gouri Sankar Kar, imec|Geoffrey Pourtois , imec

The recent attention to Ovonic threshold switching (OTS) materials is owed to the development of the so-called selector-only memory (SOM) concept. *Understanding the SOM switching mechanism at the atomic scale* is required to facilitate device optimization. With first-principles simulations, we identify *two possible atomistic mechanisms leading to mobility gap changes and hence threshold voltage modulation*, which determines the memory window (MW) of SOM: *i) local atomic bond rearrangement* or *ii) atomic segregation*, depending on the operating conditions. Our findings provide an atomic-level perspective that confirms *previous high-level modelling assertions* about the working principles of OTS and SOM.

09:55 AM

17-3 | On the Origin of Holes During Polarization Reset in Floating Body Ferroelectric FETs Towards Improving Switching Efficiency, Zhouhang Jiang, University of Notre Dame|Yi Xiao, Pennsylvania State University|Milind Weling, EMD group|Halid Mulaosmanovic, GlobalFoundries Fab1 LLC & Co. KG|Stefan Duenkel, GlobalFoundries Fab1 LLC & Co. KG|Dominik Kleimaier, GlobalFoundries Fab1 LLC & Co. KG|Steven Soss, GlobalFoundries Fab1 LLC & Co. KG|Sven Beyer, GlobalFoundries Fab1 LLC & Co. KG|Rajiv Joshi, IBM Thomas J. Watson Research Center|Mohamed Mohamed, MIT Lincoln Laboratory|Scott Meninger, MIT Lincoln Laboratory|Xiao Gong, National University of Singapore|Vijaykrishnan Narayanan, Pennsylvania State University|Kai Ni, University of Notre Dame
Speakers: Shubham Kumar

In this work, we performed a comprehensive combined experimental and modeling study on the polarization reset mechanisms of floating body (i.e., channel) ferroelectric FETs, an important class of device with growing interests due to added functionalities and improved reliabilities. Using fully-depleted silicon-on-insulator (FDSOI) FeFET as a classical example, we demonstrate that: 1) without hole generation mechanisms, floating body FeFETs during reset is simply a capacitor divider, with negligible ferroelectric voltage drop for switching; ii) Band-to-band-tunneling (BTBT) around gate-to-S/D overlap even with zero drain bias generates holes to facilitate the reset in FDSOI FeFET, though at a slower speed and hold

10:45 AM

17-4 | Unveiling the Intricate Dynamic Charactristics of FeFETs with a MFMIS Structure: Experiment and Modeling, Xiaolin Wang, National University of Singapore (NUS)|Zijie Zheng, NUS|Leming Jiao, NUS|Xuanqi Chen, NUS|Yang Feng, NUS|Chen Sun, NUS|Zuopu Zhou, NUS|Dong Zhang, NUS|Gan Liu, NUS|Bich-Yen Nguyen, Soitec|Gengchiau Liang, NUS|Kai Ni, University of Notre Dame|Xiao Gong, NUS

A dynamic model is established to gain deep insights into the operation mechanisms and predict the performance of the FeFETs under various operation speeds employing a metal-ferroelectric (FE)-metal-insulator-semiconductor (MFMIS) structure. Empowered by extensive experimental calibration and in-depth analysis based on our IGZO FeFETs with a MFMIS structure, for the first time, several key findings are unveiled Motivated and inspired by these discoveries, we propose three effective strategies to improve the dynamic performance of the MFMIS FeFETs: thickness engineering of FE and insulator layers, and aggressive device down-scaling. These approaches are substantiated by both simulation analysis and experimental validation.

11:10 AM

17-5 | First Observation of the Temperature-Dependent Two-phase Switching of the HfO2-based Ferroelectric Polarization: New Insights and Modeling of the Switching Dynamics, Leming Jiao, National University of Singapore|Zuopu Zhou, National University of Singapore|Zijie Zheng, National University of Singapore|Xiaolin Wang, National University of Singapore|Jiawei Xie, National University of Singapore|Dong Zhang, National University of Singapore|Qiwen Kong, National University of Singapore|Gengchiau Liang, National Yang-Ming Chiao Tung University|Xiao Gong, National University of Singapore

For the first time, we report the observation of the intrinsic two-phase switching of the FE capacitors. Through the temperature dependence measurement of the ΔP_{FE}-t from 300 K to 10 K, mechanisms behind the switching dynamics are revealed, involving the short-term direct switching and the long-term accumulative switching, which effectively explains the measured different polarization increasing trends in the two time periods. Furthermore, we develop a two-phase switching model which reproduces the new observations across a broad range of temperatures by appropriately incorporating the free energy equation and the thermal-related distribution function.

11:35 AM

17-6 | First Demonstration of Vertical 2T-nC FeRAM Hybrid Cell and Its Scalability for High-Density 3D Ferroelectric Capacitor Memory, Shan Deng, University of Notre Dame|Yi Xiao, Pennsylvania State University|Zhouhang Jiang, University of Notre Dame|Yixin Qin, University of Notre Dame|Renzheng Zhang, University of Notre Dame|Zijian Zhao, University of Notre Dame|John Howe, University of Notre Dame|Yushan Lee, University of Notre Dame|Jiahui Duan, University of Notre Dame|Rajiv Joshi, IBM Thomas J. Watson Research Center|Thomas Kämpfe, Fraunhofer IPMS|Tengfei Luo, University of Notre Dame|Tuo-Hung Hou, National Yang Ming Chiao Tung University|Xiao Gong, National University of Singapore|Vijaykrishnan Narayanan, Pennsylvania State University|Kai Ni, University of Notre Dame

We perform a comprehensiveexperimental and modeling study into the scaling ofvertical 2T-nC ferroelectric random-access memory(FeRAM) hybrid cell to demonstrate a high performanceand high-density 3D capacitor memory. We demonstrate:i) first time successful integration of the vertical 2T-3CFeRAM cell; ii)successful experimental operation of the memory cell; iii)the write bit line (WBL) heavily screens the couplingbetween neighboring strings;iv) aggressive stacking of the WBLs could facilitate the self-boosting during writeoperation due to ferroelectric linear capacitance; v) aggressive horizontal scaling significantly increases the read disturb to cells on neighboring planesdue to capacitance between WBLs.

12 | ALT | Alternative Channel Material Devices
9:00 AM – 12:25 PM, Grand Ballroom B
Co-Chairs: Daphnée Bosch, CEA-Leti and Paul Grudowski, NXP

This session with seven papers highlights recent advances in alternative channel materials and 3D-stacked devices, including Amorphous Oxide Semiconductors (AOS) for their BEOL-compatibility and 2D Transition Metal Dichalcogenides (TMDs) for their beneficial electrostatic properties. The first paper from Georgia Institute of Technology highlights a Gate-All-Around integration with a W-doped In2O3 channel with very high performance and good threshold voltage control. The next paper from Purdue University demonstrates for the time a CFET with IGZO NFET on Te PFET, creating a functional logic inverter. In the third paper, Huawei reveals a 6nm channel thickness Vertical GAA IGZO FET with extremely small 28nm contact CD length. The fourth paper from imec presents an MoS2-based 2D TMD GAA Nanosheet FET with exceptional drive current, Ion/Ioff ratio, and yield. In the fifth paper, TSMC reports the integration aspects of WSe2 and MoS2-based GAA Nanosheet and CFET devices, with special emphasis on the nanosheet release process among other innovations. In their second paper of this session, Purdue focuses on controlling the unique negative Schottky barrier characteristics of In2O3 FET contacts through quantum confinement. The final paper in this session from the National University of Singapore presents a unique combination of an ITO FET and Ferroelectric capacitor to create a novel BEOL-compatible NV-SRAM solution.

09:00 AM
12-0 | Welcome

09:05 AM
12-1 | First Demonstration of W-doped In2O3 Gate-All-Around (GAA) Nanosheet FET with Improved Performance and Record Threshold Voltage Stability, Eknath Sarkar, Georgia Institute Of Technology|Chengyang Zhang, Georgia Institute Of Technology|Dyutimoy Chakraborty, Georgia Institute Of Technology|Faaiq G Waqar, Georgia Institute Of Technology|Sharadindugopal Kirtania, Georgia Institute Of Technology|Khandker Akif Aabrar, Georgia Institute Of Technology|Hyeonwoo Park, Georgia Institute Of Technology|Jaewon Shin, Georgia Institute Of Technology|Mengkun Tian, Georgia Institute Of Technology|Asif I Khan, Georgia Institute Of Technology|Shimeng Yu, Georgia Institute Of Technology|Suman Datta, Georgia Institute Of Technology

We demonstrate a gate-all-around (GAA) nanosheet FET using an atomic layer deposited (ALD) tungsten (W) In_2O_3or IWO channel. We developed a novel channel release process with a metal sacrificial layer (SL), that enables lithography-independent definition of the device channel length (L_{Ch}). The fabricated nanosheet FETs with scaled dimensions of L_{Ch}=50nm and $W_{Nanoseet}$=30nm demonstrate high on-state current (I_{ON}) of 815 μA/μm for V_{DD}=1V,V_G-V_T=3.5V with an off-state current (I_{OFF}) of 4 nA/um at V_G=V_T-1V. These GAA nanosheet IWO FETs showcase record high bias stress stability with threshold voltage (V_T) shift of only 88mV for stress voltage V_G-V_T=2.6V (stress field, E_{OX}=V_{OV}/EOT=22 MV/cm).

09:30 AM
12-2 | First Demonstration of BEOL Wafer-Scale All-ALD Channel CFETs Using IGZO and Te for Monolithic 3D Integration, Chang Niu, Purdue University|Pukun Tan, Purdue University|Jian-Yu Lin, Purdue University|Linjia Long, Purdue University|Zehao Lin, Purdue University|Yizhi Zhang, Purdue University|Haiyan Wang, Purdue University|Glen Wilk, ASM|Peide Ye, Purdue University

We demonstrate the first BEOL-compatible, wafer-scale, all-ALD-channel CFETs by stacking a novel TeOx/Te p-type transistor on an IGZO n-type transistor with a common gate. The ALD-CFET inverter exhibits excellent electrical performance, achieving 116.5V/V gain and 2.2V (88%) noise margin, offering a new approach for BEOL CMOS monolithic 3D integration.

09:55 AM
12-3 | High-performance Vertical Gate-All-Around Oxide Semiconductor Transistors with 6 nm ALD IGZO Channel and Scaled Contact CD down to 28 nm, Kishou Kaneko, Huawei Technologies Japan K.K., Japan|Wanpeng Zhao, Huawei Technologies Co., LTD., China|Wei Cui, Huawei Technologies Co., LTD., China|Lu Kang, Huawei Technologies Co., LTD., China|Shiheng Lu, Huawei Technologies Co., LTD., China|Wenqiang Yuan, Huawei Technologies Co., LTD., China|Heng Wang, Huawei Technologies Co., LTD., China|Shijie Zhan, Huawei Technologies Co., LTD., China|Yuqi Wang, Huawei Technologies Co., LTD., China|Yibiao Yin, Huawei Technologies Co., LTD., China|Lijuan Xing, Huawei Technologies Co., LTD., China|Xia Sang, Huawei Technologies Co., LTD., China|Yuan Shao, Huawei Technologies Co., LTD., China|Zebin Lin, Huawei Technologies Co., LTD., China|Hongguang Shen, Huawei Technologies Co., LTD., China|Xiaojuan Cui, Huawei Technologies Co., LTD., China|Ying Wu, Huawei Technologies Co., LTD., China|Jeffrey Xu, Huawei Technologies Co., LTD., China

Vertical IGZO FETs are demonstrated on an 8-inch platform with a thin IGZO channel of 6 nm and a short gate length of 48 nm. The device exhibits a high I_{ON} of 111.4 μA/μm @ V_{DS}= 1.5 V, V_{GS}= 2 V with scaled source/drain (SD) contact CD of 40 nm, a positive threshold voltage (V_{TH}) of 0.13 V, and a low SS of 75 mV/dec. Excellent bias temperature stability (BTS) are obtained with optimized gate stack, showing a small VTHshift (ΔV_{TH}) of ± 3 mV after stressing 1k seconds under V_{GS}= ± 2 V.

10:45 AM

12-4 | High-performance Monolayer-2D Stacked Nanosheet FETs with high ION ~ 451 μA/μm and ION/IOFF > 109, Fengben Xi, imec|Himanshu Sharma, imec|Xiangyu Wu, imec|Devin Verreck, imec|Daire Cott, imec|Robert Grubbs, imec|Tien Ngo, imec|Pawan Kumar, imec|Pierre Morin, imec|Benjamin Groven, imec|Jean-Francois Marneffe, imec|Dennis Dorp, imec, imec|Souvik Ghosh, imec|Zaoyang Lin, imec|Ankit Mehta, imec|Zhuo Chen, imec|Surajit Sutar, imec|Tom Schram, imec|Quentin Smets, imec|Dennis Lin, imec|Kaustuv Banerjee, imec|Cesar Rosa, imec|Ludovic Goux, imec|Gouri Kar, imec

Stacked nanosheet FETs with the monolayer MoS_2 channels are presented. At a channel length of 40 nm, the transistor with two-tiers monolayer MoS_2, exhibits a remarkable I_{ON} ~ 451 μA/μm, a record I_{ON}/I_{OFF}> 10^9 at V_{DS} = 1 V, and a yield of 96.59%, showing good electrostatic control ability.

11:10 AM

12-5 | Stacked Channel Transistors with 2D Materials: an Integration Perspective, Yun-Yan Chung, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Bo-Jhih Chou, Institute of Electronics National Yang Ming Chiao Tung University, Hsinchu, Taiwan, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Wei-Sheng Yun, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Chen-Feng Hsu, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Shao-Ming Yu, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Yu-I Chang, Institute of Electronics National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Chen-Yi Lee, Institute of Electronics National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Sui-An Chou, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Po-Hsun Ho, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Aslan Wei, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|D. Mahaveer Sathaiya, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Bo-Heng Liu, Taiwan Instrument Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan|Chien-Wei Chen, Taiwan Instrument Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan|Chien-Ying Su, Taiwan Instrument Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan|Chi-Chung Kei, Taiwan Instrument Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan|Fu-Kuo Hsueh, Taiwan Semiconductor Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan.|Tuo-Hung Hou, Taiwan Semiconductor Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan., Institute of Electronics National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Wen-Hao Chang, Department of Electrophysics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Jin Cai, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Chung-Cheng Wu, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Jeff Wu, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Wei-Yen Woon, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Tung-Ying Lee, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Chao-Hsin Chien, Institute of Electronics National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Chao-Ching Cheng, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan|Iuliana Radu, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

The first electrical demonstration of a stacked nanosheet (NS) FET with a monolayer MoS2 channel, utilizing a typical nanosheet release process prior to high-k metal gate deposition. A flat, two-stacked nanosheets with 1-MoS2 channel and HfOX/TiN gate stack is demonstrated. IMAX/IMIN ratios of ~1E5 and a subthreshold swing of ~220 mV/dec are reported. Additionally, for the first time, the integration of stacked two NS WSe2 and two NS MoS2 in the same structural FET is demonstrated using the NS release and HKMG conformal deposition process. The two channel materials represent typical PMOS and NMOS 2D materials, respectively.

11:35 AM
12-6 | Quantum Confinement Controlled Positive to Negative Schottky Barrier Conversion in Ultrathin In2O3 Transistor Contacts, Jian-Yu Lin, Purdue University|Chang Niu, Purdue University|Zehao Lin, Purdue University|Taehyun Kim, Ulsan National Institute of Science and Technology|Beomjin Park, Ulsan National Institute of Science and Technology|Hyeongjun Jang, Ulsan National Institute of Science and Technology|Changwook Jeong, Ulsan National Institute of Science and Technology|Peide D. Ye, Purdue University

In this work, we study quantum-confinement and Fermi-level-pinning effects on the Schottky-barrier-height of ultrathin In_2O_3 transistors for the first time. A positive-to-negative Schottky-barrier-height conversion can be tuned by In_2O_3 thickness. Fermi-level-pinning study reveals In_2O_3 as a unique material with pinned negative-Schottky-barrier-height, leading to ultra-low contact resistance and resistivity.

12:00 PM
12-7 | First Demonstration of BEOL-Compatible NV-SRAM Featuring Vertically Stacked ITO FETs and HfO2-based Ferroelectric Capacitors for High Density Monolithic 3D Integration, Zuopu Zhou, National University of Singapore|Jiawei Xie, National University of Singapore|Leming Jiao, National University of Singapore|Kaizhen Han, National University of Singapore|Yuye Kang, National University of Singapore|Zijie Zheng, National University of Singapore|Qiwen Kong, National University of Singapore|Xiaolin Wang, National University of Singapore|Bich-Yen Nguyen, Soitec|Xiao Gong, National University of Singapore

For the first time, we experimentally demonstrated a BEOL-compatible non-volatile SRAM (NV-SRAM), utilizing HfO2-based MFM capacitors to provide non-volatility and ITO channel FETs to enhance the integration density. Ideal for 3D vertical stacking above silicon CMOS circuits, our NV-SRAM operates effectively with low power (VDD of 1.5 V and PL voltage of 2 V) and offers high density and bandwidth. Evaluations including SPICE simulations of the ultra-short channel ITO FETs underscore the substantial promise of NV-SRAM for data-centric computing.

13 | NC | Emerging Compute-In-Memory Hardware
9:00 AM – 12:25 PM, Continental 1 – 3
Co-Chairs: Giuseppe Desoli, STMicroelectronics and Hidehiro Fujiwara, TSMC

The session addresses innovative Compute-In-Memory (CIM) devices and architectures, the first paper presents a novel approach using memristor technology leveraging sneak current paths to represent graphlets structures and implements a random walk method by way of stochastic variations in memristor switching; the second paper presents a Phase-Change Memory (PCM) based CIM architecture for manifold learning, incorporating adaptive drift compensation to enhance accuracy, the architecture

employs a dual-core implementation on a 40nm chip die, with separate computing and compensation arrays performing vector-matrix multiplication (VMM) operations and true random number generation. The third paper demonstrates a time-continuous and analog score-based diffusion model using the RRAM-based in-memory neural differential equation solver paving the way for more advanced generative AI applications. The fourth paper presents the implementation of the forward-forward learning rule in RRAM-based CIM proposing several adaptations to address implementation concerns related to noisy devices, last layer learning, and weight updates. The fifth paper introduces a filament-free, multi-level b-RRAM with improved retention and endurance applying it to a neuro-inspired few-shot learning algorithm, showing improved learning accuracy in simulations. The sixth paper proposes capacitive coupling voltage sense amplifiers for STT-MRAM based memories leveraging the inherent error tolerance in deep learning networks to reduce read energy during sensing, reducing Bit Error Rate (BER) degradation and demonstrate error tolerance across int8 and fp8 models. The last paper of the session experimentally demonstrates a 4k CMOS-compatible short-channel V-ECRAM cross-point array showing superior synaptic characteristics, including linearity, on/off ratio, switching speed, and endurance for an analog CIM implementation.

9:00 AM
13-0 | Welcome

9:05 AM
13-1 | Graphlet Decomposition using Random-Walk Memristors, Kyung Seok Woo, Sandia National Laboratories, Texas A&M University|Nestor Ghenzi, Seoul National University|A. Alec Talin, Sandia National Laboratories|Hyungjun Park, Seoul National University|Sangheon Oh, Sandia National Laboratories|Cheol Seong Hwang, Seoul National University|R. Stanley Williams, Sandia National Laboratories, Texas A&M University|Suhas Kumar, Sandia National Laboratories

Although memristor crossbars are a promising post-CMOS solution for computing, sneak currents and stochastic switching are two persistent challenges that impede their practical implementation. Here, we show how both issues can, in fact, be taken advantage for graphlet decomposition and analysis.

09:30 AM
13-2 | Neural Manifold Learning Based on 40nm Dual-Mode PCM Compute-in-Memory Chip with Hardware Adaptive Drift Compensation, Longhao Yan, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Yuqi Li, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Xi Li, State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences|Zelun Pan, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Zeyu Wang, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Xile Wang, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Bowen Wang, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Zhe Zhan, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Xiyuan Tang, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University, Center for Brain Inspired Chips, Institute of Artificial Intelligence, Peking University|Yaoyu Tao, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University, Center for Brain Inspired Chips, Institute of Artificial

Intelligence, Peking University|Woo-Ping Ge, Center for Brain Inspired Intelligence, Chinese Institute for Brain Research (CIBR)|Zhitang Song, State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences|Ru Huang, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University|Yuchao Yang, Beijing Advanced Innovation Center for Integrated Circuits, School of Integrated Circuits, Peking University, Center for Brain Inspired Intelligence, Chinese Institute for Brain Research (CIBR), Center for Brain Inspired Chips, Institute of Artificial Intelligence, Peking University, Guangdong Provincial Key Laboratory of In-Memory Computing Chips, School of Electronic and Computer Engineering, Peking University

Neural manifold learning (NML), as a significant research topic in the field of neuroscience, plays a vital role in the realization of intelligent edge brain-computer interface (BCI). Here, we design a 288Kb dual-mode phase change memory (PCM) compute-in-memory chip and utilize its two cores for two fundamental operators in NML to develop a PCM-based NML system. In particular, in order to mitigate system performance degradation caused by PCM conductance drift, we feature a novel adaptive-PCM-drift-compensation scheme that significantly improves the accuracy of VMM results. This work improves the computing energy efficiency and throughput by 476× and computing throughput 264× respectively.

09:55 AM
13-3 | Conditional Diffusion Model Acceleration with First-Demonstrated RRAM-based In-memory Neural Differential Equation Solver, Jichang Yang, The University of Hong Kong|Hegan Chen, The University of Hong Kong, AI Chip Center for Emerging Smart Systems|Jia Chen, AI Chip Center for Emerging Smart Systems|Songqi Wang, The University of Hong Kong|Shaocong Wang, The University of Hong Kong|Yifei Yu, The University of Hong Kong|Bo Wang, The University of Hong Kong|Ning Lin, The University of Hong Kong|Xinyuan Zhang, The University of Hong Kong|Rui Chen, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, University of Chinese Academy of Sciences|Zhongrui Wang, The University of Hong Kong, AI Chip Center for Emerging Smart Systems|Dashan Shang, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, University of Chinese Academy of Sciences|Han Wang, The University of Hong Kong|Qi Liu, Fudan University|Ming Liu, Fudan University, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences

Score-based diffusion models generate by solving neural differential equations. However, their digital computer implementations are discrete in time and inherently digital, with energy efficiency constrained by the von Neumann architecture. Herein, we firstly demonstrate a chip-level solution that embodies the implementation of time-continuous and analog conditional score-based diffusion using a RRAM in-memory neural differential equation solver. Notably, the diffusion process is intrinsically robust to analog noise. Under equivalent generation quality, our system achieves 0.02msgeneration time(software baseline 3ms) and 7.2uJenergy consumption (software baseline 22.5uJ) per sample, denoting x150 enhancement on generation speed and 68% reduction on energy consumption.

10:20 AM
13 | Break

10:45 AM

13-4 | Forward-Forward Learning Exploiting Low-Voltage Reset of RRAM, Bastien Imbert, Aix-Marseille Univ., CNRS|Adrien Renaudineau, Univ. Paris-Saclay, CNRS|Mamadou Hawa Diallo, Aix-Marseille Univ., CNRS|Jorge-Daniel Aguirre-Morales, Aix-Marseille Univ., CNRS|Mohammed Akib Iftakher, Univ. Paris-Saclay, CNRS|Kamel-Eddine Harabi, Univ. Paris-Saclay, CNRS|Clément Turck, Univ. Paris-Saclay, CNRS|Marie Drouhin, Univ. Paris-Saclay, CNRS|Tifenn Hirtzlin, CEA-Leti|Elisa Vianello, CEA-Leti|Jean-Michel Portal, Aix-Marseille Univ., CNRS|Marc Bocquet, Aix-Marseille Univ., CNRS|Damien Querlioz, Univ. Paris-Saclay, CNRS

This paper presents the first adaptation of the Forward-Forward algorithm for resistive memory. Using RRAM in the low-voltage RESET regime and by co-optimizing device programming conditions and algorithm, we achieve accurate heartbeat classification, with important benefits in energy efficiency, endurance, and device retention.

11:10 AM
13-5 | Filament-free Bulk RRAM with High Endurance and Long Retention for Neuromorphic Few-Shot Learning On-Chip, Ashwani Kumar, UC San Diego|Yucheng Zhou, UC San Diego|Sai Praneeth Potladurthy, UC San Diego|Jeong-Hoon Kim, UC San Diego|Weihong Xu, UC San Diego|Flavio Ponzina, UC San Diego|Seonghyun Kim, SK Hynix|Ertugrul Cubukcu, UC San Diego|Tajana Rosing, UC San Diego, UC San Diego|Gert Cauwenberghs, UC San Diego|Duygu Kuzum, UC San Diego

Bulk switching RRAM (b-RRAM) address nonidealities of filamentary RRAM for AI at the edge. Here we report a filament-free and multi-level b-RRAM technology with long retention and high endurance. The switching stack is designed to suppress filament formation and achieve multi-level switching through modulation of oxygen vacancy distribution. Top electrode oxygen barrier improves uniformity, retention and endurance. MΩ-level resistance and nonlinearity allow highly accurate MVM operations in selectorless crossbars. Few-shot learning based on dendritic computation and BTSP is experimentally implemented on b-RRAM crossbars. Analog continual learning provided by b-RRAM increases few-shot learning accuracy for hyperdimensional computing at the system level.

11:35 AM
13-6 | MRAM Design-Technology-System Co-Optimization for Artificial Intelligence Edge Devices (Invited), Win-San Khwa, Corporate Research, TSMC, Taiwan|Yi-Lun Lu, Corporate Research, TSMC, Taiwan|Sai Qian Zhang, Meta Reality Lab Research, Meta Platforms, Inc., USA|Xiaoyu Sun, Corporate Research, TSMC, USA|Syed Shakib Sarwar, Meta Reality Lab Research, Meta Platforms, Inc., USA|Ziyun Li, Meta Reality Lab Research, Meta Platforms, Inc., USA|Wu-Wun Chen, Corporate Research, TSMC, Taiwan|Jui-Jen Wu, Corporate Research, TSMC, Taiwan|Xiaochen Peng, Corporate Research, TSMC, USA|Kerem Akarvardar, Corporate Research, TSMC, USA|Ming-Yuan Song, Corporate Research, TSMC, Taiwan|Hung-Li Chiang, Corporate Research, TSMC, Taiwan|Xinyu Bao, Corporate Research, TSMC, USA|Yu-Jen Wang, Embedded Technology Division, TSMC, Taiwan|Wen-Ting Chu, Embedded Technology Division, TSMC, Taiwan|Harry Chuang, Embedded Technology Division, TSMC, Taiwan|Yu-Der Chih, Design Technology Platform, TSMC, Taiwan|Tsung-Yung Jonathan Chang, Design Technology Platform, TSMC, Taiwan|Barbara De Salvo, Meta Reality Lab Research, Meta Platforms, Inc., USA|Chiao Liu, Meta Reality Lab Research, Meta Platforms, Inc., USA|Meng-Fan Chang, Corporate Research, TSMC, Taiwan

STT-MRAM shows great promise for use in artificial intelligence (AI) edge devices due to its compact bitcell area and high endurance. However, it faces read challenges because of its low TMR and R_P.

Conventional sense amplifiers have limitations in optimizing read energy and robustness while providing flexibility to exploit neural-net error tolerance. This article explores the design challenges of conventional sense amplifiers and examines how device parameters (TMR and R_P) impact read performances. A novel capacitive-coupling sense amplifier is introduced to offer a new design space for balancing read energy and robustness. Combining the exploitation of neural-net error tolerance with sense amplifier and device co-design, a Design-Technology-System Co-Optimization (DTSCO) approach demonstrates a read energy reduction of 27.1% to 45.3% with minimal inference accuracy degradation in edge AI applications.

12:00 PM
13-7 | Excellent Synaptic Characteristics and Half-bias selectivity in Vertical Short-channel ECRAM and selector-free 4k Cross-point Array Demonstration (Invited), Jeonghoon Son, POSTECH|Seungkun Kim, POSTECH|Jimin Lee, POSTECH|Byungwoo Lee, POSTECH|Hyunjeong Kwak, POSTECH|Jinho Byun, POSTECH|Jiyong Woo, Kyungpook National University|Seyoung Kim, POSTECH

We present a CMOS-compatible, V-ECRAM designed for the fully-parallel matrix computations for analog AI accelerators. Our V-ECRAM features superior synaptic characteristics thanks to the vertical device structure with an increased high-field update area in the channel. Upon confirmation of excellent switching characteristics, we fabricated a 4k V-ECRAM cross-point array with 88.8% yield and evaluated the array-level device statistics and training performance. The V-ECRAM exhibits extremely low c-to-c variation, d-to-d variation, and vector matrix multiplication error. Moreover, training capability of the V-ECRAM cross-point array were verified through the hardware implementation of novel Tiki-Taka training algorithms using the improved half-bias selectivity.

16 | PMA | High Frequency and Cryogenic RF
9:00 AM – 12:25 PM, Continental 6
Co-Chairs: Ho-Young Cha, Hongik University and Brianna Klein, Sandia National Laboratories

This session includes 7 papers that describe high frequency logic, filters, passives, and oscillators or device optimization for operation at cryogenic temperatures. The first paper, presented by Li from Peking University, reports on logic gates comprised of GaN complimentary logic, enabled by monolithically integrated p- and n-FETs, that demonstrate minimum propagation delays of 13 ns. The second paper, by Liu from IME, describes high frequency acoustic resonators and filters operating at 20 and 48 GHz. Ka from the Shanghai Institute of Microsystem and Information Technology contributes the third paper, presenting on a lithium niobate on silicon carbide technology capable of exciting a variety of acoustic vibrating modes with high electromechanical coupling. The fourth paper by Jeong of KAIST utilizes heterogeneous and monolithically integrated 3D InGaAs HEMTs and CMOS-based passives to realize record-high monolithic 3D RF performance. The fifth paper, by Suzuki from Tokyo Institute of Technology, presents a 600-700 GHz resonant-tunneling-diode oscillator with a high output power exceeding 0 dBm. For the sixth paper, Bian from Stanford describes a 60 GHz oscillator with a high output power of 12.7 dBm based on impact ionization avalanche transit time diodes. For the final paper, Cha from IBM presents optimization of channel structure engineering of InGaAs, enabling qubit readout by enhancing tunneling probability and reducing on-resistance.

09:00 AM
16-0 | Welcome

09:05 AM

16-1 | Polarization Enhanced GaN Complementary Logic Circuits with Short Propagation Delay,

Teng Li, School of Integrated Circuits, Peking University, Beijing, China, College of Microelectronics, Beijing University of Technology, Beijing, China|Jin Wei, School of Integrated Circuits, Peking University, Beijing, China|Meng Zhang, College of Microelectronics, Beijing University of Technology, Beijing, China|Jingjing Yu, School of Integrated Circuits, Peking University, Beijing, China|Yunhong Lao, School of Integrated Circuits, Peking University, Beijing, China|Sihang Liu, School of Integrated Circuits, Peking University, Beijing, China|Ming Zhong, School of Integrated Circuits, Peking University, Beijing, China|Jiawei Cui, School of Integrated Circuits, Peking University, Beijing, China|Junjie Yang, School of Integrated Circuits, Peking University, Beijing, China|Han Yang, School of Physics, Peking University, Beijing, China|Xuelin Yang, School of Physics, Peking University, Beijing, China|Zheyang Zheng, School of Microelectronics, University of Science and Technology of China, Hefei, China|Maojun Wang, School of Integrated Circuits, Peking University, Beijing, China|Kevin J. Chen, Dept. of ECE, Hong Kong University of Science and Technology, Hong Kong, China|Bo Shen, School of Physics, Peking University, Beijing, China

In this work, we develop a GaN complementary logic IC platform. Utilizing polarization enhanced acceptor ionization, a high-performance E-mode GaN p-FET with high I_{max} of 23mA/mm is demonstrated. The elementary logic gate circuits are demonstrated, including GaN CL inverter, transmission, NAND, NOR gate, and RS latch. The GaN CL inverter achieves a large voltage gain of 118.9V/V. The monolithic integration of GaN power HEMT with GaN CL buffers are also presented. The GaN ring oscillators (ROs) exhibit a short average propagation delay per stage (τ_{pd}) of ~13 ns.

09:30 AM

16-2 | Up to 48 GHz mmWave Ferroelectric Sc0.3Al0.7N Bulk Acoustic Wave Resonators and Filters,

Chen Liu, Institute of Microelectronics (IME), Agency for Science, Technology and Research (ASTAR)|You Qian, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)|Ying Zhang, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)|Xinghua Wang, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)|Minghua Li, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)|Peng Liu, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)|Huamao Lin, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)|Qingxin Zhang, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)|Yao Zhu, Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR)
Speakers: Zhilun Zhang, NUS

A 5 nm transition layer with a Sc% gradient was implemented to improve the quality of 40 nm $Sc_{0.3}Al_{0.7}N$ film, resulting in effective coupling coefficient (k^2_{eff}) of > 13%, quality factor up to ~ 300, and 26-dB increment in impedance ratio (R_p/R_s) for the single-layer BAW resonator exceeding 20 GHz. Compact filters have been demonstrated with a central frequency at 21 GHz and a fractional bandwidth close to 11%. A periodically poled bilayer resonator was realized by ferroelectric switching of $Sc_{0.3}Al_{0.7}N$ without the middle electrode, capable of alternating between frequencies in the mmWave spectrum (18.8 GHz and 48.3 GHz).

09:55 AM

16-3 | Predefined Novel Piezo-on-Insulator (PN-POI) Substrates for 5G/6G Acoustic Devices, Xinjian Ke, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences|Jinbo Wu, Shanghai Xin Ou Integration Technology Co., Ltd.|Shibin Zhang, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences|Xiaoli Fang, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences|Pengcheng Zheng, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences|Liping Zhang, Shanghai Xin Ou Integration Technology Co., Ltd.|Dan Ling, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences|Juxing He, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences|Kai Huang, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences|Xin Ou, State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences

This work proposed a predefined novel Piezo-on-Insulator (PN-POI) with patterned bottom metal for 5G and 6G acoustic devices. Based on the PN-POI, not only the transverse electric field excited SH0 mode and LL-SAW resonators but also the vertical electric field excited SH1 and A1 mode resonators and HBAR are also realized. These devices can be widely used in filters, oscillators, and sensors, proving the dramatically expanded functions of PN-POI. Among them, an SH1 mode resonator exhibits the largest k^2 of 36.3% and the highest phase velocity exceeds 7000 m/s, showing great potential for application in 5G and 6G acoustic devices.

10:45 AM

16-4 | Heterogeneous and Monolithic 3D (HM3D) Integrated RF Circuits: HM3D Integration of InGaAs HEMTs on CMOS-Based Backside Passive Devices, Jaeyong Jeong, KAIST|Minsik Park, Chungnam National University|Yoon-Je Suh, KAIST|Jeong-Taek Lim, Chungnam National University|Minkyoung Seong, NNFC|Jooseok Lee, Samsung Electronics|Kihyun Kim, Samsung Electronics|Nahyun Rheem, KAIST|Chan Jik Lee, KAIST|Bong Ho Kim, KAIST|Seong Kwang Kim, Samsung Electronics|Joon Pyo Kim, KAIST|Jongmin Kim, KANC|Woo-Suk Sul, NNFC|Won-Chul Lee, NNFC|Choul-Young Kim, Chungnam National University|Jongwon Lee, Chungnam National University|Sanghyeon Kim, KAIST

We demonstrate HM3D integrated RF amplifiers utilizing top-tier InGaAs HEMTs and CMOS-based backside integrated passive devices (BS-IPDs). We achieved fT/fMAX of 609/455 GHz utilizing HM3D integrated top-tier 65-nm-gate InGaAs HEMTs, which is record-high RF performance among M3D

transistors. The BS-IPDs show stable and consistent behavior before and after HM3D integration due to the low-temperature wafer bonding process. Ultimately, HM3D RF integrated amplifiers based on developed HM3D integrated top-tier InGaAs HEMTs and BS-IPDs technologies exhibit a high gain of 15.6 dB at 31 GHz, the first demonstration of an HM3D RF circuits and the highest gain among M3D RF circuits.

11:10 AM
16-5 | InP-Based Resonant-Tunneling-Diode Oscillators with Milliwatt Power Outputs in 600-700 GHz range, Safumi Suzuki, Tokyo Institute of Technology|Feifan Han, Tokyo Institute of Technology|Takumi Shimura, Tokyo Institute of Technology|Hiroki Tanaka, Tokyo Institute of Technology

We fabricated and characterized a high-power terahertz (THz) oscillator with two stripe-shaped, large-area AlAs/InGaAs resonant tunneling diodes integrated into a cavity resonator. We experimentally obtained high-power THz oscillations exceeding 1 mW in the 600-700 GHz range, which roughly agreed with the theoretical calculations.

11:35 AM
16-6 | First Demonstration of 60 GHz GaN IMPATT Oscillator with 12.7 dBm Output Power, Zhengliang Bian, Stanford University|Avery Marshall, QuinStar Inc|Lisette Zhang, QuinStar Inc|Tracy Lee, QuinStar Inc|Srabanti Chowdhury, Stanford University

This study reports the first demonstration of a V-band GaN IMPATT oscillator, showcasing a 60.8 GHz oscillation with an output power of 12.7 dBm. To enable the avalanche in the diodes, a bevel mesa edge termination with SiO_2 sidewall passivation was employed. The fabricated diodes exhibited a positive temperature coefficient of breakdown voltage up to 200°C, indicating excellent avalanche capabilities. The bulk GaN substrate was thinned to 20 μm before mounting the diode on a diamond heat sink, reducing both electrical and thermal resistance. The packaged GaN IMPATT diodes were then embedded in a V-band resonant cavity for RF characterizations.

12:00 PM
16-7 | Cryogenic InGaAs HEMTs with Record-Low On-Resistance using Optimized Channel Structure, Eunjung Cha, IBM Research Europe|Alberto Ferraris, IBM Research Europe|Daniele Caimi, IBM Research Europe|Hung-Chi Han, EPFL|Antonis Olziersky, IBM Research Europe|Marilyne Sousa, IBM Research Europe|Edoardo Charbon, EPFL|Cezar Zota, IBM Research Europe

We present cryogenic InGaAs HEMTs showing record-low on-resistance and noise characteristics for low-power qubit readout, based on analysis of HEMTs with different indium channel compositions. We show that increasing indium content reduces the barrier resistance at 4 K, leading to the lowest reported R_{ON} to date, 198 Ω·μm at L_G = 170nm. In addition, InGaAs HEMTs with a 75% indium channel content exhibit *SS* < 10 mV/dec*,* g_m = 2.3 mS/μm, resulting in a record-low noise indication factor of 0.15 √V·mm/S for cryogenic HEMTs. These results emphasize the importance of channel structure engineering for future large-scale quantum computing applications.

18 | SMB | Integrated Sensors and MEMS
9:00 AM – 12:25 PM, Imperial A
Co-Chairs: Itaru Yanagi, Hitachi and Yao Zhu, A*STAR

This session includes 7 papers that describe the advances in the area of MEMS CMOS integration, advanced MEMS processes as well as multimodal sensors. The first paper by Arslan et al. presents the integration of micro-scale PVDF transducers directly on CMOS substrate for photoacoustic imaging. The second paper by Chen et al. develops a novel 1-D dual-gap CMOS-MEMS capacitive micromachined ultrasonic transducer (CMUT) array, demonstrating superior transmitting efficiency of 16.7 kPa/V/mm2 and receiving sensitivity of 57 mV/kPa in underwater acoustic test. The third paper by Weng et al. introduces a subtractive microfluidics platform integrated with TSMC 180nm CMOS chip, demonstrating three structures including 1:64 fluidic splitter and a micro-mixer, on-chip ion-selective field-effect transistors and Hall sensors, and impedance read out circuits. The fourth paper is an invited paper by Hofmeister from STMicroelectronics. This paper provides an overview of emerging applications which will drive innovation in the MEMS industry for the years to come. It also analyzes how these new MEMS products call for innovation in design and process technology and will require new approaches in "front-end/back-end" integration. The fifth paper by Shi et al. reports an innovative MEMS technology to fabricate a monolithic chip that simultaneously provides ultrahigh capacitance and inductance densities. The sixth paper by Cho et al. proposes a next-generation anisotropic etching method that utilizes vaporized HF and ozone in metal-assisted chemical etching (MACE) process to realize high aspect ratio Si nanowire structure, with 70 times faster etch rate. The last paper by Jung et al. presents an intelligent multimodal sensors integrating gas, barometric pressure and temperature sensing, providing highly accurate gas alarms (97.8%) for mixed gases.

09:00 AM
18-0 | Welcome

09:05 AM
18-1 | Monolithic Fabrication of Micron-Scale Piezo-Polymer Transducers on CMOS, Volkan Arslan, Columbia University|Jakub Jadwiszczak, Columbia University|Jeffrey Sherman, Columbia University|Ilke Uguz, Columbia University|Kenneth Shepard, Columbia University

Interest in integrating piezoelectric transducers with CMOS technology is growing for many bioelectronic applications. However, current methods struggle to fabricate transducers down to the micron scale. We integrate polymer piezoelectric ultrasound transducer arrays of this scale onto CMOS chips and demonstrate application to high-resolution photoacoustic imaging

09:30 AM
18-2 | Design and Implementation of a Novel Dual-Gap CMOS-MEMS CMUT Array, Hung-Yu Chen, National Tsing Hua University|Clark Nguyen, University of California, Berkeley|Sheng-Shian Li, National Tsing Hua University

This study presents a novel 1-D CMOS-MEMS CMUT array with dual transduction gaps (180 nm and 400 nm) on a standard CMOS platform, designed for high transceiving efficiency at low DC bias voltages. Detailed fabrication and testing validate its performance, showing a high electromechanical coupling strength and ultrasonic transmitting efficiency of 16.7 kPa/V/mm², with a receiving sensitivity of 57 mV/kPa underwater. Self-Tx/Rx experiments confirm the device's efficiency. Integration with a monolithic amplifier yields an impressive NEF of 0.39 mPa√(mW/Hz), demonstrating its potential for advanced ultrasonic applications.

09:55 AM

18-3 | Subtractive Microfluidics in CMOS, Wei-Yang Weng, University of California, Berkeley|Alexander Di, University of California, Berkeley|Xiang Zhang, University of California, Berkeley|Ya-Chen Tsai, University of California, Berkeley|Yan-Ting Hsiao, National Taiwan University, University of California, Berkeley|Jun-Chau Chien, University of California, Berkeley, National Taiwan University

This paper introduces a microfluidics platform embedded within a silicon chip implemented in CMOS technology. The platform utilizes a one-step wet etching method to create fluidic channels by selectively removing CMOS back-end-of-line (BEOL) metals. Three types of structures are presented in a TSMC 180-nm CMOS chip: (1) passive microfluidics in the form of a micro-mixer and a 1:64 splitter, (2) fluidic channels with embedded ion-sensitive field-effect transistors (ISFETs) and Hall sensors, and (3) integrated on-chip impedance-sensing readout circuits. Our CMOS subtractive microfluidics technique enables tight integration of fluidics and electronics, paving the way for future small-size, high-throughput lab-on-chip (LOC) devices.

10:45 AM

18-4 | Emerging applications driving future MEMS Product and Technology development (Invited), Anton Hofmeister, STMicroelectronics

The paper provides an overview of emerging applications which will drive innovation in the MEMS industry for the years to come. Examples range from highly accurate Inertial MEMS for future car navigation tasks, over new sensing technologies for wearable "vital sign monitoring" solutions, to new MEMS based man-machine interfaces. The paper will analyze how these new MEMS products call for innovation in design and process technology and will require new approaches in "front-end/back-end" integration. It will also show examples of integrating "intelligence" into the MEMS device, enabling basic AI based computing locally "on the edge". Lastly, the paper will elaborate on the importance of "sustainability" built into every single step of the MEMS value chain.

11:10 AM

18-5 | Monolithic MEMS L-C Chip with Ultrahigh Performance Densities for PwrSoC Applications, Sixing Xu, Hunan University|Zhanpeng Shi, Hunan University|Jiyong Zhou, Hunan Univeristy|Jianyou Dai, Hunan University|Yier Xia, Tsinghua University|Minghao Xu, Tsinghua University|Zerui Xu, Tsinghua University|Jiezhen Liu, Hunan University|Wei Hu, Hunan University|Lei Shan, Hunan University|Xiaohong Wang, Tsinghua University|Lei Liao, Hunan University

The adoption of PwrSoC is hindered by the limited performance densities of current on-chip passive elements. This paper reports an innovative MEMS technology that achieves remarkable high capacitance and inductance densities simultaneously on a monolithic chip. We develop a multifunctional 3D high-aspect-ratio alloy electrode technology that functions as a low-resistance MEMS inductor coil and, after selective etching, serves as a porous capacitor electrode to provide ultrahigh electrochemical capacitance. The chip (4.4×5.5 mm^2), demonstrate capacitance and inductance densities of 10^5 nF/mm^2 ($6.25×10^7$ nF/mm^3) and 20.3 nH/mm^2 ($4.05×10^3$ nH/mm^3), surpassing conventional technologies by three and one orders of magnitude, respectively.

11:35 AM

18-6 | Advanced Metal-assisted Chemical Etching using HF Vapor and Ozone for MEMS Process, Hyein Cho, Department of Chemical Engineering, Kangwon National University|Yebin Ahn, Department of Chemical Engineering, Kangwon National University|Sang Beom Song, Department of Chemical Engineering, Kangwon National University|Soohyeok Park, Department of Chemical Engineering, Kangwon National University|Yejin Han, Department of Chemical Engineering, Kangwon National University|Geonhwi Kim, Department of Chemical Engineering, Kangwon National University|Eunjeong Song, Department of Energy Science and Technology, Chungnam National University|Ye Ji Choi, Department of Chemical Engineering, Kangwon National University|So Eun Jang, Department of Chemical Engineering, Kangwon National University|Duck Hyun Youn, Department of Chemical Engineering, Kangwon National University|Hyeyoung Shin, Department of Energy Science and Technology, Chungnam National University|Han-Don Um, Department of Chemical Engineering, Kangwon National University

This study proposes a next-generation anisotropic etching method that utilizes vaporized HF and ozone in the metal-assisted chemical etching (MACE) process for the first time. The etching behavior and mechanisms under various gas-phase MACE conditions were analyzed, achieving an etching rate 70 times faster than conventional gas-phase MACE, even at room temperature. Using optimized gas-phase MACE, high-quality Si nanowire structures were fabricated, and excellent responsivity was experimentally demonstrated in a dopant-free nanowire photodetector.

12:00 PM
18-7 | Intelligent Multimodal Sensors Integrating Gas, Barometric Pressure, and Temperature Sensing, Gyuweon Jung, Seoul National University|Hyeongsu Kim, Seoul National University|Chayoung Lee, Seoul National University|Jaehyeon Kim, Seoul National University|Woo Young Choi, Seoul National University|Jong-Ho Lee, Seoul National University

We present new intelligent multimodal sensors that integrates various sensing and in-memory computing (IMC)-based processing functions. The sensor linearly combines barometric pressure (*P*) sensing signals using IMC and utilizes temperature (*T*) sensing signal to provide a reliable *P*. By utilizing multimodal sensing signals and an IMC-based capacitive binarized neural network, the sensor provides highly accurate gas alarms (97.8%) for mixed gases even with varying *T* and *P*, and variations in sensing signals (σ/μ= 0.1).

19 | RSD | Emerging Devices: Security Applications and Reliablity
9:00 AM – 12:25 PM, Imperial B
Co-Chairs: Ming-Yi Lee, Macronix and Azad Naeemi, Gatech

This session covers the latest advances in security applications and the reliability of emerging devices. The first paper presents a homomorphic encryption circuit using FeFET arrays for IoT clients, achieving 99.6% accuracy, latency of 13us, and a low energy consumption of 2.72nJ per number-theoretic-transform. The second paper leverages the variability in MOSFETs to create an unclonable 28nm RRAM-based double encryption compute-in-memory circuit. The third paper presents an all-in-one lattice-based cryptosystem, including public key generation, encryption, and decryption based on a 40nm 1 Mbit RRAM chip. The fourth paper utilizes workfunction engineering and O3 plasma treatment to develop fully BEOL-compatible IGZO FeFETs with wide memory window and high endurance. The fifth paper identifies the two main cycle-to-cycle Vth variability mechanisms in GeAsTe Ovonic threshold switching devices as small random variability caused by defects that remain active during the off-state and large pseudo-random

variability caused by defects activated during the on-state. The sixth paper studies the dependence of the writing reliability of STT-MRAM on the angle of the external magnetic field, reporting a factor of 10^3 difference for a 40mT external field. The last paper presents an overview of the latest progress in the fabrication of integrated circuits based on 2D materials.

09:00 AM
19-0 | Welcome

09:05 AM
19-1 | First Demonstration of High Throughput and Reliable Homomorphic Encryption Using FeFET Arrays for Resource-Limited IoT Clients, Hanyong Shao, Peking University|Yuejia Zhou, Peking University|Zhiyuan Ning, Peking University|Wenpu Luo, Peking University|Xinyu Bin, University of Science and Technology of China|Jinghao Yang, Peking University|Kechao Tang, Peking University|Ru Huang, Peking University

Homomorphic Encryption (HE) promises robust privacy security for offloading computation, but the complex polynomial operations challenge its deployment in IoT client. In this work, we demonstrate the first HE client that enables high efficiency polynomial sampling and multiplication both on FeFET arrays. Using the fast-gate-perturbation on entropy-engineered FeFET, we develop a robust TRNG with 50 Mbps throughput and tunable bit probability, achieving all essential functions required for polynomial sampling. To simplify the polynomial multiplication, we propose a hybrid-domain FeFET Ternary Product for Vector-Matrix-Vector multiplication. This work provides a hardware solution for efficient and reliable HE clients in security applications.

09:30 AM
19-2 | First Demonstration of Unclonable Double Encryption 28nm RRAM-based Compute-in-Memory Macro for Confidential AI, Yiyang Chen, School of Integrated Circuits, Peking University|Lixia Han, School of Integrated Circuits, Peking University|Ao Shi, School of Integrated Circuits, Peking University|Lianliang Wu, School of Integrated Circuits, Peking University|Hairuo Lu, School of Integrated Circuits, Peking University|Jiaqi Li, School of Integrated Circuits, Peking University|Haozhang Yang, School of Integrated Circuits, Peking University|Yulin Feng, School of Integrated Circuits, Peking University|Zheng Zhou, School of Integrated Circuits, Peking University|Lifeng Liu, School of Integrated Circuits, Peking University|Xiaoyan Liu, School of Integrated Circuits, Peking University|Jinfeng Kang, School of Integrated Circuits, Peking University|Peng Huang, School of Integrated Circuits, Peking University

For the first time, we demonstrate an unclonable 28nm RRAM based CIM macro with in-situ double encryption and MVM to protect the AI models. Main features include: 1) the sign and the value of weights are encrypted with different keys show 2^{960} higher key space. 2) the multi-bit weights can be in-situ decrypted within one cycle. 3) the variability of the MOSFET creates an unclonable identity. So, the macro is still trustworthy even when all the keys are exposed, which is beyond all traditional encryption methods.

09:55 AM
19-3 | First Demonstration of Masked Polynomial Multiplier based on 40nm 1TG1R RRAM Secure Chip for Lattice-based Cryptography, Jingwei Sun, Peking University|Zongwei Wang, Peking University|Haoyang Gu, Peking University|Lin Bao, Peking University|Qishen Wang, Peking

University|Shengyu Bao, Peking University|Linbo Shan, Peking University|Ling Liang, Peking University|Yimao Cai, Peking University|Ru Huang, Peking University

Lattice-based Cryptography (LBC) is resilient against quantum attacks but requires extensive polynomial multiplications (PM), which are time-consuming and power-hungry. PM can be accelerated by matrix-vector multiplication (MVM), yet conventional MVM accelerators are vulnerable due to the transparency of the weight matrix. This study presents a novel masked MVM (M2VM) operation using one-transmission-gate one-RRAM (1TG1R) array, where only the absolute values of the weight matrix are stored. This architecture mitigates weight leakage risks and enhances MVM accuracy during PM. A lattice-based cryptosystem solver using 40nm 1Mb RRAM chip achieves 1.992 MPMS/W energy efficiency, significantly outperforming FPGA and other RRAM solutions.

10:45 AM

19-4 | A Fully BEOL-compatible (300℃ Annealing) IGZO FeFET with Ultra-high Memory Window (10V) and Prominent Endurance (109), Pan Xu, University of Chinese Academy of Sciences|Pengfei Jiang, Institute of Microelectronics, Chinese Academy of Sciences|Yang Yang, Institute of Microelectronics, Chinese Academy of Sciences|Xueyang Peng, University of Chinese Academy of Sciences|Wei Wei, Institute of Microelectronics, Chinese Academy of Sciences|Tiancheng Gong, Institute of Microelectronics, Chinese Academy of Sciences|Yuan Wang, Institute of Microelectronics, Chinese Academy of Sciences|Xiao Long, Institute of Microelectronics, Chinese Academy of Sciences|Jiebin Niu, Institute of Microelectronics, Chinese Academy of Sciences|Zhenhua Wu, Institute of Microelectronics, Chinese Academy of Sciences|Qing Luo, Institute of Microelectronics, Chinese Academy of Sciences|Ming Liu, Institute of Microelectronics, Chinese Academy of Sciences

In this work, we propose an integrated ferroelectric (FE) $Hf_{0.5}Zr_{0.5}O_2$ (HZO) and amorphous In-Ga-Zn-O (a-IGZO) channel FeFET with a maximum 10V MW and prominent endurance up to 10^9. Workfunction (WF) engineering is utilized to regualte the intrinsic V_t to improve the PGM/ERS efficiency with full-loop polarization switching, and the adopted Mo gate can effectively reduce the thermal budget to 300℃ ensuring a fully BEOL compatibility. Then with O_3-plasma treatment to the gate electrode, the introduced tunneling layer can futher improve the MW by gate charge injection.

11:10 AM

19-5 | Understanding the Variability in GeAsTe Ovonic Threshold Switching Devices, Zeyu Hu, Liverpool John Moores University|Guosheng Wang, Liverpool John Moores University|Zheng Chai, Xi'an Jiaotong University|Weidong Zhang, Liverpool John Moores University|Daniele Garbin, imec|Robin Degraeve, imec|Sergiu Clima, imec|Taras Ravsher, imec|Andrea Fantini, imec|Jian Zhang, Liverpool John Moores University|Attilio Belmonte, imec|Gouri Kar, imec

In this work,tTwo different cycle-to-cycle V_{th} variability mechanisms in GeAsTe OTS are identified: (i) Defects that remain active at the off-state lead to the intrinsic small random variability (SRV); (ii) Defects activated at the on-state result in large pseudo-random variability (LPV). Novel techniques including the fast frequency-domain noise analysis and the sequential variability analysis are developed to identify the SRV and LPV mechanisms and to characterize their statistical correlations with different defects. The observed single modal, bimodal and multimodal C2C V_{th} variability distributions can be explained by the combination of SRV and LPV at different pulse operation conditions.

11:35 AM
19-6 | Magnetic immunity of STT-MRAM: external magnetic field orientation impact on writing reliability, Natan Vander Meeren, KU Leuven|Simon Van Beek, imec|Maxwel Monteiro, imec|Fernando Garcia-Redondo, imec|Jyotirmoy Chatterjee, imec|Ankit Kumar, imec|Kurt Wostyn, imec|Sebastien Couet, imec|Ingrid Verbauwhede, KU Leuven

We experimentally investigate the writing reliability of STT-MRAM in the presence of magnetic fields oriented at different angles. It is established that external magnetic fields oriented non-parallel to the easy axis of the device significantly increase the write error rate for short pulse widths. These cases have been ignored in magnetic immunity testing thus far. More precisely, at 40mT, the write error rate is shown to deteriorate by over a factor of 10^3 depending on the angle of the external field. Moreover, these results are corroborated by stochastic LLGS simulations.

12:00 PM
19-7 | Integrated circuits based on two-dimensional materials (Invited), Saptarshi Das, Pennsylvania State University|Dipanjan Sen, Pennsylvania State University|Subir Ghosh, Pennsylvania State University|Rameez Raja Shaik, Pennsylvania State University|Harikrishnan Ravichandran, Pennsylvania State University

Two-dimensional (2D) materials have seen considerableadvancements over the last decade, including improvementsin growth techniques, device performance, andcircuit integration. Additionally, a large number of fieldeffecttransistors (FETs) have been integrated into analog,digital, mixed signal circuits for enabling applications suchas neuromorphic and bio-inspired computing, near-sensor processing,and hardware security. More recently, monolithic andheterogenous three-dimensional (3D) integration of 2D FETshave gained significant attention. While these developmentsare promising, achieving p-type 2D FETs for complementarylogic circuits remains a challenge. This paper reviews theprogress in integrated circuits based on 2D materials andhighlights future opportunities and challenges that need to beaddressed for their adoption in commercial electronics.

Coffee break with Exhibitors
10:20 AM – 11:15 AM
Yosemite

Coffee break with Exhibitors

CL | CL | Career Lunch and IEEE Awards
12:20 PM – 2:00 PM
Plaza Ballroom

In the IEDM Career Luncheon, two outstanding members of the electron device community will present their career paths and learnings from their career journeys. This is followed by a Q & A session moderated by Prof. Beilner and with active participation from the audience. The career luncheon is intended to provide new perspectives on careers in semiconductor technology to all members of our community, but might be particularly interesting for younger generations of scientists, engineers and entrepreneurs.

Organizer & Moderator: Janina Bellner, Friedrich Alexander University and Siemens

Panelists & Speakers: Prof. Anna Fontcuberta-i-Morral (EPFL), Switzerland and Dr. Iuliana Radu (TSMC)

22 | NC | Stochastic and Spin-Based Computing
2:15 PM – 5:15 PM, Continental 1 – 3
Co-Chairs: Christopher Bennet, Sandia National Laboratories and Elisabetta Chicca, University of Groningen

This session includes 6 papers that use emerging memory (spin or charge-based devices) whose intrinsic stochastic behaviors are instrumental to their computations. These novel approaches could bring new functionalities to diverse applications, from performing continuous optimization, to reducing the energy cost of random number generation in logic circuits or diffusion models. The first paper, by Zhihua Xiao and colleagues, shows that novel magnetic tunnel junction (MTJ) probabilistic bits (e.g. p-bits), function well for hardware accelerating diffusion networks. The second paper, by Kyuree Kim and colleagues, discusses the use of intrinsic noise in resistive RAM (ReRAM) crossbars by demonstrating a Hopfield network in hardware. The third paper, by Erwan Plouet and colleagues (Invited), uses spintronic devices in radio-frequency mode to classify various objects at high-speed. The fourth paper, by Keyi Shan and colleagues, adapts annealing methods from quantum Ising machines, and run them on ReRAM arrays for optimization problems. The fifth paper, by Chen-Yu Yang and colleagues, demonstrates a novel spin-orbit-torque MTJ device that can serve either as a deterministic synapse or a stochastic neuron, depending on the configuration. The last paper, by Nihal Singh and colleagues, experimentally shows that random MTJ fluctuations can be used to implement tunable Gaussian circuits that solve continuous optimizations tasks.

02:15 PM
22-0 | Welcome

02:20 PM
22-1 | In-Memory Neural Stochastic Differential Equations with Probabilistic Differential Pair Achieved by In-Situ P-bit using CMOS Integrated Voltage-Controlled Magnetic Tunnel Junctions,
Zhihua Xiao, The Hong Kong University of Science and Technology, AI Chip Center for Emerging Smart Systems|Yaoru Hou, The Hong Kong University of Science and Technology, AI Chip Center for Emerging Smart Systems|Zihan Tong, The Hong Kong University of Science and Technology|Yicheng Jiang, The Hong Kong University of Science and Technology|Yiyang Zhang, The Hong Kong University of Science and Technology|Xuezhao Wu, The Hong Kong University of Science and Technology|Albert Lee, InstonTech|Di Wu, InstonTech|Hao Cai, School of Integrated Circuit, Southeast University|Qiming Shao, The Hong Kong University of Science and Technology, AI Chip Center for Emerging Smart Systems

We addressed the bottleneck of existing probabilistic computing using ex-situ P-bits. The generation-sample-transfer-compute paradigm of existing P-bits reintroduces the memory bottleneck seen in von Neumann architectures, thereby limiting the efficiency of probabilistic computing. We propose a novel in-situ P-bit compatible with compute-in-memory schemes using voltage-controlled magnetic tunnel junctions that pairs a data-bit and a P-bit as a probabilistic differential pair in a crossbar array and can directly utilize the random sequences in-situ for computing. We experimentally demonstrate the high efficiency and throughput of the proposed scheme and its application to solve an in-memory neural stochastic differential equation for generative AI.

02:45 PM

22-2 | Ising Solver using Weight Profile of Memristor Crossbar Array for Combinatorial Optimization, Kyuree Kim, Inha University|Sangwook Youn, Hanyang University|Jinwoo Park, Hanyang University|Hyungjin Kim, Hanyang University

In this work, a weight profile design is presented for efficient Ising solver system based on HNN using 32×32 memristor crossbar array. It utilizes device noise in the probabilistic decision process of simulated annealing for binary current inputs. By implementing 0 and 1 weight matrix across various conductance states in the crossbar, we experimentally solve an unweighted max-cut problem. It is confirmed that higher noise levels, concentrated in high resistance states, enable more efficient convergence to the minimum point of the HNN energy function. This approach effectively exploits intrinsic noise, reducing external hardware overhead and demonstrating feasibility for optimization problems.

03:10 PM
22-3 | Convolutions with Radio-Frequency Spin-Diodes (Invited), Julie Grollier, Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay|Erwan Plouet, Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay|Hanuman Singh, Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay|Pankaj Sethi, Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay|Frank Mizrahi, Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay|Dédalo Sanz-Hernandez, Laboratoire Albert Fert, CNRS, Thales, Université Paris-Saclay
Speakers: Damien Querlioz

The classification of radio-frequency (RF) signals is crucial for applications in robotics, traffic control, and medical devices. Spintronic devices, which respond to RF signals via ferromagnetic resonance, offer a promising solution. Recent studies have shown that a neural network of nanoscale magnetic tunnel junctions can classify RF signals without digitization. However, the complexity of these junctions poses challenges for rapid scaling. In this work, we demonstrate that simple spintronic devices, known as metallic spin-diodes, can effectively perform RF classification. These devices consist of NiFe/Pt bilayers and can implement weighted sums of RF inputs. We experimentally show that chains of four spin-diodescan execute 2x2 pixel filters, achieving high-quality convolutions on the Fashion-MNIST dataset. Integrating the hardware spin-diodes in a software network, we achieve anaccuracy of 88 % on the first 100 images, compared to 88.4 % for full software with noise, and 90 % without noise.

03:35 PM
22-4 | One-Step Combinatorial Optimization Solver with Fully Integrated Analog Memristors and Annealing Module, Keyi Shan, The University of Hong Kong|Mingrui Jiang, The University of Hong Kong|Zhiyuan Du, The University of Hong Kong|Yu Xiao, Zhejiang University|Yunwei Tong, The University of Hong Kong|Zefan Li, The University of Hong Kong|Szu-Hao Yang, The University of Hong Kong|Chengping He, The University of Hong Kong|Ruibin Mao, The University of Hong Kong|Peng Lin, Zhejiang University|Can Li, The University of Hong Kong

Ising machines are effective for solving combinatorial optimization problems (COPs), but current memristor-based versions require discrete time and costly analog-to-digital conversions. We designed and fabricated the first fully analog memristor-based Ising solver, solving COPs in a single step. Our chip features a 96x96 memristor crossbar array for storing the coupling matrix and 96 amplifier-based spin circuits, emulating the Hamiltonian shift in quantum-inspired adiabatic annealing. Experimental results

show higher-quality solutions in one step, with simulations confirming tolerance to device variations. Our analysis indicates at least a 1.5x speed-up and 9.6x energy savings compared to state-of-the-art methods.

04:25 PM
22-5 | Dual-Function Unipolar Top-pSOT-MRAM for All-Spin Probabilistic Computing with Ultra-Dense Coupling and Adaptive Temporal Coding, Chen-Yu Yang, National Yang Ming Chiao Tung University|Ming-Chun Hong, National Yang Ming Chiao Tung University|Le-Chih Cho, Taiwan Semiconductor Research Institute|Baofang Cai, National University of Singapore|Yi-Ju Chen, Taiwan Semiconductor Research Institute|Cho-Lun Hsu, Taiwan Semiconductor Research Institute|Kai-Shin Li, Taiwan Semiconductor Research Institute|Geng-Chiau Liang, National Yang Ming Chiao Tung University|Tuo-Hung Hou, National Yang Ming Chiao Tung University, Taiwan Semiconductor Research Institute

A compact all-spin probabilistic computing architecture is proposed based on a novel unipolar Top-pSOT-MRAM. This new device enables high-density two-diode-one-MRAM (2D1M) integration, improved thermal stability, and great process compatibility. Additionally, high-speed deterministic and stochastic field-free unipolar STT-assisted SOT switching is employed for dual functionality, namely interchangeable binary programming and temporal-coded binary stochastic oscillation. Great tunability in frequency, duty cycle, and stochasticity is intrinsic to the stochastic temporal coding function. This all-spin probabilistic computing architecture with adaptive stochasticity and compact hardware is ideal for accelerating large-scale combinatorial optimization, such as the 100-city traveling salesman problem.

04:50 PM
22-6 | Beyond Ising: Mixed Continuous Optimization with Gaussian Probabilistic Bits using Stochastic MTJs, Nihal Singh, Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA, 93106, USA|Corentin Delacour, Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA, 93106, USA|Shaila Niazi, Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA, 93106, USA|Kemal Selcuk, Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA, 93106, USA|Daniel Golenchenko, Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA, 93106, USA|Haruna Kaneko, Research Institute of Electrical Communication, Tohoku University, Sendai, 980-8579, Japan, Graduate School of Engineering, Tohoku University, Sendai, 980-8577, Japan|Shun Kanai, Research Institute of Electrical Communication, Tohoku University, Sendai, 980-8579, Japan, Graduate School of Engineering, Tohoku University, Sendai, Japan|Hideo Ohno, Graduate School of Engineering, Tohoku University, Sendai, 980-8577, Japan|Shunsuke Fukami, Research Institute of Electrical Communication, Tohoku University, Sendai, 980-8579, Japan, Graduate School of Engineering, Tohoku University, Sendai, Japan|Kerem Camsari, Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA, 93106, USA

Ising Machines for computational problems often rely on binary variables, limiting practical applications requiring continuous variables. We demonstrate continuous probabilistic bits using a network-of-networks approach with Gaussian bits (g-bits) built from probabilistic bits (p-bits). Our setup integrates stochastic Magnetic Tunnel Junctions (sMTJs) with a digital FPGA, achieving significant efficiency improvements.

23 | ODI | Displays and Photonic Platforms

2:15 PM – 5:15 PM, Continental 4
Co-Chairs: Matteo Buffolo, University of Padova and Rainer Minixhofer, ams OSRAM

This session focuses on TFT displays, the integration of photonic devices and their underlying technology platforms. The first (invited) presentation will show the integration of a quantum dot laser into a high capacity silicon photonic integrated circuit platform. The second talk will demonstrate a novel photon trapping III-V APD integrated onto an SOI technology. The third presentation will present an advanced silicon photonics foundry platform tailored to meet the increasing demands of next-generation data communication applications. The second half of the session will focus on next generation TFT displays. The first paper in this second part gives an overview on a three-dimensional integrated architecture involving a novel combination of capacitive and optical sensing. The second paper shows the first implementation of a flexible active-matrix micro- LED display utilizing ITO TFTs pixel circuits. The last paper in the session follows-up on the topic of flexible active matrix micro-LED displays involving through plastic vias resulting in a almost bezel-less tiling capability.

02:15 PM
23-0 | Welcome

02:20 PM
23-1 | Integrated Quantum Dot Lasers and High Capacity Silicon Photonic Integrated Circuits (Invited), John Bowers, University of California Santa Barbarba (UCSB), USA|Rosalyn Koscica, Univ of California Santa Barbara|Alec Skipper, Univ of California Santa Barbara|Kaiyin Feng, Univ of California Santa Barbara|Chen Shang, Univ of California Santa Barbara|Andrew Clark, IQE|Peter Ludewig, NAsP III-V|David Harame, RF SUNY Polytechnic Institute

Optical interconnect data rates are rapidly increasing, which is driving the intimate 3D integration of photonics and electronics.As a key step in this development, we report the direct growth of quantum dot (QD) lasers with electrical pumping on 300 mm Si wafers on both a planar template and in-pocket template for in-plane photonic integration. O-band lasers with five QD layers were grown with molecular beam epitaxy (MBE) in a 300 mm reactor and then fabricated into standard Fabry-Perot ridge waveguide cavities. Edge-emitting lasers are demonstrated with high yield and reliable results ready for commercialization and scaled production, and efforts to make monolithically integrated lasing cavities grown on silicon-on-insulator (SOI) wafers vertically aligned and coupled to SiN waveguides on the same chip show the potential for 300 mm-scale Si photonic integration with in-pocket direct MBE growth.

02:45 PM
23-2 | First Photon-Trapping InGaAs Avalanche Photodiode and Its Integration on the SOI Platform, Rui Shao, National University of Singapore|Jishen Zhang, National University of Singapore|Kian Hua Tan, National University of Singapore|Satrio Wicaksono, National University of Singapore|Haiwen Xu, National University of Singapore|Yue Chen, National University of Singapore|Xuanqi Chen, National University of Singapore|Yuxuan Wang, National University of Singapore, National University of Singapore|Chen Sun, National University of Singapore|Qiwen Kong, National University of Singapore|Xuanyao Fong, National University of Singapore|Xiao Gong, National University of Singapore

InGaAs avalanche photodiodes with photon-trapping structures have been realized and integrated on SOI. They enable the realization of a record-high responsivity of 0.75 A/W and an quantum efficiency of 57.2%

among APDs with an InGaAs absorber thickness of ~ 250 nm. High detectivitiesof 9.34×10^{10} Jones at 4 V and 3.43×10^{12} Jones at 24.1 V are achieved with a broad voltage window from 4 V to 24.1 V. Our PTAPD exhibits a low dark current of 51.3 nA and a gain of >100. Our work demonstrates potential of PT structures in light manipulation and the feasibility of integrating III-V on SOI .

03:10 PM

23-3 | Silicon Photonics Platform for Next Generation Data Communication Technologies, S.K. Yeh, Taiwan Semiconductor Manufacturing Company|C.T. Shih, Taiwan Semiconductor Manufacturing Company|F. Yuan, Taiwan Semiconductor Manufacturing Company|C.M. Hung, Taiwan Semiconductor Manufacturing Company|C.H. Chu, Taiwan Semiconductor Manufacturing Company|H.Y. Lu, Taiwan Semiconductor Manufacturing Company|J.H. Yang, Taiwan Semiconductor Manufacturing Company|W.S. Lo, Taiwan Semiconductor Manufacturing Company|C.H. Chen, Taiwan Semiconductor Manufacturing Company|S.Y. Tsai, Taiwan Semiconductor Manufacturing Company|W.C. Tai, Taiwan Semiconductor Manufacturing Company|S.C. Liu, Taiwan Semiconductor Manufacturing Company|S.D. Wang, Taiwan Semiconductor Manufacturing Company|K.Q. Wen, Taiwan Semiconductor Manufacturing Company|W.C. Wang, Taiwan Semiconductor Manufacturing Company|C.C. Tung, Taiwan Semiconductor Manufacturing Company|B.T. Lin, Taiwan Semiconductor Manufacturing Company|F. Hu, Taiwan Semiconductor Manufacturing Company|P.C. Yeh, Taiwan Semiconductor Manufacturing Company|C.H. Huang, Taiwan Semiconductor Manufacturing Company|T.H. Wu, Taiwan Semiconductor Manufacturing Company|C.C. Chu, Taiwan Semiconductor Manufacturing Company|W.C. Kuo, Taiwan Semiconductor Manufacturing Company|C.Y. Tsai, Taiwan Semiconductor Manufacturing Company|S.W. Chang, Taiwan Semiconductor Manufacturing Company|E.C. Chen, Taiwan Semiconductor Manufacturing Company|C.W. Chiang, Taiwan Semiconductor Manufacturing Company|Y.M. Wang, Taiwan Semiconductor Manufacturing Company|F.C. Huang, Taiwan Semiconductor Manufacturing Company|S.M. Wu, Taiwan Semiconductor Manufacturing Company|J.Y. Lin, Taiwan Semiconductor Manufacturing Company|C.T. Tang, Taiwan Semiconductor Manufacturing Company|W.K. Liu, Taiwan Semiconductor Manufacturing Company|T.L. Hsieh, Taiwan Semiconductor Manufacturing Company|W.J. Mao, Taiwan Semiconductor Manufacturing Company|W.T. Lo, Taiwan Semiconductor Manufacturing Company|C.Y. Peng, Taiwan Semiconductor Manufacturing Company|S.H. Su, Taiwan Semiconductor Manufacturing Company|F. Tsui, Taiwan Semiconductor Manufacturing Company|N. Shi, Taiwan Semiconductor Manufacturing Company|V. Shih, Taiwan Semiconductor Manufacturing Company|S.F. Huang, Taiwan Semiconductor Manufacturing Company

TSMC has developed an advanced silicon photonics foundry platform tailored to meet the increasing demands of next-generation data communication applications. This paper presents an overview of the platform and the performance of key photonic devices.

04:00 PM

23-4 | Multi-modal Full-area High-resolution Human-Machine Interactive Surface with 3D Stacking of IGZO TFT Active-Matrix Capacitive and Optical Sensing Arrays, Yu Huang, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Jun Li, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Tong Shan, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Rongrong Shi, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Zhifan Zhang, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Li'ang Deng, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Mengwei Si, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Wei Tang, Department of Electronic

Engineering, Shanghai Jiao Tong University, Shanghai, China|Xiaojun Guo, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China

This work proposes a three-dimensional stacking architecture, incorporating an active-matrix optical sensor array and a touch one based on indium gallium zinc oxide (IGZO) thin-film transistor (TFT) backplane on glass substrate, for multi-modal human-machine interactive surface. With a semi-transparent active pixel capacitive touch sensor array (~298 ppi) integrated on top of a high resolution (~500 ppi) organic photodiode optical one, multi-modal functions of full-area capacitive/optical dual-mode fingerprint authentication, and touch/3D-remote interaction are realized in one compact system. Being fully compatible with the back-end-of-line process of the TFT backplane from the semiconductor display fab, this technology is scalable for large-area/large-volume manufacturing.

04:25 PM

23-5 | Flexible Active-matrix Micro-LED Display Utilizing InSnO TFTs with High Mobility of 39.1 cm2V-1s-1 and Mass-production Compatible Process, Zuoxu Yu, School of Integrated Circuits, National ASIC System Engineering Research Center, Southeast University|Yimeng Sang, Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials, School of Electronic Science and Engineering, Nanjing University, School of Integrated Circuits, Nanjing University|Yuzhen Zhang, School of Integrated Circuits, National ASIC System Engineering Research Center, Southeast University|Yiyang Zhang, School of Integrated Circuits, Nanjing University|Runxiao Shi, School of Integrated Circuits, National ASIC System Engineering Research Center, Southeast University|Siyang Liu, School of Integrated Circuits, National ASIC System Engineering Research Center, Southeast University|Tao Tao, Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials, School of Electronic Science and Engineering, Nanjing University|Xifeng Li, Key Laboratory of Advanced Display and System Applications of the Ministry of Education, Shanghai University|Cong Peng, Key Laboratory of Advanced Display and System Applications of the Ministry of Education, Shanghai University|Rong Zhang, Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials, School of Electronic Science and Engineering, Nanjing University|Wangran Wu, School of Integrated Circuits, National ASIC System Engineering Research Center, Southeast University|Zhe Zhuang, School of Integrated Circuits, Nanjing University|Bin Liu, Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials, School of Electronic Science and Engineering, Nanjing University|Weifeng Sun, School of Integrated Circuits, National ASIC System Engineering Research Center, Southeast University

In this work, we developed InSnO (ITO) TFTs on flexible substrates and achieved a remarkable average mobility of 39.1 $cm^2V^{-1}s^{-1}$, via mass-production compatible processes utilizing SiO_2 gate dielectric. The ITO TFTs exhibit excellent wafer-scale uniformity, reliable mechanical flexibility, and robust bending durability. We fabricated flexible 2T1C pixel circuits that can operate in both PAM and PWM schemes. The flip-chip micro-LEDs (μ-LEDs) were transferred to a flexible PI holder nondestructively and present superior endurance under cyclic bending. Moreover, we bonded μ-LEDs to the pixel circuits and demonstrated a flexible active matrix μ-LED display.

04:50 PM

23-6 | Zero-bezel Flexible Active-matrix Micro-LED Display Using Through-plastic Vias and Its Seamless Tiling, Hiroshi Tsuji, NHK|Tatsuya Takei, NHK|Masashi Miyakawa, NHK|Toshihiro Yamamoto, NHK Foundation|Genichi Motomura, NHK|Yoshihide Fujisaki, NHK|Mitsuru Nakata, NHK

We developed zero-bezel flexible active-matrix micro-LED displays (160×160 pixels, 133 ppi) using through-plastic vias with intermediate connecting electrodes. Furthermore, a tiled flexible active-matrix micro-LED display was constructed by seamlessly tiling four zero-bezel displays, demonstrating the feasibility of flexible customization of display size, shape, and aspect ratio with our new display.

27 | SMB | Novel Materials and Processes for Sensors and Detectors
2:15 PM – 5:15 PM, Imperial A
Co-Chairs: Pierpaolo Palestri, University of Modena and Reggio Emilia and Eng-Huat Toh, Global Foundries

This session includes six papers dealing with innovative materials and fabrication processes for sensors as well as radiation detectors. The first paper by T.-Y. Huang et al proposes an innovative way to employ SPAD to achieve single electron detection allowing for high-speed/ultra-low-current electron microscopy imaging. The second paper by Y.-J. Park et al investigates the use of multi-step bake to mitigate the time linear white spot in CMOS image sensors. The next paper by X. Pei et al present a technique based on the Franz-Keldish effect to reconstruct the electric field profile in wide bandgap diodes. The fourth paper by C.-H. Liu et al investigates the capability of ferroelectric and partial ferroelectric materials to act as energy harvesters as well as for electrostatic energy storage. The next paper by Z. Wang et al presents a self-powered wireless sensor system featuring PtSe2 devices for molecular sensing and photodetection. Finally, the paper by S.Liu et al shows how to exploit ferroelectric materials to combine audio and video stimulus for fuzzy subject detection.

02:15 PM
27-0 | Welcome

02:20 PM
27-1 | Scintillator-free Electron Detection and Counting using Single-Photon Avalanche Diodes, Tzu-Yun Huang, National Yang Ming Chiao Tung University|Chun-Hsien Liu, National Yang Ming Chiao Tung University|Meng-Hsuan Lu, National Yang Ming Chiao Tung University|Jau Yang Wu, Yuan Ze Univerisity|Sheng-Di Lin, National Yang Ming Chiao Tung University

Single electrons counting has been demonstrated with SPAD without scintillation. An electron detection probability of ~70% at 10-keV electron is achieved, corresponding to the lowest measureable electrical current ~0.9 aA. A parameter-free EDP model is developed. This work shows the potential of SPADs for high-speed and ultralow-current electron microscopy imaging.

02:45 PM
27-2 | Time Linear White Spot Reduction Technology with Multi-Step Bake, Yun-Jeong Park, Samsung Electronics|Jun-Taek Lee, Samsung Electronics|Seul-Rim Lee, Samsung Electronics|Ki-Hoon Yun, Samsung Electronics|Hyo-Sang An, Samsung Electronics|Woon-Phil Yang, Samsung Electronics

White Spot(WS) is an important characteristic indicator of image sensor quality. Recently the Time Linear White Spot(TLWS) that occurs after test causes serious yield loss and customer claims. In this paper, we investigated thecharacteristics and causes of TLWS through WS long-term tracing, and devised Multi-Step Bake as a method to reducethe failure rate. This technology reduces yield loss by more than 50% and

maintains the effect for a long period of time,thus it is expected to reduce defect rate at the customer base.

03:10 PM
27-3 | Non-Intrusive and Precise Electric Field Sensing of High-Field Electron Devices by Franz-Keldysh Effect, Jiandong Ye, Nanjing University|Xinyi Pei, Nanjing University|Hehe Gong, Virginia Tech|Na Sun, Nanjing University|Songhao Gu, Nanjing University|Fang-Fang Ren, Nanjing University|Jianhong Zhang, Nanjing University|Zezen Liu, Nanjing University|Binggege Guo, Virginia Tech|Dawei Yan, Jiangnan University|Hai Lu, Nanjing University|Shulin Gu, Nanjing University|Xinran Wang, Nanjing University|Rong Zhang, Nanjing University|Xiaoting Jia, Virginia Tech|Yuhao Zhang, Virginia Tech

Precise sensing of electric fields (E-fields) in device regions is essential for monitoring and optimizing optoelectronic and electron devices. This is challenging for ultra-wide bandgap (UWBG) semiconductors due to high internal E-fields. Current techniques are often surface-sensitive, intrusive, or material-specific. We demonstrate a noninvasive method based on the Franz-Keldysh effect to precisely sense internal E-fields in high-voltage devices. This method maps 2-D E-field distributions with sub-micrometer resolution. Applied to UWBG Ga_2O_3 diodes, it reveals varied E-field distributions, validated by simulations and microscopy, with a maximum detection strength of 3.1MV/cm, the highest reported. This method is widely applicable across bulk semiconductors.

04:00 PM
27-4 | Energy Material for Extreme Environment: Unveiling Novel Self-Resilience of Hf1-xZrxO2 for Electrostatic Energy Storage (EES) and Pyroelectric Energy Harvesting (PEH), Cheng-Hong Liu, National Taiwan University|Kuo-Yu Hsiang, National Yang Ming Chiao Tung University|Fu-Sheng Chang, National Taiwan University|Yii-Tay Chang, National Taiwan University|Chee Wee Liu, National Taiwan University|Min Hung Lee, National Taiwan University

The antiferroelectric HfO_2-based capacitor has been proposed as dual-functional for electrostatic energy storage and pyroelectric energy harvesting for the first time. The partial-AFE has a superior power and energy density capability of $1.46x10^{10}$ W/kg and 0.96 Wh/kg, respectively. Furthermore, the harvestable energy density was experimentally measured at an outstanding 10.37 J/cm^3 within ΔT=223K. The HfO_2-based energy material is examined in low-temperature and X-ray irradiation and validates the degradation dominated by E-field cycling. There is great potential for utilizing benefits in energy storage and harvesting through the novel recovery strategy toward an unlimited lifetime of energy devices for extreme environments.

04:25 PM
27-5 | 2D PtSe2 enabled Self-powered Wireless All-in-one Transceiver-Sensor Devices, Zhehan Wang, School of Materials Science and Engineering, Southeast University|Yanling Wu, School of Materials Science and Engineering, Southeast University|Chengdong Zhao, School of Materials Science and Engineering, Southeast University|Xuyan Zhang, School of Materials Science and Engineering, Southeast University|Zhenghua Zhou, School of Materials Science and Engineering, Southeast University|Tao Xu, SEU-FEI Nano-Pico Center, Key Lab of MEMS of Ministry of Education, Southeast University, Center of 2D Materials, Southeast University|Buyun Yu, Center of Wearable RF Technology, Southeast

University|Junyuan Hu, Center of Wearable RF Technology, Southeast University|Yonghao Jia, Center of Wearable RF Technology, Southeast University|Litao Sun, SEU-FEI Nano-Pico Center, Key Lab of MEMS of Ministry of Education, Southeast University, Center of 2D Materials, Southeast University|Weisheng Li, National Laboratory of Solid-State Microstructures, School of Electronic Sci. & Eng., Nanjing University, School of Integrated Circuits, Nanjing University, Suzhou Laboratory|Weibing Lu, Center of Wearable RF Technology, Southeast University|Deji Akinwande, Microelectronics Research Center, UT Austin|Li Tao, School of Materials Science and Engineering, Southeast University, Center of 2D Materials, Southeast University, Center of Wearable RF Technology, Southeast University

We report two-dimensional $PtSe_2$ enabled Self-powered Wireless All-in-one Transceiver-Sensor (SWATS) devices outperforming existing counterparts. Benefitted from the ambipolar nature of 2D $PtSe_2$ with hole mobility up to 36 $cm^2 \cdot V^{-1} \cdot s^{-1}$, SWATS integrated molecular sensors (<50 ppb), broadband photodetectors (360-940 nm), gigahertz radio frequency (RF) circuits all in one place. Being self-powered by solar and electromagnetic energy mix collector (3 mW output) without battery. Our SWATS devices have boundless potential in unmanned vehicle, anti-terrorist or disaster-relief uniform and other occasions.

04:50 PM
27-6 | Achieving Over 2800% Superadditive Visual-Audio Multisensory Integration in-situ Ferroelectric-Semiconducting Transistor for Fuzzy Subject Detection, Shuo Liu, Peking University|Lixia Han, Peking University|Zhiyuan Wu, Peking University|Lei Xu, Peking University|Xinrui Guo, Peking University|Junling Liu, Peking University|Yu Zhu, Peking University|Peng Huang, Peking University|Linxiao Shen, Peking University|Ming He, Peking University|Ru Huang, Peking University

We experimentally demonstrate a visual-audio multisensory integration hardware based on the novel Bi_2O_2Se ferroelectric-semiconducting transistor for the first time, achieving an unprecedented superadditive response exceeding 2800% alongside the characteristics of inverse effectiveness, temporal congruency. And 10-fold increase in the data reliability via Bayesian integration rules is achieved. A visual-audio multisensory integration hardware incorporates a 12-bit DAC enabled drive circuit and a high-fidelity amplification circuit that features the generation of over-threshold pulses. This multisensory integration system is practically applied to identify distant traffic cars, reaching a perfect 99.8% accuracy in recognizing car patterns.

28 | Focus Session | Semiconductor Technology biggest and best innovations: Past to Future
2:15 PM – 5:15 PM, Imperial B
Co-Chairs:Uygar Avci, Intel and Srabanti Bhowdhury Stanford University

In this special session on Semiconductor Technology: Biggest and Best Innovations – Past to Future, we will take a comprehensive journey through groundbreaking advancements in semiconductor technology. The session features a range of topics, from transistor scaling innovations and logic technology device breakthroughs to the extreme extendibility of dual damascene technology for advanced on-chip interconnects. We will also explore the past and future of NAND flash innovations with insights and delve into DRAM optimization strategies for sub-10nm technologies. Additionally, it will provide an overview of the evolution and achievements in image sensor technology. This session promises to offer valuable perspectives on both historical milestones and future directions in semiconductor technology.

02:15 PM

28-0 | Welcome

02:20 PM
28-1 | The Incredible Shrinking Transistor - Shattering Perceived Barriers and Forging Ahead (Invited), Tahir Ghani, Intel, Pushkar Ranade, Intel Corporation

Transistor Scaling Innovations

02:45 PM
28-2 | Logic Technology Device Innovations (Invited), Carlos Diaz, TSMC

Logic Technology Device Innovation

03:10 PM
28-3 | The Extreme Extendibility of Dual Damascene Technology for MOL and BEOL On-Chip Multilevel Interconnects (Invited), Daniel Edelstein, IBM

The Extreme Extendibility of Dual Damascene Technology for MOL and BEOL On-Chip Multilevel Interconnects

04:00 PM
28-4 | DRAM Technology & Design optimization for sub-10nm and beyond (Invited), Minsoo Yoo, Hynix

DRAM Technology & Design optimization for sub-10nm and beyond

04:25 PM
28-5 | NAND flash innovations and future (Invited), Akira Goda, Micron

NAND flash innovations and future

04:50 PM
28-6 | Major Consumer Image Sensor Innovations Presented at IEDM (Invited), Albert Theuwissen, Harvest Imaging

Image Sensors past, and progress made over the years

20 | MT | Selector Based and Charge-trap Base Memories
2:15 PM – 5:40 PM, Grand Ballroom A
Co-Chairs:Andrea Redaelli, ePCM process architecture technical director – Fellow at STMicroelectronics and Swati Saha, Infineon

Threshold voltage selector-based memories and Charge-trap based memories advancements are discussed in the session. The first part of the session focus on selector-base memories, with the first paper dealing with the integration, by Kioxia and SKHynix, of a STT-MRAM in a 64 Gb cross-point array. The other two papers deal with Ovonic Threshold Switches (OTS) used as programmable memories: the

second one, by Micron, is about the origin of the memory window, while the third, by POSTECH, presents a method to achieve multi-bit operation. The second part of the session focuses on charge-trap memories. The first paper on charge trap based memory is from SKHynix which discusses about achieving 5b MLC cell in 3D-NAND by improving the Vt control per level by utilizing a 'Bi-directional Step-Pulse-Program (BSPP)' algorithm. The second paper from Samsung studies insertion of Boron-Nitride (BN) layer into the SiN charge trapping layer (CTL) in 3D NAND for better operating window and retention as well as significantly faster erase performance. The third paper from Zhejiang University proposes a novel dual-bit Charge-trap flash cell structure with small cell size for application on both embedded and stand alone flash. The last paper from POSTECH is a novel design to use oxide semiconductor channel to improve mobility and current in 3D NAND.

02:15 PM
20-0 | Welcome

02:20 PM
20-1 | Reliable memory operation with low read disturb rate in the world smallest 1Selector-1MTJ cell for 64 Gb cross-point MRAM, Hisanori Aikawa, Kioxia Korea Corporation|Jeonghwan Song, SK hynix|Toshihiko Nagase, Kioxia Korea Corporation|Soo Man Seo, SK hynix|Yuichi Ito, Kioxia Korea Corporation|Tae Jung Ha, SK hynix|Kenichi Yoshino, Kioxia Korea Corporation|Bo Kyung Jung, SK hynix|Tadaaki Oikawa, Kioxia Korea Corporation|Ku Youl Jung, SK hynix|Su Jin Chae, SK hynix|Bum Su Kim, SK hynix|Min Chul Shin, SK hynix|Dong Keun Kim, SK hynix|Tae Ho Kim, SK hynix|Kosuke Hatsuda, Kioxia Corporation| Katsuhiko Hoya, Kioxia Corporation|Soo Gil Kim, SK hynix|Jae Yun Yi, SK hynix|Seon Yong Cha, SK Hynix

For the first time, we demonstrate reliable 1 selector-1 MTJ (1S1M) cell read/write operation with low read disturb rate of <1E-6 in 64 Gb cross-point array architecture. We have implemented cross-point 1S1M chips integrated in Half Pitch (HP) of 20.5 nm and MTJ CD of 20 nm using As-doped SiO_2 selector and perpendicularly magnetized MTJ (p-MTJ). A novel read scheme utilizing transient behavior of selector along with the low capacitance circuitry enables us to overcome MTJ read disturb easily occurred when the selector turns on in scaled 1S1M cells.

02:45 PM
20-2 | VT window model of the Single-chalcogenide Xpoint Memory (SXM), Paolo Fantini, Micron Technology Inc.|Andrea Ghetti, Micron Technology Inc.|Enrico Varesi, Micron Technology Inc.|Agostino Pirovano, Micron Technology Inc.|Dario Baratella, University of Milano-Bicocca|Chiara Ribaldone, University of Milano-Bicocca|Davide Campi, University of Milano-Bicocca|Marco Bernasconi, University of Milano-Bicocca|Roberto Bez, Micron Technology Inc.

The physics mechanism behind the polarity effect at the basis of the Single-chalcogenide Xpoint Memory (SXM) is investigated through dedicated experiments, DFT-based atomistic models and TCAD simulations.This is the first physically based model able to explain the basic functional characteristics of the SXM memory technology.

03:10 PM

20-3 | Achieving 3-bit Operation in Selector-only-memory by Controlling Variability with Microwave Annealing and Bipolar Pulse Scheme, Laeyong Jung, POSTECH|Jangseop Lee, POSTECH|Yoori Seo, POSTECH|Hyunsang Hwang, POSTECH

We propose method for multi-bit operation in SOM. To mitigate V_{th}overlap between states, we enhance uniformity and controllability of V_{th}. Uniformity improvement is achieved by reducing traps involved in memory switching through MWA and bipolar pulse scheme. MWA's vibrational energy eliminates weak homopolar bonding of Se, and the bipolar pulse scheme reduces V_{th} variability by deactivating traps with low trap energy. Moreover, mean value of V_{th} was modulated as varying bipolar pulse magnitude. Our results confirm 2-bit operation. Furthermore, we confirmed feasibility of 3-bit with tight V_{th} distribution using cross-point array device and optimized P/E conditions.

03:35 PM
20-4 | Penta-level charge trap-based 3D NAND flash memory enabled by bi-directional step-pulse-programming and improvement of cell channel process, Changhyun Lee, SKhynix America Inc|Dengtao Zhao, SKhynix America Inc|Kyeongran Yoo, SKhynix America Inc|Mohammad Sharbati, SKhynix America Inc|Paing Htet, SKhynix America Inc|Yunsu Kim, SKhynix Inc|Bongyeol Park, SKhynix Inc|Hansoo Joo, SKhynix Inc|Hyeokjun Choi, SKhynix Inc|Soonok Seo, SKhynix Inc|Dawon Kim, SKhynix Inc|Jaewoong Kim, SKhynix Inc|Taeun Youn, SKhynix Inc|Insu Park, SKhynix Inc|Jaesung Sim, SKhynix Inc|Seongjo Park, SKhynix Inc|Sungtaeg Kang, SKhynix America Inc|Jungdal Choi, SKhynix America Inc, SKhynix Inc

We present PLC (Penta-level cell, 5 bits/cell)NAND flash memory using 3D charge-trap-flash (CTF) cell.To achieve PLC cell distribution with proper cell read margin,program noise and short-term data retention (STDR) areaddressed as most challenging factors. To make path of chargetrap cell for PLC NAND, new program algorithm named as"Bi-directional Step-Pulse-Program (BSPP)" is proposed tomanage STDR effect and implemented into our 5th generation4D NAND. The BSPP program algorithm improves readwindow by 67% than the conventional one.

04:25 PM
20-5 | Spatial Charge Trap Engineering with Boron Nitride Barrier for 3D V-NAND Flash Memory, Dae Hyun Kang, KAIST|Jae Joong Jeong, KAIST|Young Keun Park, KAIST|Dong Hun Sin, Semiconductor R&D Center, Samsung Electronics|Han Mei Choi, Semiconductor R&D Center, Samsung Electronics|Byung Jin Cho, KAIST

Spatial charge trap engineering using amorphous BN energy barrier for 3D V-NAND flash memory device is presented. A 1 nm thick BN layer is inserted within a SiN CTL using ALD process. The CTL with the BN barrier located at an optimized position showed clear advantages in memory window and charge retention. The advantage of the BN barrier becomes more apparent when CTL is scaled down to 4 nm, having larger memory window, improvement in hole retention, and faster erase speed compared to the same thickness of pure SiN CTL, which helps to advance XY-scaling in 3D V-NAND flash devices.

04:50 PM
20-6 | A Novel Dual-Bit Charge Trapping Flash Cell with Operation Optimization for Standalone and Embedded Universal Applications, Zhexuan Li, Zhejiang University|Xiao Yu, Beijing PXMicro Technology Co., LTD.|Kun Ren, Zhejiang University, Zhejiang ICsprout Semiconductor Co., Ltd.|Dianyu Qi, Zhejiang

University, Zhejiang ICsprout Semiconductor Co., Ltd.|Chunsheng Jiang, Guangxi Normal University|Zhengdong Shi, Beijing PXMicro Technology Co., LTD.|Yongyu Wu, Zhejiang ICsprout Semiconductor Co., Ltd.|Guangji Li, Zhejiang ICsprout Semiconductor Co., Ltd.|Yunhao Zhang, Zhejiang ICsprout Semiconductor Co., Ltd.|Zhiqiang Su, Beijing PXMicro Technology Co., LTD.|Jun Xu, Tsinghua University|Dawei Gao, Zhejiang University, Zhejiang ICsprout Semiconductor Co., Ltd.|Liyang Pan, Beijing PXMicro Technology Co., LTD., Tsinghua University

A novel dual-bit CTF cell with a self-aligned middle select-gate is proposed. Combined with the dedicatedly-designed array architecture, the smallest 0.03μm^2 bit size is demonstrated with 55nm process. Operation optimization with DCHE programming is conducted to mitigate the TCME. Furthermore, CHH effect is observed experimentally for the first time, achieving faster erasure speed, larger MW, and wider hole distribution compared with BBHH erasure, resulting in better reliability combined with DCHE scheme. Process verification and measured results show that the smallest bit size is achieved with good cell performance and lower process cost, making it promising for standalone and embedded memories.

05:15 PM
20-7 | Electrically Erasable Oxide-Semiconductor-Channel Charge Trap Flash Memory with Unipolar Operation, Seongmin Park, POSTECH|Chanyeong Go, POSTECH|Changmin Jeon, Samsung Electronics Co.|Yoonyoung Chung, POSTECH

In this work, we first demonstrate the electrically erasable oxide-semiconductor-channel charge trap flash (OSCTF) memory. To address the hole shortage inherent in the oxide semiconductor, we inverted the gate stack and positioned a hole supplier on the gate. Additionally, we developed a novel operating method that employs unipolar positive pulses for both program and erase operations to prevent channel floating. The OSCTF memory, featuring the unique strategy, exhibited complete program/erase operation with a memory window of 4.9 V. This work opens the potential of oxide semiconductors as channel materials for charge trap flash memory.

26 | MS | Multi-scale Modeling of Transport, Interconnects and Reliability
2:15 PM – 5:40 PM, Continental 7 – 9
Co-Chairs: Dipanjan Basu, Synopsys and Andries Scholten, Fellow at NXP

This session starts with two cryogenic papers, one investigating ballistic limits of III-V HEMTs and the other exploring interconnects needed for quantum computers. Then, we have an invited paper of J. Vuckovic on recent breakthroughs in photonics design. Next, we have two papers demonstrating multi-scale modeling of thermal effects. We conclude with two reliability simulation papers – one comparing Si and 2D materials, the other analyzing BTI for oxide power transistors in BEOL voltage converters.

02:15 PM
26-0 | Welcome

02:20 PM
26-1 | Ballistic transport in state-of-the art In0.65Ga0.35As/In0.52Al0.48As quantum-well high-electron-mobility transistors at room and cryogenic temperatures, Seung-Woo Son, Kyungpook National University|In-Geun Lee, Kyungpook National University|Min-Seo Yu, Kyungpook National

University|Su-Min Choi, Kyungpook National University|Yong-Soo Jeon, Kyungpook National University|Sang-Phyeong Son, Kyungpook National University|Ji-Hoon Yoo, Kyungpook National University|Jae-Hak Lee, Kyungpook National University|Kyunghoon Yang, KAIST|Dae-Hyun Kim, Kyungpook National University

This paper presents a systematic analysis on ballistic transport in state-of-the art $In_{0.65}Ga_{0.35}As$ QW HEMTs at room and cryogenic temperatures. Our work clearly highlights the important role of ballistic mobility in state-of-the art $In_xGa_{1-x}As$ QW HEMTs from 300 K to 4 K, revealing that quantum-mechanical ballistic transport and channel degeneracy must be taken into account in the course of device modeling and characterization.Furthermore, we propose a methodology to graphically pinpoint whether carrier transport is governed by conventional diffusive transport or by near-ballistic transport in terms of channel carrier degeneracy and L_g at 300 K to 4 K.

02:45 PM
26-2 | Exploration and Analysis of Metallic, Optical, and Superconducting Cryo-Interconnects for Large-Scale Quantum Computers, Ankit Kumar, University of California, Santa Barbara|Aaron Kim, University of California, Santa Barbara|Kunjesh Agashiwala, University of California, Santa Barbara|Lin Xu, University of California, Santa Barbara|Arnab Pal, University of California, Santa Barbara|Wei Cao, University of California, Santa Barbara|Kaustav Banerjee, University of California, Santa Barbara

In this work, we comprehensively explore and analyze interconnect technologies to realize large-scale quantum computing. We determine the best interconnect materials for cryogenic interface electronics (CIE) based on required current density and wire geometry among metals, doped-multilayer-graphene (DMLG) as well as superconductors (SC), and then evaluate various transistor and interconnect technology combinations for CIE. This is followed by analyzing the heat loads (Q) across interconnects (or cables) used to transmit signals across different temperature zones in the dilution refrigerator (DR). Our results indicate the optical-fiber cables are key in realizing large-scale quantum computing beyond 10^3 qubits.

03:10 PM
26-3 | Scalable classical and quantum photonics (Invited), Jelena Vuckovic, Stanford University

Recent breakthroughs in photonics design, along with new nanofabrication approaches and heterogeneous integration play crucial roles in building photonics for applications including optical interconnects and quantum technologies.

04:00 PM
26-4 | AI-Accelerated Atoms-to-Circuits Thermal Simulation Pipeline for Integrated Circuit Design, Alexander Gabourie, DeepSim, Inc.|Carlos Polanco, University of California, Davis|Connor McClellan, DeepSim, Inc.|Haotian Su, Stanford University|Mohamadali Malakoutian, Stanford University|Cagil Koroglu, Stanford University|Srabanti Chowdhury, Stanford University|Davide Donadio, University of California, Davis|Eric Pop, Stanford University

We present the first AI-accelerated, atoms-to-circuits thermal simulation pipeline. Our approach is based on *ab initio*, atomistic materials modeling and scales to full-detail, nanoscale resolution simulations of

circuits, outperforming existing tools in accuracy and speed. We demonstrate its capabilities via temperature predictions of Intel 16 FinFETs and a RISC-V core.

04:25 PM
26-5 | Fast Prediction of Spatio-Temporal Temperature Profiles in FinFET Arrays via Numerical and Machine-Learning Approaches, Mingeun Choi, Georgia Institute of Technology|Rinku Dutta, Georgia Institute of Technology|Priyabrata Saha, Georgia Institute of Technology|Mayur Singh, Georgia Institute of Technology|Saibal Mukhopadhyay, Georgia Institute of Technology|Suman Datta, Georgia Institute of Technology|Satish Kumar, Georgia Institute of Technology

Quantifying the spatio-temporal thermal response in FinFET arrays is crucial due to the detrimental impact of the self-heating effect (SHE) on reliability. However, thermal models which are computationally efficient and which can predict temperature at high spatio-temporal resolution are rare. This paper presents a highly efficient, three-dimensional (3D) multi-scale time-dependent temperature prediction model for 14 nm node bulk FinFET arrays, considering nanoscale thermal resistances and cross-coupling among FinFETs.Benchmarking shows that this model accelerates transient temperature prediction by 2348 times compared to the conventional Fluent-based simulations.

04:50 PM
26-6 | MARS: a Multiscale Ab initio Reliability Simulator for Advanced Si and 2D Material Based MOSFETs, Yue-Yang Liu, Institute of Semiconductors, Chinese Academy of Sciences|Guang-Hua Xu, School of Microelectronics, Fudan University|Tao Xiong, Institute of Semiconductors, Chinese Academy of Sciences|Wen-Feng Li, Institute of Semiconductors, Chinese Academy of Sciences|Yu Zhao, Institute of Semiconductors, Chinese Academy of Sciences|Ting-Wei Liu, Institute of Semiconductors, Chinese Academy of Sciences|Zirui Wang, School of Integrated Circuits, Peking University|Runsheng Wang, School of Integrated Circuits, Peking University| Lin-Wang Wang, Institute of Semiconductors, Chinese Academy of Sciences|Xiangwei Jiang, Department of Mathematical and Physical Sciences, National Natural Science Foundation of China

We propose an accurate reliability simulator, MARS (Multiscale *Ab initio* Reliability Simulator), that works for both industrial Si MOSFET and emerging two-dimensional material FET. It has the following features and advantages: (1) All the defect fingerprints are obtained by *ab initio* calculations on atomistic interfaces models. (2) The Marcus charge transfer theory is adopted to calculate the charge trapping/emission rates, and no empirical parameter or approximation is used. (3) It is able to simulate both BTI and HCD issues in Si MOSFETs, and the hysteresis issue in 2D FETs. (4) Excellent agreements between simulation and experimental data are presented.

05:15 PM
26-7 | Bias Temperature Instability Analysis of Oxide Power Transistors for BEOL On-chip Voltage Converter in Thermally-Constrained H3D Systems, Jungyoun Kwak, Georgia Institute of Technology|Jaewon Shin, Georgia Institute of Technology |Sunbin Deng, Georgia Institute of Technology |Gyujun Jeong, Georgia Institute of Technology |Janak Sharda, Georgia Institute of Technology |Suman Datta, Georgia Institute of Technology |Shimeng Yu, Georgia Institute of Technology

This paper introduces a framework for analyzing Bias-temperature instability (BTI)-induced aging and thermal management in High-voltage IWO power FETs for BEOL on-chip converters in H3D systems. AC

stress is measured and ML-assisted BTI compact model is developed for circuit-level aging simulation. Logic-on-Memory reduces peak temperatures compared to Memory-on-Logic.

21 | Focus Session | Leading Semiconductor Products and Advanced Packaging
2:15 PM – 6:05 PM, Grand Ballroom B
Co-Chairs: Youseok Suh, Qualcomm and Tenko Yamashita, IBM

As we navigate the dynamic landscape of semiconductor technology, we are on the cusp of a major transition to new leading nodes set to revolutionize production by 2024–2025. This session will delve into the cutting-edge advancements that are shaping the future of semiconductor design and packaging. We will explore topics ranging from the co-optimization of GPU AI chips and heterogeneous computing platforms to the next-generation SoC platforms and innovative wafer bonding techniques. Our distinguished speakers from Nvidia, AMD, Qualcomm, POSTEC, TSMC, Intel, TEL, and IBM will provide insights into how these technological strides are driving the evolution of high-performance computing and advanced AI

02:15 PM
21-0 | Welcome

02:20 PM
21-1 | Systematic Co-Optimization of GPU AI Chip From Process Technology, Chip Design, System and Algorithms (Invited), John Hu, Nvidia Corporation|Louis Liu, Nvidia Corporation|Shuhan Liu, Nvidia Corporation, Stanford University|Boonkhim Liew, Nvidia Corporation|David Guan, Nvidia Corporation|James Chen, Nvidia Corporation|Steven Jones, Nvidia Corporation|William Dally, Nvidia Corporation

Co-optimization of GPU from technology, design, system and algorithms has enabled 1000x AI compute in 10 years. DFM/DFR enables optimal performance, power and yield, and achieves defects per trillion perfections in today's GPU with 100s billion transistors and in large language model application that runs thousands GPU as ONE

02:45 PM
21-2 | Coevolution of Chiplet Technology and Cache Architecture for AI and Compute (Invited), John Wuu, AMD|Mike Mantor, AMD|Gabriel Loh, AMD|Alan Smith, AMD|Dave Johnson, AMD|David Fisher, AMD|Brett Johnson, AMD|Carson Henrion, AMD|Russell Schreiber, AMD|Jeff Lucas, AMD|Stephen Dussinger, AMD|Alistair Tomlinson, AMD|Will Walker, AMD|Paul Moyer, AMD|Deepak Kulkarni, AMD|Daniel Ng, AMD|Wonjun Jung, AMD|Raja Swaminathan, AMD|Samuel Naffziger, AMD

Last level cache (LLC) is an important component to processor compute performance. As it often occupies a non-trivial percentage of SOC die area, it presents co-optimization opportunities with chiplet technology development. On the CPU side, server LLC advances culminated in the hybrid-bonded AMD 3D V-Cache™, for which highlights from the first and second-generation products are summarized. On the GPU side including AI accelerators, the progression of the AMD Infinity Cache™ LLC from planar to 2.5D chiplets to 3.5D integration is tracked. The products combine to showcase the possibilities that symbiotic co-development between cache architecture and chiplet technology can realize in further propelling AI and compute performance.

03:10 PM

21-3 | Heterogeneous Computing Platform for Power-Performance Efficient On-Device AI (Invited), Jie Deng, Qualcomm|Giri Nallapati, Qualcomm

Abstract — This paper explores the rapid growth of on-device AI and the crucial role of heterogeneous computing in addressing the increasing performance demands and power challenges of edge computing. Innovations in processor design and System-Technology-Co-Optimization (STCO), exemplified by the Snapdragon®8 Gen 4, have significantly enhanced performance and power efficiency. However, sustaining power-perf-cost efficiency as technology scales presents an ongoing challenge.

03:35 PM

21-4 | Ultra-stacked Forksheet-FET and Monolithic Complementary-FET for Å7~5 node Visibility (Invited), Rockhyun Baek, Pohang University of Science and Technology (POSTECH), Pohang University of Science and Technology (POSTECH)|Junjong Lee, Pohang University of Science and Technology (POSTECH)|Seungjoon Eom, Pohang University of Science and Technology (POSTECH)|Minchan Kim, Pohang University of Science and Technology (POSTECH)|Yonghwan Ahn, Pohang University of Science and Technology (POSTECH)|Seunghwan Lee, Pohang University of Science and Technology (POSTECH)|Jinsu Jeong, Pohang University of Science and Technology (POSTECH)|Sanguk Lee, Pohang University of Science and Technology (POSTECH)

For the first time, we comprehensively compared the competitiveness of ultra-stacked forksheet-FET (FS) and monolithic complementary-FET (CF) for Å7~5 nodes. Assuming nanosheet-FET (NS) in Å10 node, ultra-stacked (>4) FS does not show meaningful area scaling over 4stack FS (FS_4) in high-density (HD) applications of Å7. However, in high-performance (HP) of Å7, FS_5 shows a large scaling over FS_4 with small performance (Perf) degradation. CF_3 still has a smaller area than FS_5 but has worse Perf and larger process cost (PC), undermining the PPAC (Power-Perf-Area-Cost) of CF_3. In Å5, however, FS can be replaced by CF_4 or functional symmetry CF (CF_S) in terms of PPA.

04:25 PM

21-5 | Next Generation TSMC-SoIC® Platform for Ultra-High Bandwidth HPC Application (Invited), Yen-Ming Chen, TSMC|T. Ko, TSMC|K. C. Ting, TSMC|S. K. Goel, TSMC|A. Patidar, TSMC|K. H. Tam, TSMC|K. Huang, TSMC|W. P. Changchien, TSMC|W. Y. Wang, TSMC|C. Y. Huang, TSMC|C. H. Wang, TSMC|W. Lai, TSMC|B. Z. Chen, TSMC|Y. H. Lung, TSMC|S. C. Lin, TSMC|S. F. Yeh, TSMC|C. W. Shih, TSMC|T. J. Wu, TSMC|Y. C. Lin, TSMC|Y. H. Chen, TSMC|C. H. Hsieh, TSMC|T. Y. Chen, TSMC|H. Y. Pan, TSMC|T. S. Lin, TSMC|C. C. Hu, TSMC|C. Bair, TSMC|S. B. Jan, TSMC|L.C. Hung, TSMC|C. H. Yao, TSMC|T. C. Huang, TSMC|J. H Shieh, TSMC|W. C. Chiou, TSMC|Frank Lee, TSMC|L. C. Lu, TSMC|K. C. Hsu, TSMC

This work introduces the next generation System-on-Integrated-Chips (SoIC) 3D stacking technology, facilitating ultra-high bandwidth density between stacked dies, with device performance remaining stable. This innovative 3D technology, with TSMC's cutting-edge System-on-Chip nodes and advanced package solutions, pushes the boundaries of Moore’s Law for the next generation of High-Performance Computing applications

04:50 PM

21-6 | Tomorrow's Modular & Scalable Compute Systems (Invited), Johanna Swan, Intel|Aleksandar Aleksov, Intel|Georgios Dogiamis, Intel|Adel Elsherbini, Intel

The demand for AI solutions across markets requires software-hardware co-optimization with a focus on system performance and energy efficiency with affordability. To achieve manufacturing at scale, three key packaging thrusts require focus on fungible solution enablement: i) advanced memory integration to eliminate capacity, bandwidth and latency bottlenecks, ii) utilization of hybrid bond (HB) interconnect pitch scaling to access power-efficient, bandwidth density between heterogeneous components, and iii) modularity and system expansion with connectivity to avoid networked latency and bandwidth limitations. The combination of these elements while utopian in vision face numerous challenges which need addressed.

05:15 PM
21-7 | Implications of Wafer Bonding for Advanced Logic Technology Development (Invited), Sitaram Arkalgud, TEL|Christopher Netzband, TEL|Andrew Tuchman, TEL|Yoshihiro Kondo, TEL|Hirokazu Aizawa, TEL|Ilseok Son, TEL|Angelique Raley, TEL

3DI and Heterogenous Integration (HI) have established themselves in the semiconductor industry over the past decade with FPGAs, BSI CMOS Image Sensors, HPC GPUs and High Bandwidth Memory entering volume production. The primary characteristics of 3DI and HI are the use of wafer or die bonding, TSVs and thinning. With these advanced packaging (AP) technologies becoming more mainstream and with device scaling reaching fundamental limits, scaled AP technologies (bonding, thinning, TSV) are now being incorporated into both BEOL and FEOL semiconductor processing to achieve higher performance, bandwidth and/or density. This presentation focuses on the challenges associated with fusion wafer bonding in advanced logic applications.

05:40 PM
21-8 | D2W and W2W Hybrid bonding system with below 2.5 micron pitch for 3D chiplet AI applications (Invited), Katsuyuki Sakuma, IBM Research|Roy Yu, IBM Research|Nick Polomoff, IBM Research|Arvind Kumar, IBM Research|Sathya Raghavan, IBM Research|Michael Belyansky, IBM Research|Aakrati Jain, IBM Research|Ravi Bonam, IBM Research|Yasir Sulehria, IBM Research|Hsianghan Hsu, IBM Research|Kishan Jayanand, IBM Research|Hemanth Jagannathan, IBM Research

Hybrid bonding is an emerging ultra-fine pitch interconnect joining technology for multi-chip/multi-stack high performance chiplet systems. With sub-μm contact sizes, it is projected to achieve ~10^6/mm^2 interconnection densities, as needed for these systems. Aspects of system density, performance, functionality, reliability all feed into the co-optimized system architecture, thermal budget, design, process, and materials. In this paper, we discuss the latest developments in bonding surface topography and cleanliness vs. protection and handling, for dielectric and metal density related bonding. We examine the metal-metal solid-state fusion performance by grain structure distributions, along with other design, thermal, and process issues and solutions for < 2.5 mm pitch (1.6 ´ 10^5/mm^2) die-to-die (D2D), die-to-wafer (D2W), and wafer-to-wafer (W2W) hybrid bonded systems.

24 | EDT | Advancements in 2D Material Devices
2:15 PM – 6:05 PM, Continental 5

Co-Chairs: Nazila Haratipour, Principal Engineer at Kepler Computing and Farnaz Niroui, MIT

This two-dimensional material session features eight papers that span from growth to device fabrication and system integration, showcasing significant advancements in the field. Samsung Electronics kicks off with a report on the 8” direct growth of single-crystalline MoS2 on high-k dielectrics, leading to high-performing transistors and paving the way for high-volume manufacturing. The next three papers focus on advancements in gate and contact modules to enhance device performance. IMEC discusses interfacial engineering for improved WSe2-based pFET devices. Intel presents a unique gate oxide process that improves scaled gate-all-around 2D NMOS and PMOS device performance. TSMC reports p-type contact engineering through substitutional doping and alloying. Next, MIT and Samsung Electronics introduce novel integration schemes for multi-channel 2D transistors. Nanjing University presents a monolayer MoS2 transistor scaled to a 40 nm contacted gate pitch, corresponding to the 1 nm node. The session concludes with a presentation by TSMC on a lower-power CMOS inverter implemented with enhancement-mode operation on a monolayer 2D material channel.

02:15 PM
24-0 | Welcome

02:20 PM
24-1 | Direct growth and manufacturing of single-crystalline 2D FETs on 8-inch Si wafers, Min Seok Yoo, Samsung Advanced Institute of Technology, Samsung Electronics|Alum Jung, Samsung Advanced Institute of Technology, Samsung Electronics|Suk Yang, Semiconductor R&D Center, Samsung Electronics|Joung Eun Yoo, Samsung Advanced Institute of Technology, Samsung Electronics|Eun-Kyu Lee, Samsung Advanced Institute of Technology, Samsung Electronics|Kyung-Eun Byun, Samsung Advanced Institute of Technology, Samsung Electronics|Jaeyoon Baik, Beamline Division, Pohang Accelerator Laboratory, POSTECH|Dong-Jin Yun, Samsung Advanced Institute of Technology, Samsung Electronics|Jaehyun Park, Semiconductor R&D Center, Samsung Electronics|Jeehwan Kim, Samsung Advanced Institute of Technology, Samsung Electronics, Research Laboratory of Electronics, Massachusetts Institute of Technology|Minsu Seol, Samsung Advanced Institute of Technology, Samsung Electronics

While 2D transition metal dichalcogenides (TMDs) are seen as promising next-generation channel materials to overcome the scaling limitations of Si, their commercialization requires processes for directly growing single-crystalline (SC) 2D TMD channels on high-k gate dielectrics and fabricating devices. This study presents a method for directly growing 2D MoS_2 on AlO and HfO gate dielectrics using MOCVD, achieving selectively grown, SC-channels on 200 mm wafers. Our direct-grown SC-MoS_2 exhibited on-current up to 419.0 μA/μm and nearly 100% yield at 500 nm channel length.

02:45 PM
24-2 | The critical role of 2D TMD interfacial layers for pFET performance, Tien Dat Ngo, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Xiangyu Wu, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Chelsey Dorow, Intel Foundry Technology Research, Intel Corporation, Hillsboro, OR 97214, USA |Robert Kimes Grubbs, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Luis Pinotti, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Daire Cott, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Kaustuv Banerjee, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Henry Medina Silva, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Ilse Hoflijk, imec, Remisebosweg 1, B-3001 Leuven,

Belgium|Anja Vanleenhove, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Inge Vaesen, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Thierry Conard, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Souvik Ghosh, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Olivier Richard, imec, Remisebosweg 1, B-3001 Leuven, Belgium|FionaCrystal Mascarenhas, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Luca Mana, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Danielle Vanhaeren, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Thomas Nuytten, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Fengben Xi, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Kirby Maxey, Intel Foundry Technology Research, Intel Corporation, Hillsboro, OR 97214, USA |Azimkhan Kozhakhmetov, Intel Foundry Technology Research, Intel Corporation, Hillsboro, OR 97214, USA |Nazmul Arefin, Global Sourcing for Equipment and Materials, Intel Corporation, Hillsboro, OR 97214, USA|Sergej Pasko, AIXTRON SE, Herzogenrath 52134, Germany|Simonas Krotkus, AIXTRON SE, Herzogenrath 52134, Germany|Jan Mischke, AIXTRON SE, Herzogenrath 52134, Germany|Salim EL Kazzi, AIXTRON SE, Herzogenrath 52134, Germany|Matthew Metz, Intel Foundry Technology Research, Intel Corporation, Hillsboro, OR 97214, USA |Kevin O'Brien, Intel Foundry Technology Research, Intel Corporation, Hillsboro, OR 97214, USA |Uygar Avci, Intel Foundry Technology Research, Intel Corporation, Hillsboro, OR 97214, USA |Cesar Javier Lockhart de la Rosa, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Gouri Sankar Kar, imec, Remisebosweg 1, B-3001 Leuven, Belgium|Bogdan Govoreanu, imec, Remisebosweg 1, B-3001 Leuven, Belgium

We present developments in 2D TMD interface engineering, highlighting the interfacial layer's critical role in WSe_2-based pFETs. We demonstrate the first use of native oxide formed by 'sacrificial' WSe_2 oxidation for nucleating high-k gate-stack. Novel co-seeding method achieves controllable p-type doping, enhancing on-currents by 10x with on/off ratios of ~10^7.

03:10 PM

24-3 | Gate oxide module development for scaled GAA 2D FETs enabling SS<75mV/d and record Idmax>900µA/µm at Lg<50nm, Wouter Mortelmans, Intel|Pratyush Buragohain, Intel|Ande Kitamura, Intel|Chelsey Dorow, Intel|Carly Rogan, Intel|Lutfe Siddiqui, Intel|Rahul Ramamurthy, Intel|Jennifer Lux, Intel|Ting Zhong, Intel|Shane Harlson, Intel|Eric Gillispie, Intel|Tyrone Wilson, Intel|Raphael Toku, Intel|Adedapo Oni, Intel|Ashish Penumatcha, Intel|Mahmut Kavrik, Intel|Marc Jaikissoon, Intel|Kirby Maxey, Intel|Azimkhan Kozhakhmetov, Intel|Chi-Yin Cheng, Intel|Chia-Ching Lin, Intel|Sudarat Lee, Intel|Andrey Vyatskikh, Intel|Nazmul Arefin, Intel|David Kencke, Intel|Joshua Kevek, Intel|Tristan Tronic, Intel|Matthew Metz, Intel|Scott Clendenning, Intel|Kevin O'Brien, Intel|Uygar Avci, Intel

This work builds on existing research to improve viability of 2D TMD semiconductors as replacement for ultra-scaled Si transistors. We focus on GAA 2D N-/PMOS with scaled Lg (=S-to-D distance) down to 30nm. Our unique gate oxide process and cleans show improved interface quality over channel and contacts, resulting in improved device performance with record SS<75mV/dec and Idmax>900 µA/µm at Lg<50nm using monolayer MoS_2. The median DIBL at Lg~60nm is 17mV/V but increases to 177mV/V at Lg~30nm attributed to short channel effects. This shows continued advancements on interface control and EOT scaling are needed to bridge the gap with Si.

04:00 PM

24-4 | Bilayer Alloy Contacts for High-Performance p-Type 2D Semiconductor Transistors, Amin Azizi, Corporate Research, TSMC, San Jose, CA, USA|Goutham Arutchelvan, Corporate Research, TSMC, Hsinchu, Taiwan|Nathaniel Safron, Corporate Research, TSMC, San Jose, CA, USA|Chih-Piao Chuu,

Corporate Research, TSMC, Hsinchu, Taiwan|Yangjin Lee, University of California, Berkeley, CA, USA|Mehmet Dogan, University of California, Berkeley, CA, USA |D. Mahaveer Sathaiya, TCADD, TSMC, Hsinchu, Taiwan|H.-S. Philip Wong, Corporate Research, TSMC, Hsinchu, Taiwan|Marvin Cohen, University of California, Berkeley, CA, USA|Alex Zettl, University of California, Berkeley, CA, USA|Iuliana Radu, Corporate Research, TSMC, Hsinchu, Taiwan

Notable progress has been reported for n-type contacts to 2D materials, either through doping or through careful choice of contact metals. Here, we report on p-type contact engineering via substitutional doping and alloying. We tune the dopant concentration from lightly to heavily doped WSe_2. We demonstrate that 2L TMD alloy can reach degenerate doping density for WSe_2. The degenerate doping plays a critical role in lowering contact resistance (R_c) to metal. Extracted R_c is ~98 Ω·μm for a $sR_{sh}$of 4.5 kΩ/sq, independent of V_g. Pd/alloy contacts show superior thermal stability when compared to typical semimetal contacts (Bi and Sb).

04:25 PM
24-5 | Enhancement-Mode Multichannel MoS2 Transistor with Spacer Engineering and Design-Technology Co-Optimization Based on the 8" Platform, Jiadi Zhu, Massachusetts Institute of Technology|Aijia Yao, Massachusetts Institute of Technology|Peng Wu, Massachusetts Institute of Technology|Yixuan Jiao, Massachusetts Institute of Technology|Ji-Hoon Park, Massachusetts Institute of Technology|Jianfeng Jiang, Massachusetts Institute of Technology|Tilo Yang, Massachusetts Institute of Technology|Ayush Gupta, Massachusetts Institute of Technology|Suraj Cheema, Massachusetts Institute of Technology|Jing Kong, Massachusetts Institute of Technology|Tomas Palacios, Massachusetts Institute of Technology

A novel integration scheme for multichannel MoS_2 transistors (MCTs) enabled by low-temperature synthesis is demonstrated on 8" wafers with self-aligned source/drain contacts, multiple gate-dielectric-MoS_2-dielectric-gate layers, reduced lithography steps and no sacrificial layers. 1-channel MCT feature 386μA/μm I_{ON}at V_{DS}=1V, SS=85mV/dec, DIBL=28mV/V. We report the first functional high-performance 2-channel MCT with 673μA/μm I_{ON} and 88mV/dec SS at 400nm L_{Ch}. Local-back gate transistors with 1.5nm physical-oxide-thickness and 4nm L_{CH} were fabricated to calibrate device models at extreme scales for design-technology co-optimization (DTCO), which projects MCTs scaling, including power and performance for "1 nm" technology node and beyond.

04:50 PM
24-6 | Transfer free 2D CMOS multi bridge channel FET, Changhyun Kim, Samsung Advanced Institute of Technology|Junyoung Kwon, Samsung Advanced Institute of Technology|Min Seok Yoo, Samsung Advanced Institute of Technology|Hyun Mi Lee, Samsung Advanced Institute of Technology|Eunji Yang, Samsung Advanced Institute of Technology|Eun-Kyu Lee, Samsung Advanced Institute of Technology|Hyungjun Youn, Samsung Advanced Institute of Technology|Baekwon Park, Samsung Advanced Institute of Technology|Huije Ryu, Samsung Advanced Institute of Technology|Yoonhoo Ha, Samsung Advanced Institute of Technology|Haesung Kim, Samsung Advanced Institute of Technology|Woong Ko, Samsung Advanced Institute of Technology|Dongmin Kim, Samsung Advanced Institute of Technology|Dong-jin Yun, Samsung Advanced Institute of Technology|Jaehyun Park, Semiconductor R&D center, Samsung electronics|Minsu Seol, Samsung Advanced Institute of Technology|Jeehwan Kim, Massachusetts Institute of Technology, Samsung Advanced Institute of Technology|Kyung-Eun Byun, Samsung Advanced Institute of Technology

This work introduces the channel-last scheme for the first time to implement 2D channel multi bridge channel field effect transistor (MBCFET). We demonstrated 2D channel MBCFETs with a three-layer bridge structure on a 200mm wafer scale without transfer process. We implemented both NMOS and PMOS MBCFETs, and verify operation in 80% of the 720 devices fabricated. In the case of 2D channel MBCFETs utilizing the channel-first scheme, multi stack structure which has three-layer of 2D channel was fabricated based on direct growth method.

05:15 PM
24-7 | Scaling MoS2 transistors to 1 nm node, Weisheng Li, Nanjing University|Mingyi Du, Nanjing University|Chunsong Zhao, Huawei Technologies Co., LTD.|Guangkai Xiong, Nanjing University|Weizhuo Gan, Huawei Technologies Co., LTD.|Lei Liu, Nanjing University|Taotao Li, Nanjing University|Yuan Gao, Nanjing University|Fuchen Hou, Southern University of Science and Technology|Junhao Lin, Southern University of Science and Technology|Dongxu Fan, Nanjing University|Hao Qiu, Nanjing University|Zhihao Yu, Nanjing University of Posts and Telecommunications|Jeffrey Xu, Huawei Technologies Co., LTD.|Yi Shi, Nanjing University|Xinran Wang, Nanjing University

We report on the first monolayer MoS2 FETs scaledto 40 nm contacted gate pitch (CGP), corresponding to 1 nmnode as defined by IRDS.

05:40 PM
24-8 | Low-Power CMOS Inverter with Enhancement-mode Operation and Matched VTH at VDD = 1 V on Monolayer 2D Material Channel, Ang-Sheng Chou, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Ching-Hao Hsu, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan|Yu-Tung Lin, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan|Fa-Rong Hou, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan|Edward Chen, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Po-Sen Mao, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, Department of Electrophysics, National Yang Ming Chiao Tung University|Ming-Yang Li, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Sui-An Chou, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Dawei Heh, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Hsiang-Chi Hu, Department of Electrophysics National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Yu-Sung Chang, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan|Wen-Chia Wu, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Zih-Syuan Huang, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan|Yu-Wei Hsu, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan|Yuan-Chun Su, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, Department of Electrophysics, National Yang Ming Chiao Tung University|Terry Hung, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Po-Hsun Ho, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Tsung-En Lee, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Chen-Feng Hsu, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Goutham Arutchelvan, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Yun-Yan Chung,

Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Chao-Hsin Chien, Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Georgios Vellianitis, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Wei-Yen Woon, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Jin Cai, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Mark van Dal, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Wen-Hao Chang, Department of Electrophysics National Yang Ming Chiao Tung University, Hsinchu, Taiwan|Chih-I Wu, Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan|Chao-Ching Cheng, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan|Iuliana Radu, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan

Efficient digital circuits require CMOS transistors with well-matched threshold voltage (V_{TH}). In this work, we demonstrate for the first time CMOS co-integration, and well-matched V_{TH} showcased through inverters based two-dimensional (2D) materials with supply voltage (V_{DD}) of 1 V: voltage gain exceeding 10 V/V, noise margin over 80%, low average static-power consumption ~ 7 pW, and a switching voltage (V_M) ~ 0.5 V. While still far from Si performance, reaching these numbers simultaneously requires multiple step developments working well together for monolayer 2D materials in the co-integrated flow. Sensitivity of various electrical metrics to process steps is also discussed in the paper.

25 | PMA | High Voltage Wide Bandgap Power Devices
2:15 PM – 6:05 PM, Continental 6
Co-Chairs: Munetaka Noguchi, Mitsubishi Electric and Zhikai Tang, Texas Instruments

This session includes 8 papers that showcase the latest technology innovation in high-voltage wide bandgap power switching devices and integrated circuits. The first paper proposes a novel GaN-HEMT/SiC-JFET cascode device implementing vertical stack co-packaging with minimized parasitic inductance that results in extremely fast 800 V switching and strong dv/dt control. The session continues with the demonstration of a high-performance GaN-on-GaN vertical JFET with significantly reduced Crss by introducing the p-GaN shield structure. The third paper presents the first 10 kV GaN lateral power HEMT with p-GaN/2DEG based superjunction architecture. It is followed by description of ultra-wide bandgap AlN-based Schottky barrier diode with graded n+-AlGaN enabling low ohmic contact resistance for future power electronics applications. The fifth paper demonstrates the first 10 kV enhancement-mode lateral Ga2O3 JFET with NiO RESURF, operating up to 250°C. The sixth paper describes on a novel 150 mm single-crystal SiC engineered substrate, aiming at the reuse of dummy-grade material and recycling of prime-grade material for cost effectiveness. The seventh paper presents irradiation-hardened 800 V GaN device technology on the GaN-on-SiC power integration platform for aerospace applications. The final paper reports on GaN-on-Si JBS diodes based on an e-mode-compatible process, representing the potential for ultra-compact all-GaN power solutions.

02:15 PM
25-0 | Welcome

02:20 PM

25-1 | Stacked Strongly Coupled GaN/SiC Cascode Device with Fast Switching and Reclaimed Strong dv/dt Control, Ji Shu, The Hong Kong University of Science and Technology|Heng Wang, The Hong Kong University of Science and Technology|Mian Tao, The Hong Kong University of Science and Technology|Yat Hon Ng, The Hong Kong University of Science and Technology|Sirui Feng, The Hong Kong University of Science and Technology|Yangming Du, The Hong Kong University of Science and Technology|Zongjie Zhou, The Hong Kong University of Science and Technology|Jiahui Sun, The Hong Kong University of Science and Technology|Ricky Shi-Wei Lee, The Hong Kong University of Science and Technology|Kevin Jing Chen, The Hong Kong University of Science and Technology

We present a GaN-HEMT/SiC-JFET cascode device that replaces the most performance- and reliability-limiting MOS channel of SiC MOSFETs with a high-quality GaN 2DEG channel. Compared with SiC MOSFETs, the GaN/SiC cascode device delivers faster switching speed with substantially lower loss. A compact 3D co-packaging solution with stacked GaN and SiC chips results in greatly reduced parasitic interconnection inductance (L_P), With an ultra-low L_P, an increased capacitive gate-to-drain coupling in the low-voltage HEMT would allow strong d*v*/d*t* control via changing gate resistance R_G. The demonstrated GaN/SiC cascode device unveils an ultimate power device that unlocks the full potential of wide-bandgap semiconductors.

02:45 PM
25-2 | Low RonCrss Nomally-off Vertical GaN Transistor on GaN Substrate Using p-GaN Shield Structure for High-Power and High-Speed Switching, Naoki Torii, Panasonic Holdings Corporation|Daisuke Shibata, Panasonic Holdings Corporation|Masahiro Ogawa, Panasonic Holdings Corporation|Masao Kawaguchi, Panasonic Holdings Corporation|Hiroyuki Handa, Panasonic Holdings Corporation|Naohiro Tsurumi, Panasonic Holdings Corporation|Satoshi Tamura, Panasonic Holdings Corporation|Yoshio Okayama, Panasonic Holdings Corporation

A novel normally-off vertical GaN transistor on a GaN substrate using a p-GaN shield structure features a low RonCrss of 171 mΩ·pF. It achieves a maximum drain current of 57 A, breakdown voltage over 900 V, and fast switching at 350 V/10 A.

03:10 PM
25-3 | 10-kV E-mode GaN Lateral Superjunction Transistor, Junjie Yang, School of Integrated Circuits, Peking University, Beijing, China|Jingjing Yu, School of Integrated Circuits, Peking University, Beijing, China|Jiawei Cui, School of Integrated Circuits, Peking University, Beijing, China|Sihang Liu, School of Integrated Circuits, Peking University, Beijing, China|Hao Chang, School of Integrated Circuits, Peking University, Beijing, China|Yunhong Lao, School of Integrated Circuits, Peking University, Beijing, China|Han Yang, School of Physics, Peking University, Beijing, China|Teng Li, School of Integrated Circuits, Peking University, Beijing, China|Xuelin Yang, School of Physics, Peking University, Beijing, China|Jinyan Wang, School of Integrated Circuits, Peking University, Beijing, China|Xiaosen Liu, School of Integrated Circuits, Tsinghua University, Beijing, China.|Yan Wang, School of Integrated Circuits, Tsinghua University, Beijing, China.|Maojun Wang, School of Integrated Circuits, Peking University, Beijing, China|Bo Shen, School of Physics, Peking University, Beijing, China|Jin Wei, School of Integrated Circuits, Peking University, Beijing, China

This work presents an E-mode GaN lateral superjunction p-GaN gate HEMT (SJ-HEMT).The p-pillar is a thinned p-GaN layer, while the n-pillar is a 2DEG stripe between two adjacent p-pillars.Charge balance is

realized using alternative thinned p-GaN stripe and 2DEG stripe, contributing to improved *BV* and best-in-class FOM (= BV^2/R_{SP}). Thanks to the screening effect and the hole emission from p-pillars, a low dynamic R_{ON} is obtained for V_{DS} stress up to 6.5 kV. This work showcased the potential of GaN power HEMTs in kV-level applications.

04:00 PM
25-4 | Thermionic Field Emission in a Si-doped AlN SBD with a Graded n+-AlGaN Top Contact Layer, Takuya Maeda, The University of Tokyo|Yusuke Wakamoto, The University of Tokyo|Issei Sasaki, The University of Tokyo|Akihira Munakata, The University of Tokyo|Masanobu Hiroki, NTT Basic Research Lab.|Kazuyuki Hirama, NTT Basic Research Lab.|Kazuhide Kumakura, NTT Basic Research Lab.|Yoshitaka Taniyasu, NTT Basic Research Lab.

AlN SBDs with a graded n^+-AlGaN top contact layer, which enables low contact resistance without sacrificing AlN crystal quality, are demonstrated. The devices showed ideal thermionic field emission. The barrier height of 3.38 eV, which is consistent with the value from the *C-V* measurements, was obtained.

04:25 PM
25-5 | 10 kV, 250 oC Operational, Enhancement-Mode Ga2O3 JFET with Charge-Balance and Hybrid-Drain Designs, Yuan Qin, Virginia Polytechnic Institute and State University|Zineng Yang, Virginia Polytechnic Institute and State University|Hehe Gong, Virginia Polytechnic Institute and State University|Alan Jacobs, U.S. Naval Research Laboratory|Joseph Spencer, U.S. Naval Research Laboratory, Virginia Polytechnic Institute and State University|Matthew Porter, Virginia Polytechnic Institute and State University|Bixuan Wang, Virginia Polytechnic Institute and State University|Kohei Sasaki, Novel Crystal Technology|Chia-Hung Lin, Novel Crystal Technology|Marko Tadjer, U.S. Naval Research Laboratory|Yuhao Zhang, Virginia Polytechnic Institute and State University

We report the first 10 kV Enhancement-mode (E-mode) power transistor in ultra-wide bandgap (UWBG) materials. This lateral Ga_2O_3 JFET deploys a highly-doped p-type NiO for E-mode gate, as well as the lowly-doped NiO superjunction and hybrid-drain structures for electric field management. The device sets a new record of Baliga's FOM in all 3kV+ UWBG transistors. Moreover, the device maintains E-mode operation and >10 kV breakdown voltage at high temperatures up to 250 ^oC. This is the first report of 250 ^oC operation as well as HTRB and HTGB reliability data in all high-voltage transistors beyond SiC and Si.

04:50 PM
25-6 | Cost-Effective 1200 V SiC MOSFETs on a Novel 150 mm SiC Engineered Substrate with Dummy-Grade Material Reuse, Xinhua Wang, Institute of Microelectronics, CAS|Xiangjie Xing, Institute of Microelectronics, CAS|Xiaolei Yang, Nanjing Electronic Devices Institute|Xin Yang, Virginia Tech University|Yan Chen, Institute of Microelectronics, CAS|Guoliang Ma, Wuhan University|Bixuan Wang, Virginia Tech University|Zhifei Zhao, Nanjing Electronic Devices Institute|Chao Yuan, Wuhan University|Yun Bai, Institute of Microelectronics, CAS|Sen Huang, Institute of Microelectronics, CAS|Yipei Lei, Institute of Microelectronics, CAS|Jingyuan Shi, Institute of Microelectronics, CAS|Fuchao Liu, TJ Innovative Semiconductor Substrate Technology Co., Ltd.|Yuhao Zhang, Virginia Tech University|Fenwen Mu, TJ Innovative Semiconductor Substrate Technology Co., Ltd.|Xinyu Liu, Institute of Microelectronics, CAS|Sheng Liu, Wuhan University|Yue Hao, Xidian University

The SiC substrate cost accounts for >50% of final device cost. This work demonstrates a novel 150 mm single-crystal SiC engineered substrate allowing for 40% substrate cost reduction, which homogeneously integrates a prime-grade SiC layer onto a dummy-grade SiC substrate by surface-active bonding. The 150 mm SiC epi achieved a high killer-defect-free yield of 99.2%. The 1200 V, 20 mΩ SiC MOSFETs demonstrate a yield over 70%, as well as a performance and reliability comparable to the state-of-the-art commercial devices. Moreover, we report the wafer-level device data and high-current robustness for a SiC engineering substrate for the first time.

05:15 PM
25-7 | 800-V Irradiation-Hardened Device Technology on GaN-on-SiC Power Integration Platform,
Feng Zhou, Nanjing University|qi Wang, Harbin Institute of Technology, Nanjing University, Nanjing University, Harbin Institute of Technology|ming Liu, Harbin Institute of Technology|yang Xia, CorEnergy Semiconductor Company Ltd.|ke Wu, CorEnergy Semiconductor Company Ltd.|heng Li, CorEnergy Semiconductor Company Ltd.|gang Zhu, CorEnergy Semiconductor Company Ltd.|zong Xu, Nanjing University|fang Ren, Nanjing University|Dong Zhou, Nanjing University|jun Chen, Nanjing University|dou Zheng, Nanjing University|Rong Zhang, Nanjing University|dong Ye, Nanjing University| Hai Lu, Nanjing University
Speakers: Hehe Gong, Virginia Tech

This work reports the first demonstration of 800V irradiation-hardened (IH) GaN device technology on the GaN-on-SiC power integration platform. IH p-GaN HEMT, MIS HEMT and rectifier are achieved simultaneously, showing single-event burnout voltages above 800 V and SEB degradation rates of only 5~10%. These results are the best reported among Si/GaN/SiC devices to date. Meanwhile, nanosecond switching is revealed, achieving a high-power conversion efficiency of 96% under 500W/300K irradiation conditions. In the half-bridge circuit tests, the high-side and low-side IH devices are immune to crosstalk, revealing 600V/1MHz high-frequency switching. These results show the enormous potential of IH-GaN devices/circuits for irradiation applications.

05:40 PM
25-8 | 1200 V GaN-on-Si Junction Barrier Schottky (JBS) Diodes by An E-Mode-Compatibe Process,
Wensong Zou, Southern University of Science and Technology|Jiawei Chen, Southern University of Science and Technology, Shenzhen Pinghu Laboratory|David Zhou, Shenzhen Pinghu Laboratory|Jinshi Zhang, JT Microelectronics Co., Ltd.|Ran Chen, JT Microelectronics Co., Ltd.|Xiong Liu, JT Microelectronics Co., Ltd.|Mengyuan Hua, Southern University of Science and Technology|Jun Ma, Southern University of Science and Technology
Speakers: Luca Nela, NovaWave AG

In this work we demonstrate novel 1200 V GaN-on-Si junction barrier Schottky diodes using an e-mode-compatible process, presenting much improved reverse-blocking performance as well as excellent dynamic and switching characteristics, in addition to superior ESD robustness, high repetitive surge capability, and long lifetime revealed by accelerated HTRB tests.

Coffee break with Exhibitors
3:35 PM – 4:25 PM, Yosemite

Coffee break with Exhibitors

29 | Evening Panel – IEDM at 70: From Semiconductor to Era-Defining Computing Technology
8:00 PM – 10:00 PM, Continental 4 – 5

Before the IEDM meeting was in place, there was a lack of scalability of mechanical switches and vacuum tubes in rapidly growing telephony applications at the time that led to the need for a solid-state switch and the development of semiconductor transistor devices. The transistor is over 75 years old. The critical scaling of transistors has enabled integrated circuits with billions of interconnected transistors that are now fueling computing and their corresponding memory storage across various applications in the semiconductor industry. Moore's Law and Dennard's Scaling drove the era-defining computing that has spanned across a wide range of form factors and use cases from servers in the cloud, to desktops, and mobile devices at the edge. Today computing is at the core of AI applications with a diversity of computing processors and a range of computing power.

The demand for computing is on the rise with the continuing advancement of AI. The AI algorithms have become more complex requiring higher computing performance. As a result, computing power has increased on an unsustainable curve and uneconomical outcome. Should this trend continue, the golden age of AI will be short lived. Computing and its foundations are the chokepoint. The resulting path forward in the pursuit of energy-efficient computing requires a hard engineering focus and hence receives attention at IEDM and other IEEE conferences and technical communities.

How did we arrive at today's problem? What is the path forward? What are the approaches for our unquenchable appetite for computing? Bringing efficiency to an exponential challenge? All these questions and more will be discussed during the special 70th anniversary IEDM 2024 evening panel.

Organizer and Moderator: Ali Keshavarzi, Stanford University
Co-organizer: Ali Khakifirooz, Intel Corporation
Panelists: Tsu-Jae King Liu (UC Berkeley), Tom Lee (Stanford), Mark Lundstrom (Purdue), Mark Papermaster (AMD), Arijit Raychowdhury (Georgia Tech), Kevin Zhang (TSMC)

30 | MT | Ferroelectric FET and NAND Flash Memories
9:00 AM – 12:00 PM, Grand Ballroom A
Co-Chairs: Wanki Kim, Samsung and Maarten Rosmeulen, IMEC

This session includes 4 papers on the topic of NAND Flash and 2 papers about FeFET memories. The first paper proposes a 3D NAND Flash architecture with horizontal channel that provides superior scalability. The next 2 papers explore the use of ferroelectric layers for next generation 3D NAND memory. One

paper investigates the use of oxide semiconductor channels in ferroelectric VNAND. The last two papers present results on high-endurance FeFET memories.

09:00 AM
30-0 | Welcome

09:05 AM
30-1 | Superior Scalability of Advanced Horizontal Channel Flash For Future Generations of 3D Flash Memory, Minoru Oda, Kioxia Corporation|Kosuke Sakamawari, Kioxia Corporation|Shunichi Seno, Kioxia Corporation|Yuki Nakata, Kioxia Corporation|Ryo Fukuoka, Kioxia Corporation|Haruka Kusai, Kioxia Corporation|Keiji Hosotani, Kioxia Corporation|Toru Nakanishi, Kioxia Corporation|Daisuke Hagishima, Kioxia Corporation|Toshiya Ishikawa, Kioxia Corporation|Tatsuo Ogura, Kioxia Corporation|Shinya Naito, Kioxia Corporation|Takashi Kurusu, Kioxia Corporation|Sumiko Mano, Kioxia Corporation|Tsuyoshi Ogikubo, Kioxia Corporation|Motohiko Fujimatsu, Kioxia Corporation|Kikuko Sugimae, Kioxia Corporation|Mina Hatakeyama, Kioxia Corporation|Yuki Inuzuka, Kioxia Corporation|Yusuke Niki, Kioxia Corporation|Rieko Tanaka, Kioxia Corporation|Noboru Shibata, Kioxia Corporation|Hiroshi Nakamura, Kioxia Corporation|Makoto Fujiwara, Kioxia Corporation|Koji Matsuo, Kioxia Corporation|Yoshiro Shimojo, Kioxia Corporation|Fumitaka Arai, Kioxia Corporation|Masaki Kondo, Kioxia Corporation|Tomohiro Oki, Kioxia Corporation|Masaru Kito, Kioxia Corporation

We propose a novel architecture, advanced horizontal channel flash (HCF), that uses Local Block Interconnect, staggered Select Gates, and memory cells employing Floating Gate based charge storage. HCF with minimized 2F2 cell shows better cell efficiency than that of Vertical Gate NAND designs with 6F2 cell and of conventional 3D flash memory with 4F2 cell. Furthermore, HCF maintains the advantage of the VG-type devices, where cell current remains independent of the stacking number. The operation of the HCF device has been confirmed by TCAD simulation and a test vehicle fabricated using a 3D flash compatible process flow.

09:30 AM
30-2 | Gate-stack Optimization to Mitigate the Cylindrical Effect in Ferroelectric VNAND, Kwangsoo Kim, Samsung Electronics|Suhwan Lim, Samsung electronics|Jongho Woo, Samsung electronics|Junyeong Lim, Samsung electronics|Sijung Yoo, Samsung Advanced Institute of Technology|Hyoseok Kim, Samsung electronics|Jaewoo Park, Samsung electronics|Haeyeon Jun, Samsung electronics|Seunghyun Kim, Samsung electronics|Myunghun Woo, Samsung electronics|Taeyoung Kim, Samsung electronics|Sanghyun Park, Samsung electronics|Hanseung Ko, Samsung electronics|Youngji Noh, Samsung electronics|Moonkang Choi, Samsung electronics|Jongyeon Baek, Samsung electronics|Jisung Kim, Samsung electronics|Kiheun Lee, Samsung electronics|Sam Park, Samsung electronics|Dukhyun Choe, Samsung Advanced Institute of Technology|Moonyoung Jung, Samsung electronics|Gukhyon Yon, Samsung electronics|Suhyeong Lee, Samsung electronics|Hyung Joon Kim, Samsung electronics|Kijoon Kim, Samsung electronics|Sungduk Hong, Samsung electronics|Kwangmin Park, Samsung electronics|Bong Jin kuh, Samsung electronics|Wanki Kim, Samsung electronics|Daewon Ha, Samsung electronics|Sujin Ahn, Samsung electronics|Jaihyuk Song, Samsung electronics

For the first time, we demonstrate an in-depth analysis on a novel multi-layered gate-interfacial-layer (G.IL) and high-k channel-interfacial-layer (Ch.IL) in metal-insulator-ferroelectric-insulator-silicon (MIFIS) gate

stack FeFETs, using simulations and experimental validation. By exploring materials with varying energy barrier heights between the gate metal and G.IL to control the tunneling of charges from gate, we demonstrate an optimal gate stack incorporating a high-k Ch.IL. Our findings underline the benefits of this configuration, including a larger memory window (MW) and improved reliability characteristics (especially disturb and retention characteristics).

09:55 AM

30-3 | Clarifying the Role of Ferroelectric in Expanding the Memory Window of Ferroelectric FETs with Gate-Side Injection: Isolating Contributions from Polarization and Charge Trapping, Yixin Qin, University of Notre Dame|Saikat Chakraborty, University of Texas, Austin|Zijian Zhao, University of Notre Dame|Kijoon Kim, Samsung Electronics Co., Ltd|Suhwan Lim, Samsung Electronics Co., Ltd|Jongho Woo, Samsung Electronics Co., Ltd|Kwangsoo Kim, Samsung Electronics Co., Ltd|Wanki Kim, Samsung Electronics Co., Ltd|Daewon Ha, Samsung Electronics Co., Ltd|Xiao Gong, National University of Singapore|Asif Khan, Georgia Institute of Technology|Vijaykrishnan Narayanan, Pennsylvania State University|Jaydeep Kulkarni, University of Texas, Austin|Kai Ni, University of Notre Dame

In this work, we performed a comprehensive experimental and modeling study, clarifying the role of ferroelectric materials in boosting the memory window of FeFETs with gate-side charge injection for the first time. We separated the ferroelectric contributions to the memory window into remnant polarization and top charge trap layer (CTL) trapping.

10:45 AM

30-4 | Oxide Channel Ferroelectric NAND Device with Source- tied Covering Metal Structure: Wide Memory Window (14.3 V), Reliable Retention (> 10 years) and Disturbance Immunity (△Vth ≤ 0.1 V) for QLC Operation, Hongrae Joh, KAIST|Giuk Kim, KAIST|Jihye Ock, KAIST|Seungyeob Kim, KAIST|Sangmok Lee, KAIST|Sangho Lee, KAIST|Kwangsoo Kim, Samsung Electronics|Suhwan Lim, Samsung Electronics|Jongho Woo, Samsung Electronics|Wanki Kim, Samsung Electronics|Daewon Ha, Samsung Electronics|Jinho Ahn, Hanyang University|Sanghun Jeon, KAIST

We show oxide-channel gate-injection type ferroelectric NAND device, featuring source-tied covering metal, control dielectric and Si_3N_4 charge-trap-layer. Proposed device exhibits wide memory window (14.3V), superior retention (~10 years) and disturbance immunity (ΔV_{th}< 0.1 V after 10^5 disturb cycles). We also propose 3D vertical NAND (VNAND) integration strategy without any density loss.

11:10 AM

30-5 | Novel Design Strategy for High-Endurance (>1010) and Fast-Erase Oxide-Semiconductor Channel FeFET, Zhuo Chen, IMEC, KU Leuven|Hyun-Cheol Kim, IMEC, KU Leuven|Wei Zheng, IMEC|Roman Izmailov, IMEC, KU Leuven|Brecht Truijen, IMEC|Subhali Subhechha, IMEC|Amey Walke, IMEC|Adrian Chasin, IMEC|Mihaela Popovici, IMEC|Jie Li, IMEC|Anastasiia Kruv, IMEC|Hongwei Tang, IMEC, KU Leuven|Fengben Xi, IMEC|Geert Van den bosch, IMEC|Maarten Rosmeulen, IMEC|Nicolò Ronchi, IMEC|Valeri Afanas'ev, IMEC, KU Leuven|Jan Van Houdt, IMEC, KU Leuven

We fabricate ALD Oxide-Semiconductor Channel (OSC) FeFETs on 300-mm wafers. New design strategies of OSC FeFETs by La:HZO/IGZO interfacial engineering and IGZO channel thickness/length scaling are implemented. In-poor IGZO improves the Memory Window (MW) and V_t stability. High MW and state-of-art endurance (>10^{10} cycles) are demonstrated in novel dual-composition-channel FeFETs.

11:35 AM
30-6 | Demonstration of Ferroelectric FET Memory with Oxide Semiconductor Channel to Achieve Smallest Cell Area 0.009 μm2 and High Endurance for Non-Volatile High-Bandwidth Memory Applications, Yu-Ming Lin, R&D, Taiwan Semiconductor Manufacturing Company|Chun-Chieh Lu, R&D, Taiwan Semiconductor Manufacturing Company|Yu-Chuan Shih, R&D, Taiwan Semiconductor Manufacturing Company|Chih-Yu Chang, R&D, Taiwan Semiconductor Manufacturing Company|Yu-Kai Chang, R&D, Taiwan Semiconductor Manufacturing Company|Yu-Chien Chiu, R&D, Taiwan Semiconductor Manufacturing Company|Wen-Ling Lu, R&D, Taiwan Semiconductor Manufacturing Company|Chih-Hung Nien, R&D, Taiwan Semiconductor Manufacturing Company|Yu-Ming Hsiang, R&D, Taiwan Semiconductor Manufacturing Company|Ya-Yun Cheng, R&D, Taiwan Semiconductor Manufacturing Company|Yi-Ching Liu, R&D, Taiwan Semiconductor Manufacturing Company|Huai-Ying Huang, R&D, Taiwan Semiconductor Manufacturing Company|Pei-Jean Liao, R&D, Taiwan Semiconductor Manufacturing Company|Vincent Duen-Huei Hou, R&D, Taiwan Semiconductor Manufacturing Company|Gerben Doornbos, R&D, Taiwan Semiconductor Manufacturing Company|Georgios Vellianitis, R&D, Taiwan Semiconductor Manufacturing Company|Mark van Dal, R&D, Taiwan Semiconductor Manufacturing Company|Jeff Wu, R&D, Taiwan Semiconductor Manufacturing Company

We demonstrated a smallest cell area of 0.009 μm^2 in FeFET memory with oxide semiconductor fabricated on 300-mm wafer, and achieved high read current of 40 μA/μm, program speed below 30 ns, 1000 s retention at 85 °C, and 10^{12}high endurance cycles. Asymmetric dipole switching issue in n-type OS can be mitigated by HfZrO phase engineering to attain highly reproducible switching behaviors with reduced operation voltage.The device endurance is improved by interface layer and bulk engineering to minimize the oxygen vacancy generation / migration. This work paves way to realize BEOL-compatible memory with high density and low-power consumption.

35 | SMB | Biosensors and wearables
9:00 AM – 12:00 PM, Continental 6
Co-Chairs: Man Wong, Hong Kong University of Science and Technology and Cunjiang Yu, UIUC

The 6 talks in this session cover a range of biosensing and wearables systems. These include a highly sensitive dual-gate bioFET sensor array for DNA detection by Y. Li et al.; An implantable flexible active-matrix electrode array for surface brain electrophysiology mapping by Y. Xie et al.; Large-area bio-chip for bacterial DNA detection by W. Tang et al.; an invited talk on MEMS wideband seismometer and stain gauges for wearable cardiopulmonary applications by Ayazi et al.; a dual-gate TFT coupled piezoelectric wearable pulse sensor by Lin et al.; a high-density flexible tactile sensor array for robotics applications by Tang et al.

09:00 AM
35-0 | Welcome

09:05 AM
35-1 | Dual-gate IGZO FET Sensor Array for Multi-biomarker Detection Achieving Ultra High Sensitivity with 4.426%/decade of ssDNA and 1102nA/decade of Protein CA125, Yao Li, Institute of Microelectronics, Chinese Academy of Sciences, University of the Chinese Academy of Sciences|yuying zhou, Institute of Microelectronics, Chinese Academy of Sciences, University of the Chinese Academy of

Sciences|Bing Chen, Department of Gastroenterology, The First Affiliated Hospital of Zhengzhou University|Shuaidi Zhang, Institute of Microelectronics, Chinese Academy of Sciences|Ke Hu, Institute of Microelectronics, Chinese Academy of Sciences, University of the Chinese Academy of Sciences|Peiyun Li, Institute of Microelectronics, Chinese Academy of Sciences, University of the Chinese Academy of Sciences|Congyan Lu, Institute of Microelectronics, Chinese Academy of Sciences|Wenchang Zhang, Institute of Microelectronics, Chinese Academy of Sciences|Xiaonan Yang, School of Information Engineering, Zhengzhou University|Feng Zhang, Institute of Microelectronics, Chinese Academy of Sciences|Jiawei Wang, Institute of Microelectronics, Chinese Academy of Sciences|Ling Li, Institute of Microelectronics, Chinese Academy of Sciences

This work proposes a dual-gate IGZO-bioFET sensor array that is able to simultaneously detect cross-scale biomarkers without initial offset variation and exhibiting excellent performance, including high sensitivity (ssDNA - 4.426%/decade, CA125 protein - 1102 nA/decade), extremely low detect-of-limit (ssDNA - 1.67 aM, CA125 protein - 0.1 fg/mL), low operation voltage (0.1 V) and low initial offset variation (~ 2 nA).

09:30 AM
35-2 | An Implantable, 1024-Channel Multiplexed Electrode Array for High-Density Brain Activity Mapping, Xing Sheng, Tsinghua University|Yang Xie, Tsinghua University

Brain-machine interface (BMI) devices with flexibility, high-density and high-throughput capabilities emerge as pivotal developmental trends in recent years. Conventional neural electrodes are constrained by the fan-out density. Here we present a flexible and implantable electrocorticography (ECoG) device array based on metal-oxide semiconductor thin-film transistors (TFTs), to record brain activities at a large scale. Employing a multiplexing technique, the system is capable to record ECoG signals with up to 1024 channels and a density of 44 sites/mm^2, while compressing the driving leads to around 64. In an epileptic animal model, the device exhibits outstanding spatial resolution to record extensive brain areas.

09:55 AM
35-3 | Large-area 64×64 Ion-Sensitive Thin-Film Transistor Bio-chip for Real-time Detection of Multiple Pathogenic Bacteria DNAs, Wei Tang, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Jun Li, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Haiyang Yu, Shanghai Veterinary Research Institute, Chinese Academy of Agricultural Sciences, Shanghai, China|Fucheng Wang, Shanghai Veterinary Research Institute, Chinese Academy of Agricultural Sciences, Shanghai, China|Zhonghao Shi, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Yu Huang, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Ziheng Wang, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Mengwei Si, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China|Wei Jiang, Shanghai Veterinary Research Institute, Chinese Academy of Agricultural Sciences, Shanghai, China|Xiaojun Guo, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China

This work presents a large-area (32 mm × 32 mm) bio-sensor chip consisting of 64×64 ion-sensitive thin-film transistor (ISTFT) pixels. The chip is fabricated based on the industry standard low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) backplane processes from the semiconductor fab. Full-area dynamic mapping of proton dynamics in solution with high sensitivity and high spatiotemporal

resolution is demonstrated. Furthermore, the bio-chip is integrated with a customized microfluidic channel to realize real-time label-free detection of multiple DNA biomarkers, enabling parallel screening of pathogenic bacteria.

10:45 AM
35-4 | Advanced MEMS-Based Wearable Devices for Cardiopulmonary Applications (Invited), Farrokh Ayazi, Georgia Tech, StethX Microsystems|Xinyu Jiang, Georgia Tech|Brian Sang, Georgia Tech

Advances in MEMS sensors have enabled a number of new wearable medical applications at low cost and high fidelity.This paper presents the latest results from MEMS wideband seismometers and strain gauges in wearable medical applications.While wafer-level packaging of the sensors enables high reliability and repeatability for these devices, their small size, high performance, and robustness make them ideal for use in emerging areas.We discuss applications of these devices in precision seismocardiography (SCG), mechanomyography (MMG), lung sound detection, and strain plethysmography (SPG) in the wearable cardiopulmonary space.

11:10 AM
35-5 | High Performance 3D ITZO DGTFTs and Their Application in Wearable Pulse Sensors, Delang Lin, School of Microelectronics, South China University of Technology|Rongsheng Chen, School of Microelectronics, South China University of Technology, State Key Laboratory of Advanced Displays and Optoelectronics Technologies, Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology|Man Chun Tseng, State Key Laboratory of Advanced Displays and Optoelectronics Technologies, Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology|Fion Sze Yan Yeung, State Key Laboratory of Advanced Displays and Optoelectronics Technologies, Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology|Hoi Sing Kwok, State Key Laboratory of Advanced Displays and Optoelectronics Technologies, Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology

The 3D ITZO DGTFTs with OTES barrier layer were successfully prepared. The resulting DGTFTs exhibit excellent transistor characteristics and reliability. Moreover, the prepared DGTFTs have high top-gate coupling coefficients, making them promising for high-sensitivity wearable applications, as evidenced by the realization of a wearable impulse sensor that accurately identifies characteristic peaks of weak pulse waves.

11:35 AM
35-6 | Flexible Active-Matrix Tactile Sensor Arrays with High Density of 4096 pixels/cm2 and In-Array Sensitivity of 51 kPa-1, Bowen Zhu, Westlake University|Yingjie Tang, Westlake University|Lang Wang, Westlake University|Siyu Zhang, Westlake University|Hui Zhang, Westlake University|Yan Wang, Westlake University|Yitong Chen, Westlake University|Fanfan Li, Westlake University|Dingwei Li, Westlake University|Huihui Ren, Westlake University|Guolei Liu, Westlake University|Qi Huang, Westlake University|Hua Xu, Guangzhou New Vision Optoelectronic Technology Co., Ltd.|Liaoyong Wen, Westlake University

In this work, we demonstrate a flexible active-matrix (AM) tactile sensor array (TSA) with both high pixel density and sensitivity, by monolithically integrating a 64 × 64 lanthanum-doped indium zinc oxide (Ln-

IZO) thin-film transistor (TFT) array (4096 pixels, 1 × 1 cm^2) with a hierarchically micro-/nanostructured high pressure-sensitive film. The flexible AM-TSA exhibits a high spatial resolution of 150 μm, high in-array tactile sensitivity of 51 kPa^{-1}, fast response/recovery time (51/32 ms), a low detection limit of 2.5 Pa, and robust mechanical stability, feasible for applications in tactile robotics.

36 | EDT | BEOL-compatible Oxide Channel Devices
9:00 AM – 12:00 PM, Continental 7 – 9
Co-Chairs: Veeresh Deshpande, IIT Bombay and Tania Roy, Duke University

This session features six papers on recent advancements in BEOL-compatible monolithic 3D integration with oxide channels. The first paper highlights the enhancement of Vt stability through capping techniques. The second paper presents an ideal subthreshold swing of 60 mV/dec at room temperature, achieved through interface optimization. Two subsequent papers focus on oxide channels with ferroelectric gate oxide, including a demonstration of a refresh-free, high-endurance 1T-1FeFET cell. The fourth paper delves into scaled transistors, showcasing discrete ferroelectric domain switching. The next paper demonstrates high Cmax/Cmin ratios in memcapacitive synapses using ferroelectric dielectrics. The final paper discusses the monolithic 3D integration of a vertically stacked memory array, featuring IGZO FETs and MoS2 analog RRAMs for low voltage switching.

09:00 AM
36-0 | Welcome

09:05 AM
36-1 | Enhancement-mode Atomic Layer Deposited W-doped In2O3 Transistor at 55 nm Channel Length by Oxide Capping Layer with Improved Stability, Qing Lin, TSMC|Nathaniel Safron, TSMC|Donglai Zhong, TSMC|Goutham Arutchelvan, TSMC|Carlo Gilardi, TSMC|Chanyoung Yoo, Stanford University|Jonathan Hartanto, Stanford University|Balreen Saini, Stanford University|Sheng-Chih Lai, TSMC|Gregory Pitner, TSMC|Gary Chen, TSMC|Marvin Chang, TSMC|Yu-ming Lin, TSMC|Wilman Tsai, Stanford University|Paul McIntyre, Stanford University|Iuliana Radu, TSMC

Oxide capping and post-capping anneal are used on back-gated W-doped In_2O_3 transistors, demonstrating enhancement mode at 55 nm L_{CH}. This approach achieves positive V_{TH} shift, lower contact resistance, higher mobility, and improved positive-bias-stress stability simultaneously, thereby enabling 1.42× increase in I_{ON} and breaking the traditional performance, V_{TH}, and stability trade-off.

09:30 AM
36-2 | First Demonstration of Double-Gate IGZO Transistors with Ideal Subthreshold Swing of 60 mV/dec at Room Temperature and 76 mV/dec at 380 K over 5 Decades and gm Exceeding 1 mS/μm with Contact Length Scaling, Wenjie Zhao, Peking University, Huazhong University of Science and Technology|Shenwu Zhu, Peking University, Huazhong University of Science and Technology|Qijun Li, Huazhong University of Science and Technology|Qianlan Hu, Peking University|Honggang Liu, Huazhong University of Science and Technology|Anyu Tong, Peking University|Min Zeng, Huazhong University of Science and Technology|Ru Huang, Peking University|Yanqing Wu, Peking University

In this work, contacted length scaling for atomic-layer-deposited IGZO transistors has been systematically investigated. The 70 nm dual-gate IGZO transistor has demonstrated an ideal subthreshold swing of 60

mV/dec at room temperature and 76 mV/dec at elevated temperature of 380 K over 5 decades for the first time. Furthermore, the shorter 35 nm dual-gate transistor with contact length of 80 nm has achieved a record-high transconductance exceeding 1 mS/μm. When the contact length is further reduced to 40 nm, the transconductance remains above 0.75 mS/μm and the on-state current exceeds 1.33 mA/μm for the 35 nm channel length transistor, respectively.

09:55 AM
36-3 | Amorphous Indium Oxide Channel FeFETs with Write Voltage of 0.9V and Endurance >10^12 for Refresh-free 1T-1FeFET embedded Memory, Sharadindu Gopal Kirtania, Georgia Institute of Technology|Omkar Phadke, Georgia Institute of Technology|Eknath Sarker, Georgia Institute of Technology|Khandker Akif Aabrar, Georgia Institute of Technology|Dyutimoy Chakraborty, Georgia Institute of Technology|Faaiq Waqar, Georgia Institute of Technology|Shin Jaewon, Georgia Institute of Technology|Tanvir Pantha, University of Texas Dallas|Sourav Datta, University of Texas Dallas|Asif Khan, Georgia Institute of Technology|Shimeng Yu, Georgia Institute of Technology|Suman Datta, Georgia Institute of Technology

For the first time, we demonstrate a back end of the line (BEOL) compatible amorphous oxide semiconductor (AOS) FeFET with a record-low operating voltage <0.9V and write-speed of 20ns while maintaining a current window (ILVT/IHVT) >103. We also demonstrate a) bipolar write endurance reaching 1012 cycles (measured), b) fast read speed of 50 ns, c) read endurance greater than 1012 cycles, and d) retention time exceeding 104 seconds at 85℃.

10:20 AM
36-4 | Highly-Scaled BEOL E-mode Transistor and Discrete-Domain Ferroelectric Memory Platform Enabled by PEALD In2O3, Yanjie Shao, Massachusetts Institute of Technology|John Huang, Massachusetts Institute of Technology|Elham Rafie Borujeny, Massachusetts Institute of Technology|Tyra Espedal, Massachusetts Institute of Technology|Dimitri Antoniadis, Massachusetts Institute of Technology|Jesús del Alamo, Massachusetts Institute of Technology

This work demonstrates a promising BEOL platform for active-area-scaled E-mode FETs and ferroelectric memory devices based on PEALD In_2O_3. Channel width scaling emerges as a crucial approach for high-performance E-mode FETs, as well as for single/few ferroelectricdomain switching that opens new opportunities for dense, fast, and low-voltage ferroelectricmemory.

11:10 AM
36-5 | BEOL-compatible Non-Volatile Capacitive Synapse with ALD W-doped In2O3 Semiconductor Layer, Junmo Lee, Georgia Institute of Technology|Chengyang Zhang, Georgia Institute of Technology|Minji Shon, Georgia Institute of Technology|James Read, Georgia Institute of Technology|Sunbin Deng, Georgia Institute of Technology|Omkar Phadke, Georgia Institute of Technology|Prasanna Venkatesan Ravindran, Georgia Institute of Technology|Mengkun Tian, Georgia Institute of Technology|Yuan-Chun Luo, Georgia Institute of Technology|Tae-Hyeon Kim, Georgia Institute of Technology|Asif Khan, Georgia Institute of Technology|Suman Datta, Georgia Institute of Technology|Shimeng Yu, Georgia Institute of Technology

We experimentally demonstrate BEOL-compatible metal-ferroelectric-semiconductor-type non-volatile capacitive synapse with ALD-grown W-doped In_2O_3 as the semiconductor layer. For the first time, ALD

with *in-situ* W doping technique is utilized for the In_2O_3layer. Record high capacitance on/off ratio (~23) among BEOL capacitive synapses is achieved in this work. Overlap area and W-doping control techniques are proposed to enhance capacitance on-off ratio, and design guidelines to optimize on-off ratio are established. Moreover, write endurance of >1E7 is achieved. Array-level benchmark of the compute-in-memory hardware based on the fabricated device suggests 24.4x figure-of-merit (=TOPS/WxTOPS/mm^2) performance improvement over state-of-the-art resistive synapse counter part.

11:35 AM
36-6 | 1T1R and 2T0C1R IGZO-MoS2 All-BEOL 3D Memory Cells, Baoshan Tang, National University of Singapore|Zihang Fang, National University of Singapore|Ruyue Wan, National University of Singapore|Sonu Hooda, National University of Singapore|JINFENG LEONG, National University of Singapore|Quanzhen Wan, National University of Singapore|Chun-Kuei Chen, National University of Singapore|Evgeny Zamburg, National University of Singapore|Joong-sik Kim, National University of Singapore|Aaron Thean, National University of Singapore

We investigated the monolithic 3D integration of vertically stacked 1T1R and 2T0C1R DRAM-RRAM hybrid memory array with IGZO FETs and MoS_2 analog RRAMs for low voltage switching. Furthermore, to address RRAMs endurance limitations, we propose an ultra-compact vertically stacked 2T0C1R gain cell DRAM-RRAM hybrid using dual-gated IGZO FET. We also propose an all-IGZO buffer capable of 3D BEOL data pipelining for concurrent multi-stacked array operations.

32 | MS | Modeling of Advanced Channel Materials: 2D, IGZO, and GaN
9:00 AM – 12:25 PM, Continental 1 – 3
Co-Chairs: Benoît Sklénard, CEA-Leti and Devin Verreck, IMEC

This session includes 7 papers on the modeling of advanced channel materials. The first 4 papers study 2D materials. The first paper is an invited paper by Luisier of ETH Zurich which discusses a simulation framework that combines ab-initio, molecular dynamics, kinetic Monte Carlo and quantum transport. The second paper by Xu from the University of California Santa Barbera, models electrothermal effects in 3D transistors with 2D material channels, using a multiscale approach. The third paper by Ansari from Tyndall National Institute, reports on the modeling of transport across grain boundaries in 2D transition metal dichalcogenides. The fourth paper by Nguyen from the University of Udine, proposes a design study of a steep slope Dirac-source FET based on hydrogenated graphene. The next two papers study devices with In-Ga-Zn-O (IGZO) channels using DFT and NEGF quantum transport. The fifth paper of the session by Seo from Korea Advanced Institute of Science and Technology investigates the impact of cation disorder, dimensions and composition on carrier mobility. The sixth paper by Zhao from IMECAS studies the problem of TiN/IGZO contact resistance in channel-all-around FETs. The final paper of the session by Hassan Palash from the Bangladesh University of Engineering and Technology reports a TCAD analysis of GaN-based optically triggered HEMT and FinFET.

09:00 AM
32-0 | Welcome

09:05 AM
32-1 | Nanoscale Device Modeling beyond the Ballistic Limit of Transport and Fixed Geometries (Invited), Mathieu Luisier, ETH Zurich|Jonathan Backman, ETH Zurich|Jiang Cao, ETH Zurich|Leonard

Deuschle, ETH Zurich|Manasa Kaniselvan, ETH Zurich|Youseung Lee, ETH Zurich|Alexander Maeder, ETH Zurich|Vincent Maillou, ETH Zurich|Marko Mladenovic, ETH Zurich|Nicolas Vetsch, ETH Zurich|Anders Winka, ETH Zurich|Xia Chen Hao, ETH Zurich|Alexandros Ziogas, ETH Zurich

To design the multi-functional, multi-materials nano-devices equipping today's electronic products, a dedicated simulation environment that fulfills very specific requirements is needed. In this paper, we present such a framework that relies on density functional theory, molecular dynamics, kinetic Monte Carlo, and quantum transport. We then demonstrate its key features (inclusion of scattering and treatment of evolving geometry) using four representative device examples.

09:30 AM

32-2 | Analysis and Implication of Electrothermal Effects in Emerging 3D Transistors and Integration Topologies with Two-dimensional Semiconductors, Lin Xu, ECE Department, University of California, Santa Barbara, CA|Ankit Kumar, ECE Department, University of California, Santa Barbara, CA|Emmanuel Quezada, ECE Department, University of California, Santa Barbara, CA|Jianfeng Jiang, EECS, Massachusetts Institute of Technology, Cambridge, MA|Guenhyung Oh, ECE Department, University of California, Santa Barbara, CA|Kunjesh Agashiwala, ECE Department, University of California, Santa Barbara, CA|Junkai Jiang, ECE Department, University of California, Santa Barbara, CA|Arnab Pal, ECE Department, University of California, Santa Barbara, CA|Wei Cao, ECE Department, University of California, Santa Barbara, CA|Minseong Lee, ECE Department, University of California, Santa Barbara, CA, SAMSUNG Electronics Co. Ltd., Suwon-City, South Korea|Kaustav Banerjee, ECE Department, University of California, Santa Barbara, CA

Thisworkpresents the first comprehensiveelectrothermal modeling andanalysis oftwo-dimensional semiconductor (2DS) based emerging 3D transistor architectures including nanosheet field-effect transistors(NSFETs) and complementary FETs (CFETs).Using a multi-scale (from materials and interfaces to devices) simulation framework that accurately accounts for the enhanced thermal boundary resistance between 2D layered semiconductors and adjacent materials, our methodology establishes a foundational platform for analyzing the self-heating effect (SHE) and offers comprehensive design guidelines for optimizing the electrothermal and reliability performance of emerging 3D FETs and 3D integration topologies in advanced technology nodes.

09:55 AM

32-3 | Correlation of TMD Defects with Device Performance in Ultra-Scaled Channels: Theoretical Insights and Experimental Observations, Lida Ansari, Tyndall National Institute, University College Cork|Andrey Vyatskikh, Intel Foundry Technology Research|Chelsey Dorow, Intel Foundry Technology Research|Saurabh Kharwar, Tyndall National Institute, University College Cork|Sharieh Jamalzadeh, Tyndall National Institute, University College Cork|Pau Hurley, Tyndall National Institute, University College Cork|Luca Camilli, Tor Vergata University of Rome|Manuela Scarselli, Tor Vergata University of Rome|Matthew Shaw, Intel Foundry Technology Research|Lutfe Siddiqui, TCAD, Intel|Ashish Penumatcha, Intel Foundry Technology Research|Kevin O'Brien, Intel Foundry Technology Research|Carly Rogan, Intel Foundry Technology Research|Scott Clendenning, Intel Foundry Technology Research|Jessica Torres, Intel Foundry Technology Research|Uygar Avci, Intel Foundry Technology Research|Farzan Gity, Tyndall National Institute, University College Cork

We present a comprehensive analysis of the effects of two prevalent types of grain boundaries (GBs), namely 4|4E and 4|4P, as well as vacancies. While it is clear that TMD defects pose a serious concern for device variability, our results show the impact of GBs on device performance actually depends on many factors: i) GB type, ii) device polarity, iii) position of GB, and iv) channel length. Lastly, we correlate linear channel defects to device performance through ALD decoration of linear defects in large-area grown ML MoS_2 devices, which consistently aligns with our theoretical predictions.

10:20 AM
32-4 | Sub-60mV/dec Swing and Drive Current in Dirac-Source FETs: a Design Study based on First-Principle Transport Simulations, Duy Nguyen, DPIA, University of Udine, Université Paris-Saclay, CNRS, C2N|Alessandro Pilotto, DPIA, University of Udine|Daniel Lizzit, DPIA, University of Udine|Marco Pala, DPIA, University of Udine|David Esseni, DPIA, University of Udine

A modelling framework consisting of NEGF-based ab-initio simulations is used to investigate Dirac-Source FETs (DSFETs). First, pivotal methodological aspects to obtain sub-60mV/dec swing in simulations are discussed. Then, a novel HGr-DSFET that outperforms the graphene-MoS_2 DSFET in terms of drive current is proposed. Rethermalization due to phonons is also discussed.

11:10 AM
32-5 | Transport Properties of Crystalline IGZO Channel Devices: Effects of Cation Disorders, Composition and Dimensions, Deokhwa Seo, Korea Advanced Institute of Science and Technology|Seunghyo Han, Korea Advanced Institute of Science and Technology|Jun-Hwe Cha, SK hynix Inc.|Seiyon Kim, SK hynix Inc.|Mincheol Shin, Korea Advanced Institute of Science and Technology

In this work, we present a comprehensive investigation of the transport properties of crystalline IGZO channel devices. We calculate the bulk mobility employing first-principles method, which shows remarkable agreement with the experimental results. Building on this success, we develop an effective model which faithfully reproduces the atomistic calculation results. We then calculate the mobility across various regions of the IGZO composition space, and explore the impact of changing dimensions from bulk to thin-body to nanowires. Finally, the current-voltage characteristics of nanowire transistors with IGZO channels are computed incorporating cation disorder scattering mechanism, which reveals disorder-induced threshold voltage variations.

11:35 AM
32-6 | Deep Insights into Interlayer in TiN/IGZO Contact and Its Impact on Contact Resistance of CAA FETs: First-Principles Calculation, Experimental Study and Modeling, Yue Zhao, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Lijun Xu, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Chuanke Chen, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Chunyu Zhang, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Ziheng Bai, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Lihua Xu, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Xufan Li, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Kexin Shang, Key Lab of Fabrication

Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Kun Luo, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Jiangtao Liu, Guizhou Minzu University, Guiyang, China|Qinzhi Xu, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Zhenhua Wu, Zhejiang University, Hangzhou, China|Lingfei Wang, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Ling Li, Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China|Ling Liu, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China

Contact engineering is increasingly important inIndium-Gallium-Zine-oxide based M3D-DRAM and limits theperformance metric, integration density and thermal budget. Inthis work, we systematically analyze the formation mechanismof interfacial oxide layer in CMOS-compatible titanium nitrideTiN/IGZO contacts and its effect on contact resistance (RC) inChannel-All-Around (CAA) FETs. Based on the first-principalcalculation, the dimension and composition of TiNxOy, as wellas interfacial property of IGZO, are key in non-ideal contactsand random fluctuations. Effects of oxide layer thickness andvacancy are studied, providing theoretical fundamentals forcontact engineering. Moreover, experiments are conducted toexplore the impact of different binary oxide (e.g., InO, GaO,AlO, etc.) contact interlayers. Correspondingly, a Y-functionmethod is firstly proposed to extract gate voltage-dependent RCin CAA-FETs. According to a modified transfer-line model, Rccompact model is developed, incorporating mechanisms ofSchottky emission and oxide-layer tunneling. It is calibrated tothe experiments and embedded into a core compact model,enabling accurate 2T0C DRAM simulation, and providing theguideline for fabrication.

12:00 PM
32-7 | Performance Optimization of GaN based Optically Triggered Transistors, Rafid Hassan Palash, Dept. of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka-1205, Bangladesh|Toiyob Hossain, Dept. of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka-1205, Bangladesh|Bejoy Sikder, Dept. of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka-1205, Bangladesh|Qingyun Xie, Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A. |Victor Moroz, Synopsys, Inc., Mountain View, CA, U.S.A.|Tomás Palacios, Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A. |Nadim Chowdhury, Dept. of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka-1205, Bangladesh

31 | ALT | 3D-integrated Circuit Technology
9:00 AM – 12:50 PM, Grand Ballroom B
Co-Chairs: Bich-Yen Nguyen, SOITEC and Liesbeth Witters, IMEC

This session presents eight papers on the latest advancements in 3D Integrated Circuit (3DIC) technology, covering fabrication, system-technology co-optimization, and electrical and thermal characterization. Key topics include backside power delivery networks for sub-2nm nodes, active power delivery in 3D-stacked systems with GaN devices, and a new approach to evaluating PPA benefits for 3D-stacked Network on Chip. The session also highlights innovations in 3D heterogeneous integration, such as multilayer RDL

stacking, low-temperature bonding techniques, and selective layer transfer for efficient bonding of ultra-thin chiplets. The final two papers explore integrated photonics, featuring a large-scale Digital Optical Computing System for AI training and a full integration technology for Broadband Optical Engine applications with enhanced PPA and bandwidth.

09:00 AM
31-0 | Welcome

09:05 AM
31-1 | Power and Thermal Integrity Analysis of High Performance and Low Power CPUs at Sub-2nm Node Designed with Various Advanced Backside PDNs, Linqiu Wang, Peking University|Feifan Xie, Purdue, Peking University|Jizhe Liu, Peking University|Tianchi Liu, Peking University|Lianmao Peng, Peking University|Zhiyong Zhang, Peking University|Tiwei Wei, Purdue University|Rongmei Chen, Peking University

In this work, we comprehensively evaluated power and thermal integrity of a high performance (HP) CPU and a low power (LP) or high density (HD) CPU in a sub-2nm technology node. Five power delivery networks (PDNs), including conventional front-side PDN, BPR-nTSV,an improved BPR-slit-nTSV, Power-via (PV), and direct backside contact (BSC) BSPDNs, were applied to the HP and HD CPUs, covering all the proposed most advanced backside PDN generic structures up to now.

09:30 AM
31-2 | Vertically Integrated Active Power Delivery Network (PDN) for Heterogenous 3D (H3D) Stacked Systems: 3D On-chip Integration of GaN Power Devices on PDN with Direct Heat Spreading Layer Bonding, Jaeyong Jeong, KAIST|Chan Jik Lee, KAIST|Sung Joon Choi, KAIST|Nahyun Rheem, KAIST|Minseo Song, KAIST|Yoon-Je Suh, KAIST|Bong Ho Kim, KAIST|Joon Pyo Kim, KAIST|Joonsup Shim, KAIST|Jiseon Lee, KANC|Myungsoo Park, KANC|Yumin Koh, KANC|Donghyun Kim, KANC|Sanghyeon Kim, KAIST

We demonstrate heterogeneous 3D integration of GaN power devices on CMOS PDN with direct heat spreading layer bonding for vertically integrated active PDN. Our GaN device, with LG of 1.5 μm and LGD of 15 μm, achieves Ron of 22.3 Ω·mm and VBD of 137 V, surpassing Si limits. Using thermoreflectance microscopy, we show that direct heat spreading significantly reduces thermal effects, improving thermal resistance (RTH) by 48.8% compared to conventional GaN devices.

09:55 AM
31-3 | System technology co-optimization of cost-bandwidth tradeoffs in Network on Chip through 3D integration and backside signals, Moritz Brunion, imec|Arvind Sharma, imec|Gioele Mirabelli, imec|Dawit Abdi, imec|Yun Zhou, imec|Halil Kükner, imec|Odysseas Zografos, imec|Fernando Redondo, imec UK|Dwaipayan Biswas, imec|Geert Hellings, imec|Julien Ryckaert, imec|James Myers, imec UK

The routing of the NoC in many-core systems allocates floorplan resources, which are scaling slower through technology advancements than high-density logic in conventional 2D systems. In this paper we compare fine-grained disintegration of the NoC channel routing through 3D-die stacking and signals routed on wafer backside. Physical modelling using a A10 nanosheet technology suggests that extending the backside metal stack with 2 or 3 dedicated, bidirectional routing layers provides a cost effective

scaling booster, and is preferable to heterogeneous 3D implementations. We estimate up to 20% lower cost over the 3D-stacking approach and 2D baseline at 3500 signals per channel-link.

10:45 AM

31-4 | Hyper RDL (HRDL) Interposer by Layer Transfer Technology for 3D IC and Advanced Packaging, Yu-Lun Liu, National Yang Ming Chiao Tung University|Chien-Kang Hsiung, National Yang Ming Chiao Tung University, Applied Materials Inc.|Chun-Ta Li, National Yang Ming Chiao Tung University|Tzu-Han Sun, National Yang Ming Chiao Tung University|Yu-Tao Yang, MediaTek USA Inc.|Wen-Tzu Tsai, National Yang Ming Chiao Tung University|Mu-Ping Hsu, National Yang Ming Chiao Tung University|Kuan-Neng Chen, National Yang Ming Chiao Tung University

Interposer technology is essential for electrical connections between dies and components. Among those interposer technologies, RDL offers improved signal integrity and cost reduction. This study expands on Hyper RDL (HRDL) interposers, using layer transfer and low-temperature hybrid bonding interconnects (LTHBI) to achieve multilayer stacking with reduced warpage and high flexibility in fine and coarse pitch RDL stacking design. Moreover, LTHBI enhances interposer integrity while lowering the thermal budget. Compared to conventional RDL interposers, HRDL demonstrates superior performance and flexibility, paving the way for the next generation packaging solutions, offering a multi layer, low-warpage, and cost-effective alternative for heterogeneous integration.

11:10 AM

31-5 | Selective Layer Transfer: Industry First Heterogeneous Integration Technology Enabling Ultra-Fast Assembly & Sub-1um Chiplet Thickness for Next Generation AI & Compute Applications, Adel Elsherbini1, Tushar Talukdar1, Thomas Sounart1, Paul Nordeen1, Andrey Vyatskikh1, Brandon Rawlings1, Feras Eid1, Mohammadreza, Yaghoobi2, Chytra Pawashe2, Grant Kloster1, Felipe Bedoya1, William Brezinski1, Richard Vreeland1, Marta Anguera Antonana1, Herbert, Barnett1, Georgios Dogiamis1, Qiang Yu3, Shawna Liff2, Johanna Swan1, Intel Foundry 1Technology Research, 2Logic Technology Development, 3Design Enablement

We present a novel heterogeneous integration technology, selective layer transfer (SLT), which enables ultra-fast (>100X faster than traditional assembly), cost efficient hybrid or fusion bonding of specific chiplets from one wafer (donor wafer) to another wafer (receiver wafer). SLT can enable a generation or more performance increase in AI accelerators. We will cover the process flow, the mechanical simulations of the different process steps, and the fabrication results of several test chips demonstrating the viability and flexibility of this technology. To our knowledge, this is the first demonstration in the literature of this capability.

11:35 AM

31-6 | Precise Alignment in Ultra-Thin (< 1 μm) Interlayer Wafer-Level Active Device Transfer with SOI Temporary Bonding, Bo-Jheng Shih, National Yang Ming Chiao Tung University|Shie-Ping Chang, National Yang Ming Chiao Tung University|Ting-Yu Chen, National Yang Ming Chiao Tung University|Zih-Yang Chen, National Yang Ming Chiao Tung University|Po-Jung Sung, Taiwan Semiconductor Research Institute|Nein-Chih Lin, Taiwan Semiconductor Research Institute|Chih-Chao Yang, Taiwan Semiconductor Research Institute|Po-Tsang Huang, National Yang Ming Chiao Tung University|Huang-Chung Cheng, National Yang Ming Chiao Tung University|Ming-Yang Li, Taiwan Semiconductor Manufacturing

Company|Iuliana P. Radu, Taiwan Semiconductor Manufacturing Company|Kuan-Neng Chen, National Yang Ming Chiao Tung University

This study introduces a groundbreaking SOI-based temporary bonding technique for 3DIC, resolving significant challenges in thermal management and interlayer alignment. This platform can achieve interlayer thickness below 1 μm, allowing precise visible-light alignment. Integrating advanced bonding, grinding, CMP, and wet etching, it is found that high Young's modulus adhesives can enhance the stability of remaining silicon under 10 μm during grinding and later completely be removed. Additionally, our thermal-aware partitioning and placement strategies reduce peak temperatures by 7.5%. This platform paves the way for the next generation of ultra-efficient and high-performance 3DIC.

12:00 PM
31-7 | Novel Parallel Digital Optical Computing System (DOC) for Generative A.I., Chun-Hao Fann, TSMC|Wei-Heng Lin, TSMC|Nien Fang Wu, TSMC|Jiun Yi Wu, TSMC|Harry Hsia, TSMC|Douglas C. H. Yu, TSMC

Generative A.I.'s (GAI) popularity has made photonics-based computation an attractive approach for its potential to meet the demands for higher energy efficiency performance (EEP). Here, a world's first on-chip large-scale Digital Optical Computing System (DOC) for GAI training is reported. DOC employs a novel wafer-based system integration technology featuring multilayer low-loss photonic interconnect fan-out (PIFO) and EIC/PIC stack architecture leveraging TSMC SoIC®. A low energy consumption of <0.1 pJ/MAC at 8-bit operation with a >15x EEP improvement compared to the state-of-the-art GPU [10] is achieved for a 512 x 512 MAC large scale operation.

12:25 PM
31-8 | EPIC-BOE: An Electronic-Photonic Chiplet Integration Technology with IC Processes for Broadband Optical Engine Applications, Harry Hsia, TSMC|J. Y. Wu, TSMC|S. W. Liang, TSMC|T. F. Tsai, TSMC|S. W. Lu, TSMC|C. W. Tseng, TSMC|H. K. Chiu, TSMC|C. C. Chang, TSMC|C. H. Tung, TSMC|C. S. Liu, TSMC|K. C. Yee, TSMC|Douglas C. H. Yu, TSMC
Speakers: Herbert Tseng, TSMC

Future GAI system demands more parallelism for performance with higher energy efficiency, high bandwidth density, and low latency than today's systems. We propose first full integration technology for Broadband Optical Engine (BOE) applications from fiber to CoWoS system by leveraging TSMC 3DFabricTM and IC processes forming compact CPOachieving GAI system PPA enhancement. It has high bandwidth coverage from 1260 to 1360 nm and high fiber count that vertical coupler enjoys.

33 | Focus Session | Emerging Power Electronic Devices and Integration for a Sustainable Society
9:00 AM – 12:50 PM, Continental 4
Co-Chairs: Kevin Chen, Hong Kong University of Science and Technology and Michael Waltl, TU Wien

The focus session on "Emerging Power Electronic Devices and Integration for a Sustainable Society" will highlight advancements and future trends in semiconductor technologies like GaN (Gallium Nitride) and SiC (Silicon Carbide), which are crucial for sustainable power electronics. It will begin with an introduction to a new CMOS-friendly, large-diameter substrate platform, emphasizing the importance of substrate innovation in advancing device technologies. Enhancements in SiC power devices for high-power

applications and the future potential of GaN in high-voltage, high-current, and bidirectional settings will also be explored. The session will cover deep P-Well technology to improve the performance of 1.2 kV 4H-SiC MOSFETs and introduce a novel approach combining a smart GaN HEMT with an IGBT. Reliability challenges in vertical GaN devices will be addressed, with insights from silicon and SiC technologies, and the session will conclude by discussing efforts to bridge the gap between state-of-the-art and space-grade power semiconductor devices, underscoring the need for reliability in extreme conditions.

09:00 AM
33-0 | Welcome

09:05 AM
33-1 | Substrate Innovation enabling advanced device technologies (Invited), Christophe. Maleville, SOITEC

Substrate Innovation enabling advanced device technologies

09:30 AM
33-2 | Propelling Widespread GaN Electronics Adoption With Large Diameter and CMOS Fab Friendly GaN-on-QST® Manufacturing Platform (Invited), Vladimir Odnoblyudov, QROMIS, Inc.|Cem Basceri, QROMIS, Inc.|Casey Kurth, QROMIS, Inc.|Masa Yamada, Shin-Etsu Chemical Co.|Shigeru Konishi, Shin-Etsu Chemical Co.|Minoru Kawahara, Shin-Etsu Chemical Co.|C.-C. Liao, Vanguard International Semiconductor Corp.|Shyh Shen, Vanguard International Semiconductor Corp.|Jeff Chiu, Vanguard International Semiconductor Corp.|Karen Geens, IMEC|Anurag Vohra, IMEC|Benoit Bakeroot, IMEC|Stefaan Decoutere, IMEC|Herwig Hahn, AIXTRON SE|Michael Heuken, AIXTRON SE

The SEMI standard thickness, CMOS fab-friendly and large diameter QST®(QROMIS Substrate Technology) substrates enable manufacturing of commercial high-performance GaN power devices. This is achieved by utilizing a polycrystalline ceramic substrate core with the coefficient of thermal expansion (CTE) matched to GaN. In this work, the status of 200mm and 300mm commercial QST®substrates and GaN-on-QST®epi-wafers will be discussed. The production status of 650V GaN-on-QST®E-mode HEMT devices on a commercial, high volume 200mm CMOS foundry manufacturing platform is presented. Also, the results of the development work in 200mm CMOS fabs on high-quality 1,200V E-mode HEMTs are included.

09:55 AM
33-3 | The Future of GaN is also High Voltage, High Current and Bidirectional (Invited), Umesh Mishra, University of California, Santa Barbara, Renesas Electronics|Davide Bisi, Renesas Electronics|Geetak Gupta, Renesas Electronics|Carl Neufeld, Renesas Electronics|Primit Parikh, Renesas Electronics

In this talk, we present latest breakthrough in high-power GaN technologies: high-voltage rating up to 1200 V, high-current rating up to 170 A for a single die, short-circuit capability up to 5 µs, and monolithic bi-directional switches for novel, more compact circuit topologies for lighter, smaller, more efficient and more reliable power conversion systems for data-centers, artificial intelligence, transportation, and much more.

10:45 AM

33-4 | Performance and reliability improvement trends in silicon carbide power devices (Invited), Hiroshi Kono, Toshiba Electronic Devices & Storage Corporation|Ryoichi Ohara, Toshiba Electronic Devices & Storage Corporation|Takuma Suzuki, Toshiba Electronic Devices & Storage Corporation|Shunsuke Asaba, Toshiba Electronic Devices & Storage Corporation|Kenya Sano, oshiba Electronic Devices & Storage Corporation

In this paper, we discuss technological trends in silicon carbide power devices in which both performance and reliability are continually improving. The impact of crystal defects in silicon carbide such as stacking faults and threading dislocations on the device is discussed, followed by a discussion of device structures that achieve both better performance and higher reliability by suppressing the influence of crystal defects.

11:10 AM
33-5 | Combo ICeGaN: The combination of a smart GaN HEMT and an IGBT (Invited), Florin Udrea, University of Cambridge

SiCandGaNdevices

11:35 AM
33-6 | Enhancing 1.2 kV 4H-SiC MOSFET Performance and Ruggedness through Deep P-Well Technology (Invited), Woongje Sung, University at Albany|Dongyoung Kim, University at Albany|Skylar deBoer, University at Albany|Justin Lynch, University at Albany|Seung Yup Jang, NoMIS Power Corporation|Adam Morgan, NoMIS Power Corporation

This paper presents advancements in 1.2 kV 4H-SiC MOSFETs with deep P-well by optimizing the JFET width and the channel length. Channeling implantation was used to form a deep junction with low implantation energy. Overall, the implementation of a short channel length and narrow JFET width with the deep P-well structure offers significantly enhanced conduction behaviors and switching characteristics, suitable for power converter applications.

12:00 PM
33-7 | Vertical GaN Devices: Reliability Challenges and Lessons Learned from Si and SiC (Invited), Matteo Meneghini, Univ. of Padova|Manuel Fregolent, Univ. of Padova|Nicolò Zagni, University of Modena and Reggio Emilia|Youssef Hamadoui, IEMN-CNRS|Alberto Marcuzzi, Univ. of Padova|Davide Favero, Univ. of Padova|Carlo De Santi, Univ. of Padova|Matteo Buffolo, Univ. of Padova|Marco Tomasi, Univ. of Padova|Giorgio Zappalà, Univ. of Padova|Eldad Bahat-Treidel, Ferdinand Braun Institut (Berlin, Germany)|Enrico Brusaterra, Ferdinand Braun Institut (Berlin, Germany)|Frank Brunner, Ferdinand Braun Institut (Berlin, Germany)|Oliver Hilt, Ferdinand Braun Institut (Berlin, Germany)|Christian Huber, Robert Bosch GmbH (Renningen, Germany) |Farid Medjdoub, IEMN-CNRS|Gaudenzio Meneghesso, Univ. of Padova|Giovanni Verzellesi, University of Modena and Reggio Emilia|Paolo Pavan, University of Modena and Reggio Emilia|Enrico Zanoni, Univ. of Padova

We discuss recent advancements in the development of vertical GaN devices, and the related reliability challenges. Results indicate that: (i) vertical GaN devices can show high performance, low background doping, and kV-range breakdown voltages; avalanche capability (a property of Si and SiC devices) is demonstrated also for vertical devices on silicon substrate; (ii)threshold voltage instabilities are related to

the presence of traps, whose contribution can be modeled with great accuracy; (iii) gate stack reliability is mainly limited by oxide breakdown; factors limiting off-state failure are discussed.

12:25 PM
33-8 | Closing the Gap Between State-of-the-Art and Space Grade Power Semiconductor Devices (Invited), Eric Faraci, Infineon Technologies

Placeholder per discussion with Srabanti. Will submit full abstract by 9/15 at the latest.Paper will discuss market trends in space, where power requirements are increasing and reliability requirements are component level are changing. Historically there has been a large gap in performance between commercial-off-the-shelf (COTS) vs. space grade semiconductor components, this paper will discuss how this gap is being reduced. Will go into details about bringing power GaN HEMT and state-of-the-art high voltage power 130 nm Si BiCMOS process to space market, including radiation hardening and reliability.

34 | RSD | Transistor Reliability with Novel Processes, Materials and Evaluation Methodologies
9:00 AM – 12:50 PM, Continental 5
Co-Chairs: Bonnie Weir, Broadcom and Huimei Zhou, IBM

In this session, reliability mechanisms are studied for a variety of process conditions, transistor types, and materials; low-thermal-budget, IGZO, SiC, IWO, and finFETs under AC and DC stress. First, an analysis of the reliability of a novel low-thermal-budget multi-threshold-voltage replacement-gate transistor is described, followed by a paper comparing top-gate and bottom-gate reliability of IGZO devices demonstrating stable threshold-voltage behavior for indium content below 5%. The third paper explores bias-temperature instability of IGZTO devices under both AC and DC stress. Fourth, an invited paper gives a status overview of planar-gate silicon-carbide transistor reliability. Next, dynamic variation of on-current and sub-threshold slope of finFETs vs. temperature down to the cryogenic regime is comprehensively investigated. The sixth paper presents a low-thermal-budget reliable dual-gate IWO transistor solution for on-chip DC-DC conversion. The final two papers explore HKMG finFET TDDB under AC and off-state stress. AC stress up to 15 GHz shows improved TDDB lifetime vs. DC stress. The effect of off-state stress on TDDB and transistor aging is demonstrated as a function of source-drain current during stress.

09:00 AM
34-0 | Welcome

09:05 AM
34-1 | Low Thermal Budget Multi-Vth RMG solution with excellent TDDB and BTI Reliability by combining hydrogen radical IL treatment, n-dipole-first shifter and low-temperature HK PDA,
Jacopo Franco, imec|Hiroaki Arimura, imec|Andrea Vici, imec|Jean-Francois de Marneffe, imec|Giorgio Molinaro, imec|Jishnu Ganguly, imec|Leo Lukose, imec|Robin Degraeve, imec|Ben Kaczer, imec|Hans Mertens, imec|Min-Soo Kim, imec|Naoto Horiguchi, imec

We demonstrate a low thermal budget multi-Vth RMG scheme yielding four pMOS/nMOS flavors using only two metals and one dipole shifter material, and adopting the same low-temperature treatments for all the devices, namely a new thermally stable hydrogen radical IL treatment and a long HK PDA for sufficient BTI/TDDB reliability.

09:30 AM

34-2 | Unraveling BTI in IGZO devices: impact of device architecture, channel film deposition method and stoichiometry/phase, and device operating conditions, Adrian Chasin, imec|Jacopo Franco, imec|Simon Van Beek, imec|Harold Dekkers, imec|Anastasiia Kruv, imec|Pietro Rinaudo, imec, KULeuven|Ying Zhao, imec, KULeuven|Daisuke Matsubayashi, imec|Alexandru Pavel, imec|Yiqun Wan, imec|Kruti Trivedi, imec|Nouredine Rassoul, imec|Jie Li, imec|Yuchao Jiang, imec|Michiel Van Setten, imec|Subhali Subhechha, imec|Attilio Belmonte, imec|Ben Kaczer, imec|Gouri Kar, imec

We study the impact of the device architecture, channel deposition method, stoichiometry and phase, and AC stress on the BTI of IGZO transistors. Two main conclusions are obtained. Firstly, reliability of IGZO based devices is strongly architecture dependent, and therefore reliability solutions are not universal. Secondly, top-gate devices are more severely impacted by the abnormal negative ΔV_{th}, ascribed to a H-doping process, than back-gated counterparts. Two remedies for the negative ΔV_{th} are identified: In-poor films and AC stress with duty-cycle<25% do not reveal sings of H-doping process within the experimental time window, promising for reliable product operation.

09:55 AM

34-3 | Revealing the Impact of Hydrogen (H) on NBTI/PBTI of IGZTO FETs Under DC and AC Stress: Deep Dive into H Dynamics and Advanced Modeling, Gan Liu, National University of Singapore|Zhilun Zhang, National University of Singapore|Duy Hieu Trinh, National University of Singapore|Hanjie Li, National University of Singapore|Qiwen Kong, National University of Singapore|Chen Sun, National University of Singapore|Zuopu Zhou, National University of Singapore|Dong Zhang, National University of Singapore|Xiaolin Wang, National University of Singapore|Kaizhen Han, National University of Singapore|Yuye Kang, National University of Singapore|Bich-Yen Nguyen, Soitec|Kai Ni, University of Notre Dame|Gengchiau Liang, National University of Singapore, Industry Academia Innovation School, National Yang-Ming Chiao Tung University|Xiao Gong, National University of Singapore

In this work, we present a systematic and comprehensiveinvestigation into the impact of hydrogen (H) on the reliability performanceof IGZTO FETs. Our research unveils: (1) DC NBTIresults exhibit saturation behavior and are less severe than PBTI. (2) H^+ involved in NBTI experiences minimal response to AC stress, resulting inultra-stable AC performance. Using a novel test vehicle, the presence of H^+ in the oxide semiconductor (OS) system is experimentally identified andconfirmed for the first time. A model was further proposed and extended toaccurately describe the threshold voltage shift (ΔV_{th}) through AC BTIprocess.

10:45 AM

34-4 | A Status Overview of SiC MOSFET Reliability (Invited), Peter Moens, onsemi|Sotirios Maslougkas, onsemi|Marina Avramenko, onsemi|German Gomez-Garcia, onsemi|Sara Kuzmanoska, onsemi|martin domeij, onsemi

This paper provides a status overview of SiC transistor reliability, with focus on a commercially released planar gate technology with a thermally grown gate oxide. Gate dielectric lifetime from time dependent dielectric breakdown (TDDB), lifetime under reverse drain bias, susceptibility to single event burn-out under neutron irradiation, bias temperature instability (BTI), gate switching instability (GSI), and bipolar degradation are discussed. Experimental data, modeling and lifetime projections are provided with a focus on automotive traction applications.

11:10 AM

34-5 | Towards Understanding the Dynamic Variation in FinFET at Cryogenic Temperature: New Observations and Physical Modeling, Zirui Wang, Peking University|Haoran Wang, Beihang University|Wen-Feng Li, Institute of Semiconductors, Chinese Academy of Sciences|Yuxiao Wang, Beihang University|Zixuan Sun, Peking University|Anyi Zhu, Peking University|Lang Zeng, Beihang University|Yue-Yang Liu, Institute of Semiconductors, Chinese Academy of Sciences|Runsheng Wang, Peking University|Ru huang, Peking University

The dynamic variability at cryogenic temperature for FinFET are comprehensively studied for the first time. (1) drain current relaxation accompanied with decreasing SS and increasing I_{on}, which causes cycle-to-cycle variations and SS-T fluctuations. (2) SS deviates from the Boltzmann limit early around 150K and gradually saturate towards 50K. (3) Evident protrusion along with clockwise hysteresis. These new findings are well understood in the unified framework of band tail states induced by dopant, roughness and interface state. Based on the physics, a self-consistent statistical simulation method is developed, This work provides deep understandings for cryogenic CMOS instability and reliability.

11:35 AM

34-6 | Boosted Performance and Enhanced Reliability of BEOL-Compatible Dual-Gate Oxide Power Transistors for On-Chip DC-DC Voltage Conversion, Sunbin Deng, Georgia Institute of Technology|Jaewon Shin, Georgia Institute of Technology|Chengyang Zhang, Georgia Institute of Technology|Hyeonwoo Park, Georgia Institute of Technology|Omkar Phadke, Georgia Institute of Technology|Jungyoun Kwak, Georgia Institute of Technology, Georgia Institute of Technology|Shimeng Yu, Georgia Institute of Technology, Georgia Institute of Technology|Suman Datta, Georgia Institute of Technology

We experimentally demonstrated dual-gate (DG) tungsten-doped indium oxide (IWO) power transistors for efficient on-chip voltage conversion in heterogeneous three-dimensional integrated systems. Compared to single-gate counterparts, DG devices exhibited boosted performance with ~5.5x increase in breakdown voltage and ~2x reduction in subthreshold swing and enhanced reliability with up to 6x reduction in DC BTI-induced $\Delta V_{th}$and near-zero HCD-induced ΔV_{th}. Comprehensive reliability characterization highlighted the vital role that ΔV_{th} compensatory effect held in enhancing reliability of the DG devices. We also observed distinct degradation behaviors between DC and AC electrical stresses due to the reduced responsiveness of hydrogen impurities to higher-frequency signals.

12:00 PM

34-7 | Fine characterization and Modeling of the Frequency Dependence of TDDB in RF domain (F>10GHz), Alexis Divay, CEA-LETI|Tarek Daher, CEA-LETI|Léo Basset, CEA-LETI|Serge Blonkowski, CEA-LETI|Xavier Federspiel, ST Microelectronics|David Roy, ST Microelectronics|Fred Gaillard, CEA-LETI|Blandine Duriez, CEA-LETI|Xavier Garros, CEA-LETI

An innovative and reliable RF setup based on sine wave stress is proposed, revealing for the first time that TDDB follows a kind of power law with frequency up to 15 GHz. A physical model based on dielectric relaxation is then proposed to explain the increase in TDDB with frequency. Finally, by using an effective duty factor for RF, AC and RF sine waves can be matched to derive a universal TDDB frequency behavior that is independent of the signal waveform.

12:25 PM
34-8 | Design Strategy for Mitigating Off-state Current Degradation in Non-Conductive Stress (NCS) Reliability, P.J. Liao, TSMC|Y.K. Chang, TSMC|C.M. Fu, TSMC|C.T. Ou, TSMC|C.M. Lin, TSMC|K.Y. Chia, TSMC|J.H. Lee, TSMC|W.H. Chuang, TSMC|Ryan Lu, TSMC|Jun He, TSMC

In this work, a systematic non-conductive stress is applied to understand NCS acceleration lifetime model for circuit applications at off-state high drain bias. A study on a wide voltage range NCS validated the ISOFF and VDG accelerated IDOFF degradation lifetime model. The defined reliability boundary based on application-specific mission profiles provides guidance on the "Design for Reliability" (DFR) workflow for optimizing circuit design to mitigate off-state reliability risks before multi-project-wafer verification.

Coffee break with Exhibitors
10:20 AM – 11:10 AM
Yosemite

Coffee break with Exhibitors

37 | MT | Materials and Process Advances for Ferroelectric Memory Applications
1:30 PM – 4:30 PM, Grand Ballroom A
Co-Chair: Nanbo Gong, IBM and Yu-Ming Lin, TSMC

This session contains 6 papers and will cover recent advances in HfO2-based ferroelectric materials optimization strategies for memory applications. In the first paper by Pohang University of Science and Technology (POSTECH), Hwang et al. demonstrated high-performance HZO-based ferroelectric capacitors with vertically well-ordered domain structures by inserting a ultra-thin 2D-WS2 bottom interfacial layer. The second paper (by KAIST and Samsung R&D) provided a new design methodology for FeRAM cell capacitor that operates at low voltage ($\leq$ 1 V) with steep polarization (ΔP) switching characteristics and overcomes disturbance issue with AFE domain engineering. The third paper (by S. Cao et al.) focused on the development of cross-point FeRAM and comprehensively investigated its application for embedded and standalone memories. The fourth paper from KAIST demonstrated 32 Kb ferroelectric random access memory array using 3D trench ferroelectric capacitor with great uniformity and excellent high temperature retention characteristics for over 10 years at 175 ℃. The last two papers, both by imec, showcased the use of IGZO in combination with ferroelectric materials to demonstrated new and improved memory applications, including an enlarged capacitive memory window (CMW) in FeCAPs (by S. Mukherjee et al.) and a novel 3D Charge Coupled Device (CCD) for high density block addressable buffer memory (by R. Kishore et al.)

01:30 PM
37-0 | Welcome

01:35 PM
37-1 | Record Endurance (> 1012 cycles), High Polarization (2Pr > 50 μC/cm2), and 10-year Data Retention (85 oC) in HZO Capacitors with Well-Ordered Ferroelectric Domain Structures via 2D-WS2 Interface, Seungkwon Hwang, Pohang University of Science and Technology (POSTECH), Korea Institute of Materials Science (KIMS)|Hojung Jang, Pohang University of Science and Technology

(POSTECH)|Kyumin Lee, Pohang University of Science and Technology (POSTECH)|Laeyong Jung, Pohang University of Science and Technology (POSTECH)|Jongwon Yoon, Korea Institute of Materials Science (KIMS)|Jung-Dae Kwon, Korea Institute of Materials Science (KIMS)|Kyung Song, Korea Institute of Materials Science (KIMS)|Yonghun Kim, Korea Institute of Materials Science (KIMS)|Hyunsang Hwang, Pohang University of Science and Technology (POSTECH)

We demonstrate high-performance $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric capacitors with vertically ordered domains by integrating a 2D-WS_2 layer. WS_2 serves as protective and seed layer, enhancing interfacial stability and domain order. Our capacitors achieve excellent ferroelectricity, abrupt switching, over 10^{12} cycles endurance, high polarization (> 50 μC/cm²), and over 10 years data retention.

02:00 PM
37-2 | Design Methodology for Low-Voltage Operational (≤1 V) FRAM Cell Capacitors and Approaches for Overcoming Disturb Issues in 1T-nC Arrays: Experimental & Modeling, Sangho Lee, KAIST|Giuk Kim, KAIST| Chaeheon Kim, KAIST|Yunseok Nam, KAIST|Junghyeon Hwang, KAIST|Yangjin Jung, KAIST|Mincheol Shin, KAIST|Youngin Goh, Samsung Electronics|Mintae Ryu, Samsung Electronics|Jihye Suh, Samsung Electronics|Kilho Lee, Samsung Electronics|Wanki Kim, Samsung Electronics|Daewon Ha, Samsung Electronics|Jinho Ahn, Hanyang University|Sanghun Jeon, KAIST

We propose a methodology for designing an FRAM cell capacitor operating at ≤ 1 V, achieving high ΔP switching (23.5 μC/cm²), and ensuring BEOL compatibility (≤ 400 ℃). Our model framework validates that steep ΔP switching mitigates disturbance in 1T-nC FRAM arrays, and demonstrates the optimal number of cell capacitors.

02:25 PM
37-3 | Comprehensive Performance Re-assessment of Hafnia-based Cross-point FeRAM with Ultra-fast and Low-power Operation from Device/Array Perspective, Shengjie Cao, School of Integrated Circuits, Peking University|Zhiyuan Fu, School of Integrated Circuits, Peking University|Minyue Deng, School of Integrated Circuits, Peking University|Hao Zheng, School of Integrated Circuits, Peking University|Qianqian Huang, School of Integrated Circuits, Peking University|Ru Huang, School of Integrated Circuits, Peking University

In this work, hafnia-based selector-less cross-point FeRAM (XP-FeRAM) with ultra-fast and low-power operation is experimentally demonstrated from device-level optimization to array-level evaluation for embedded and standalone memories. For device optimization, the impacts of ferroelectric (FE) layer deposition process sequence considering different applications are investigated for the first time with the awareness of switching speed. Moreover, from array perspective, a modified V/2 operation scheme with in-situ write-back is further proposed and experimentally demonstrated in the fabricated XP-FeRAM array, Additionally, memory performances and scalability design spaces are robustly evaluated, showing the great potential of XP-FeRAMs for high-speed, high-density and low-power memory applications.

03:15 PM
37-4 | 3D trench Hf0.5Zr0.5O2-based 32 Kbit 1T1C FeRAM Chip with 2/5 ns Write/Read speed, Low power consumption (0.605 pJ/bit) and Prominent High-temperature Reliability (baking @ 175℃), Jiajie Yu, Fudan University, National Integrated Circuit Innovation Center, China Resources Microelectronics Limited|Shuming Guo, China Resources Microelectronics Limited|Jinna Zhang, Fudan

University|Xingcheng Jin, China Resources Microelectronics Limited|Chao Wu, Fudan University|Minghao Zhao, China Resources Microelectronics Limited|Hongbo Li, China Resources Microelectronics Limited|Chongyong Guo, China Resources Microelectronics Limited|Kangli Xu, Fudan University|Yuxin Tian, Fudan University|Dong Tian, Fudan University|Zhenhai Li, Fudan University|Tianyu Wang, National Integrated Circuit Innovation Center|Hao Zhu, Fudan University, National Integrated Circuit Innovation Center|Qingqing Sun, Fudan University, National Integrated Circuit Innovation Center|Yufeng Xie, Fudan University, National Integrated Circuit Innovation Center|Hao Wang, China Resources Microelectronics Limited|David Wei Zhang, Fudan University, National Integrated Circuit Innovation Center|Lin Chen, Fudan University, National Integrated Circuit Innovation Center

A 32 Kb 3D HZO FeRAM with 2Pr ~35 uC/cm2 at 1.8 V, 0.07 um2 capacitors area, 10 years at 175 ℃ retention, 2/5 ns write/read, 1012 cycles endurance, and 0.605 pJ/bit power consumption, high yield (>96%) at 175 ℃ and 100% pass rate after 140 hours is proposed.

03:40 PM
37-5 | Improved Capacitive Memory Window for Non-destructive Read in HZO-based Ferroelectric Capacitors with Incorporation of Semiconducting IGZO, Shankha Mukherjee, imec, KU Leuven|Jasper Bizindavyi, imec|Sergiu Clima, imec|Yang Xiang, imec|Mihaela Popovici, imec|Attilio Belmonte, imec|Roman Izmailov, imec, KU Leuven|Jimmy Stiers, imec|Anastasiia Kruv, imec|Subhali Subhechha, imec|Harold Dekkers, imec|GouriSankar Kar, imec|Gourab De, imec, KU Leuven|Nicolo Ronchi, imec|Zied Belkhiri, imec|Geert Van den Bosch, imec|Maarten Rosmeulen, imec|Francky Catthoor, imec, KU Leuven|Shimeng Yu, Georgia Institute of Technology|Valeri Afanas'ev, KU Leuven, imec|Jan Van Houdt, imec, KU Leuven

In this work, we show an improved ferroelectric (FE) capacitive memory window (CMW) by integrating asemiconducting IGZO layer into FE capacitors and achieve, after optimizingthe stack,a record high CMW for non-destructive read. Furthermore, we demonstrate the first CMW in 3D memory devices in a NAND array configuration.

04:05 PM
37-6 | Novel High Density 3D Buffer Memory Enabled by IGZO Channel Charge Coupled Device, Rishabh Kishore, imec|Swaraj Bandhu Mahato, imec|Subhali Subhechha, imec|Jiwon Lee, imec|Ruben Bonne, imec|Yiqun Wan, imec|Nouredine Rassoul, imec|Sana Rachidi, imec|Jie Li, imec|Yuchao Jiang, imec|Bowen Wang, imec|Attilio Belmonte, imec|Gouri Kar, imec|Maarten Rosmeulen, imec

We present a novel 3D Charge Coupled Device (CCD) with IGZO channel for high density block addressable buffer memory integrable in 3D NAND Flash string architecture. The concept is demonstrated using planar 4-phase CCD structure with 142-bits featuring efficient and fast charge transfer, long retention, large endurance, and multilevel capability.

39 | ALT | Interconnect and Contact Process Technology
1:30 PM – 4:30 PM, Continental 1 – 3
Co-Chairs: Martin OToole, ASML and Kazuyuki Tomida, Rapidus

This session includes six papers that describe recent advances in the area of interconnect and contact process technology. The first two papers from IBM and Intel demonstrate a subtractive Ru BEOL interconnect with an air gap technology that enables resistance and capacitance improvements needed for future scaling nodes. The third paper from IMEC leverages these subtractive metal etch processes to fabricate the devices needed for a superconducting digital logic technology. The fourth paper by Samsung describes graphene as a conductor candidate for future interconnects. The last two papers from IMEC discuss the challenges and opportunities reducing contact resistance. The fifth paper explores the potential of Nb contacts which can deliver a 35% decrease in the parasitic resistance. The final paper explores a new methodology to perform the direct extraction of contact and source/drain epi resistance components in NS-based n-FET devices.

01:30 PM
39-0 | Welcome

01:35 PM
39-1 | Fully subtractive Ru Topvia interconnects with minimum 9 nm-space airgap for RC performance and reliability enhancement as post-Cu interconnects, Koichi Motoyama, IBM Research|Jaemyung Choi, Samsung Electronics|Huai Huang, IBM Research|Chris Penny, IBM Research|Nick Lanzillo, IBM Research|Johnsoo Kim, Samsung Electronics|Joongsuk Oh, Samsung Electronics|Gwangsik Kim, Samsung Electronics|Janggeun Lee, Samsung Electronics|Sejun Park, Samsung Electronics|Taesun Kim, Samsung Electronics|Shobha Hosadurga, IBM Research|Darsith Jayachandran, IBM Research|Haojun Zhang, IBM Research|Joe Lee, IBM Research|Shravana Katakam, IBM Research|Gideon Oyibo, IBM Research|Wei-Tsu Tseng, IBM Research|Belle Antonovich, IBM Research|Nicholas Latham, IBM Research|Wai Kin Li, IBM Research|Chung Ju Yang, IBM Research|Samuel Munnangi, IBM Research|Andy Simon, IBM Research|Su Chen Fan, IBM Research|John Arnold, IBM Research|Tenko Yamashita, IBM Research|Kisik Choi, IBM Research|Kang-ill Seo , Samsung Electronics|Dechao Guo, IBM Research|Huiming Bu, IBM Research

Minimum 18 nm pitch fully subtractive self-aligned Ru Topvia interconnects with embedded airgap have been demonstrated. It has been confirmed that Ru Topvia interconnects with Topvia trimming process can improve dielectric breakdown voltage between vias and adjacent lines, which is essential for future CMOS technologies. Moreover, in comparison to conventional damascene Cu interconnects with low-k, Ru top via interconnects with airgap provided a clear advantage, exhibiting 23% lower capacitance. Furthermore, excellent TDDB performance on subtractive Ru interconnects with 9 nm-space airgap has been obtained and superior EM performance of Ru Topvia interconnects has been achieved.

02:00 PM
39-2 | Subtractive Ruthenium Interconnects with Airgap, Ananya Dutta, Intel Corporation|Akshit Peer, Intel Corporation|Christopher Jezewski, Intel Corporation|Saima Siddiqui, Intel Corporation|Ian Jenkins, Intel Corporation|Emmannuel Khora, Intel Corporation|Gauri Auluck, Intel Corporation|YuWen Huang, Intel Corporation|Felipe Bedoya, Intel Corporation|Nafees Kabir, Intel Corporation|Supriya Mocherla, Intel Corporation|Puja Rani Saha, Intel Corporation|Leah Shoer, Intel Corporation|Kyle Chan, Intel Corporation|Akhilesh Tanneeru, Intel Corporation|Jay P Gupta, Intel Corporation|Vijay Bharamaiah Jeevendrakumar, Intel Corporation|David E Collins, Intel Corporation|Syam Madhusoodhanan, Intel Corporation|Jeff Bielefeld, Intel Corporation|William Brezinski, Intel Corporation|Remi Fayad, Intel Corporation|Supanee Sukrittanon, Intel Corporation|Sudipto Naskar, Intel Corporation|Sreenivas Kosaraju,

Intel Corporation|Nityan Nair, Intel Corporation|Gurpreet Singh, Intel Corporation| Joseph D Silva, Intel Corporation|Clifford J Engel, Intel Corporation|Franco Noel, Intel Corporation|Brian J Krist, Intel Corporation|Jimmy Wang, Intel Corporation|Matthew V Metz, Intel Corporation|Mauro J Kobrinsky, Intel Corporation

Subtractive ruthenium interconnects are being researched as a metallization scheme to replace damascene Cu in tight pitch interconnect layers. In this paper, we present R&D results obtained in a 3-layer stack test vehicle with standard performance and defectivity structures, which include resistance (R) and capacitance (C) benefits, and defect densities for via chains and leakage combs. In addition, we identify key performance enhancement factors that decrease Ru resistance by up to 15%. Furthermore, we report an airgap flow with robust next-via landing process, capable of providing 25% of line-line capacitance reduction.

02:25 PM
39-3 | NbTiN based two-metal level semi-damascene interconnects, Josephson junctions and capacitors for Superconducting Digital Logic, Ankit Pokhrel, IMEC|Daniel Perez Lozano, IMEC|Jean-Philippe Soulie, IMEC|Diziana Vangoidsenhoven, IMEC|Sujan Sarkar, IMEC|Rajendra Saroj, IMEC|Yann Canvel, IMEC|Vincent Renaud, IMEC|Bart Kenens, IMEC|Amey Walke, IMEC|Jasper Bizindavyi, IMEC|Sara Iraci, IMEC|Seifallah Ibrahim, IMEC USA|Blake Hodges, IMEC USA|Trent Josephsen, IMEC USA|Manu Perumkunnil, IMEC|Benjamin Huet, IMEC|Sabine O'Neal, IMEC USA|Quentin Herr, IMEC USA, IMEC|Zsolt Tokei, IMEC|Anna Herr, IMEC USA, IMEC

Superconducting Digital (SCD) is a promising alternative to CMOS technology, enabling energy-efficient High-Performance Computing. We report the fabrication of three key devices for SCD: NbTiN BEOL interconnects, NbTiN/αSi/NbTiN Josephson junctions (JJs), and NbTiN/HZO/NbTiN Metal-Insulator-Metal (MIM) capacitors. Material characterization demonstrate high-quality devices with critical dimensions down to 50 nm. NbTiN interconnects have critical temperature >13K and high critical current density (Jc) >120 mA/μm^2, JJs have Jc of 0.4 mA/μm^2. MIM capacitors have high specific capacitance of ~28 fF/μm^2 (k-value=30). Devices were fabricated using CMOS compatible processes below 420^{o}C on 300mm wafers, bridging the gap from feasibility to industrial fabrication.

02:50 PM
39-4 | Graphene as new conductors in Back-End-Of-Line: non-catalytic growth, doping, integration and reliability, Keun Wook Shin, Samsung Advanced Institute of Technology|Changhyun Kim, Samsung Advanced Institute of Technology|Sangjun Lee, Samsung Advanced Institute of Technology|Joung Eun Yoo, Samsung Advanced Institute of Technology|Baekwon Park, Samsung Advanced Institute of Technology|Eun-Kyu Lee, Samsung Advanced Institute of Technology|Dong-Su Ko, Samsung Advanced Institute of Technology|Alum Jung, Samsung Advanced Institute of Technology|Dae-Jin Yang, Samsung Advanced Institute of Technology|Chang-Seok Lee, Samsung Advanced Institute of Technology|Sang Won Kim, Samsung Advanced Institute of Technology|Kyung-Eun Byun, Samsung Advanced Institute of Technology

In this study, we conduct a comprehensive investigation into the development of CMOS-compatible graphene as a new conductor in BEOL, focusing on non-catalytic growth, doping, integration, and reliability. We demonstrate the non-catalytic growth of multilayer graphene on SiO_2 at around 500 ^{o}C by ICP-CVD. We observe a resistivity of 110 μohm-cm at 2.3 nm, upon doping with $AuCl_3$. MLG is

successfully integrated into a three-dimensional trench and implement a line pattern to evaluate the electrical characteristics and reliability of the world's first non-catalytic grown MLG wiring.

03:40 PM
39-5 | Nb Contacts for Thermally-stable High-performance Logic and Memory Peripheral Transistor, Ritam Sarkar, IMEC|Romain Ritzenthaler, IMEC|Jean Luc Everaert, IMEC|Pierre Eyben, IMEC|Kiroubanand Sankaran, IMEC| Clément Porret, IMEC|Prafulla Gupta, IMEC|Jishnu Ganguly, IMEC|Hiroaki Arimura, IMEC|Jef Geypen, IMEC|Elena Capogreco, IMEC|Saemi Roh, SK Hynix|Vladimir Machkaoutsan, Micron Technology|Lucas PB Lima , IMEC|Min Kim, IMEC|Alessio Spessot , IMEC|Naoto Horiguchi , IMEC

We report on the first demonstration of Nb as a thermally stable contact metal having a low contact resistivity in CTLM and FinFET platforms for both logic and memory peri applications. Nb exhibits a 35% decrease in the parasitic resistance, along with 3x reduction in post DRAM anneal contact resistivity.

04:05 PM
39-6 | Direct extraction of contact and S/D epi access resistance components on 45nm Gate Pitch NS-based n-FET devices for the 2nm node, Pierre Eyben, IMEC|Andrea Pondini, IMEC, KULeuven|An De Keersgieter, IMEC|Hiroaki Arimura, IMEC|Hans Mertens, IMEC|Thomas Chiarella, IMEC|Clément Porret, IMEC|Erik Rosseel, IMEC|Ritam Sarkar, IMEC|Maryam Hosseini, IMEC|Xiuju Zhou, IMEC|Lennaert Wouters, IMEC|Philippe Matagne, IMEC|Jerome Mitard, IMEC|Naoto Horiguchi, IMEC

We report on a new methodology to perform direct extraction of contact and source/drain epi resistance components in NS-based n-FET device (n-NSFET) with 45nm Gate Pitch and 16nm Gate Length. We have combined this method with advanced metrology (XTEM and scalpel SSRM) to analyze the device topology and carrier distribution, and to extract contact resistivity. We have investigated the impact of post S/D epi spike anneal and compared the results with reference contact resistivity values extracted on TLM test-structures. We have used this information to calibrate a TCAD deck and propose solutions to boost device performance.

42 | EDT | Magnetic Devices for Memory and Computing
1:30 PM – 4:30 PM, Continental 7 – 9
Co-Chairs: Louis Hutin, CEA-Leti and Qiming Shao, Hong Kong University of Science & Technology

This session presents the latest research that addresses key challenges in MRAM technology, from achieving ultra-low error rates and power consumption to ensuring magnetic field immunity. It will also cover emerging applications in unconventional computing and energy harvesting, offering a glimpse into the future of magnetic device technologies. The first paper from IMEC presents a novel approach to achieving a low write-error rate of 1 part per million in spin-orbit torque magnetic random-access memory (SOT-MRAM) by utilizing a synthetic antiferromagnetic free layer in the magnetic tunnel junction stack. The second paper from Truth Memory Technology Corporation presents the first experimental demonstration of a CMOS-integrated 128 Kb antiferromagnet-based MRAM that is immune to magnetic fields up to 3 T for applications, where resilience to electromagnetic interference is critical. The third paper from ShanghaiTech University presents a novel field-free switching scheme for MRAM using Rashba-type crystal spin-orbit torque in wafer-scale semiconductor compound heterostructures with an ultra-low write current density and stable operation across a wide temperature range (−40°C to 125°C). The fourth paper from Zhejiang Hikstor Technology Co. LTD presents a novel channel-less SOT-MRAM

device that achieves over 99.9% bit yield and shows a 16.5% reduction in critical switching current, making it highly suitable for large-scale MRAM chip fabrication. The fifth paper from the Hong Kong University of Science and Technology presents a novel cryogenic in-memory computing architecture using magnetic topological insulators for neural network accelerators, operating at temperatures at 2 K and achieving software-level accuracy in quantum control tasks. The last invited paper from the National University of Singapore discusses recent advances in spintronic devices for applications in nonvolatile memories, unconventional computing, and energy harvesting, highlighting the challenges and potential solutions.

01:30 PM
42-0 | Welcome

01:35 PM
42-1 | Achieving 1ppm write-error rate in SOT-MRAM with synthetic antiferromagnetic free layer, Dai Nguyen, IMEC|Giacomo Talmelli, IMEC|Maxwel Gama Monteiro, IMEC|Alvaro Palomino Lopez, IMEC|Vaishnavi Kateel, IMEC|Domenico Giuliano, IMEC, KUL|Simon Van Beek, IMEC|Natan Vandermeeren, IMEC, KUL|Nathali Franchina, IMEC|Kurt Wostyn, IMEC|Sebastien Couet, IMEC

We demonstrate functionality of a perpendicular SOT-MRAM with a synthetic antiferromagnetic-based free layer MTJ, reducing the write error rate to 10^{-6} and maintaining BEOL compatibility at 400 ^{o}C. Micromagnetic simulations guide material selection, ensuring reliable device operation for experimental validation. These devices fabricated on 300 mm wafers advance technological integration.

02:00 PM
42-2 | First CMOS-integrated 128 Kb antiferromagnet-based MRAM with immunity to 3 T magnetic fields, Danrong Xiong, Truth Memory Tech. Corporation|Xiaofei Fan, Truth Memory Tech. Corporation|Chuanpeng Jiang, Beihang University|Gefei Wang, Truth Memory Tech. Corporation|Hong-xi Liu, Truth Memory Tech. Corporation|Shiyang Lu, Beihang University|Hongchao Zhang, Truth Memory Tech. Corporation|Jinhao Li, Beihang University|He Zhang, Beihang University|Kaihua Cao, Beihang University|Zhaohao Wang, Beihang University|Weisheng Zhao, Beihang University

We demonstrate the first-ever CMOS-integrated 128 Kb antiferromagnet-based MRAM, i.e., ARAM, with immunity to 3 T magnetic fields. These devices achieve 0.2 ns ultrafast field-free switching and 10^{10} robust endurance. The ARAM holds great promise for applications such as autonomous vehicles and space exploration, offering resilience against electromagnetic interference.

02:25 PM
42-3 | Field-Free Rashba-Type Crystal Torque MRAM with High Efficiency and Thermal Stability, Puyang Huang, ShanghaiTech University|Shan Yao, ShanghaiTech University|Aitian Chen, University of Electronic Science and Technology of China, King Abdullah University of Science and Technology|Zhenghang Zhi, ShanghaiTech University|Chenyi Fu, Beihang University|Zheng Zhu, Suzhou Inston Technology Co., Ltd.|Peng Chen, Songshan Lake Materials Laboratory|Hao Wu, Songshan Lake Materials Laboratory|Di Wu, Suzhou Inston Technology Co., Ltd.|Shouzhong Peng, Beihang University|Yumeng Yang, ShanghaiTech University|Xixiang Zhang, King Abdullah University of Science and Technology|Xufeng Kou, ShanghaiTech University

We report a field-free switching (FFS) scheme of Rashba-type crystal torque magnetic random-access memory (CT-MRAM) based on the AlInSb/InSb/CdTe heterostructures. Benefiting from the giant interfacial Rashba spin-orbit coupling (SOC), the spin-orbit torque efficiency of the spingeneration channel (ξ = 1.5) is four times larger than the conventional heavy-metal systems, enabling an ultra-low write current density of JSW = 7.5 × 105 A/cm2 at room temperature. Moreover, the crystal torque inherited from the low-symmetry point group (3m1) not only simplifies the device structure, but also warrants a stable FFS operation over a wide temperature range from -40 ℃ to 125 ℃.

02:50 PM
42-4 | A novel Channel-less SOT-MRAM with 115% TMR, 2 ns Switching, and High Bit Yield (>99.9%), Enlong Liu, Zhejiang Hikstor Technology Co. LTD|Wenlong Yang, Zhejiang Hikstor Technology Co. LTD|Kaiyuan Zhou, Zhejiang Hikstor Technology Co. LTD|Yang Gao, Zhejiang Hikstor Technology Co. LTD|Zhenghui Ji, Zhejiang Hikstor Technology Co. LTD|Dinggui Zeng, Zhejiang Hikstor Technology Co. LTD|Ming Wang, Zhejiang Hikstor Technology Co. LTD|Qingxiu Li, Zhejiang Hikstor Technology Co. LTD|Yifan Xi, Zhejiang Hikstor Technology Co. LTD|Dandan Yang, Zhejiang Hikstor Technology Co. LTD|Guilin Chen, Zhejiang Hikstor Technology Co. LTD|Hao Zhou, Zhejiang Hikstor Technology Co. LTD|Yihui Sun, Zhejiang Hikstor Technology Co. LTD|Zejie Zheng, Zhejiang Hikstor Technology Co. LTD|Qijun Guo, Zhejiang Hikstor Technology Co. LTD|Qiang Dai, Zhejiang Hikstor Technology Co. LTD|Fantao Meng, Zhejiang Hikstor Technology Co. LTD|Shikun He, Zhejiang Hikstor Technology Co. LTD

We present a novel channel-less SOT-MTJ device featuring a self-aligned SOT channel integrated simultaneously with the MTJ etch. The device exhibits high performance, showing 2ns switching, 10^{-6}write-error-rate, >10^{12}endurance, and 16.5% current reduction. Achieving a record >99.9% yield, this channel-less SOT-MTJ design paves the way for high-performance SOT-MRAM.

03:40 PM
42-5 | Cryogenic In-Memory Computing Circuits with Giant Anomalous Hall Current in Magnetic Topological Insulators for Quantum Control, Kun Qian, Hong Kong University of Science and Technology|Albert Lee, InstonTech.|Zhihua Xiao, Hong Kong University of Science and Technology|Haoran He, University of California, Los Angeles|Shunkong Cheung, Hong Kong University of Science and Technology|Yuting Liu, Harbin Institute of Technology|Ferris Nugraha, Hong Kong University of Science and Technology|Qiming Shao, Hong Kong University of Science and Technology

Room-temperature AI for quantum control offers significant advantages over conventional methods but encounters challenges such as latency. Computing at cryogenic temperatures < 4.2 K is a promising yet elusive solution. Magnetic topological insulators (MTIs) are potential candidates as cryogenic memristors due to electrical-tunable readout via anomalous Hall effect (AHE). In previous Hall-based neuron network (NN) designs, signal-to-noise ratio of Hall voltage summation and read disturbance can lead to errors. For the first time, we propose and experimentally verify the multiply-and-accumulate operation of a transverse-read Hall-current based neural network. The MTI NN-model is accurate and efficient for the qubit state preparation.

04:05 PM
42-6 | Spin Devices for Nonvolatile Memories, Unconventional Computing, and Energy Harvesting (Invited), Hyunsoo Yang, National University of Singapore|Guoyi Shi, National University of Singapore|Yuchen Pu, National University of Singapore|Qu Yang, National University of Singapore|Yakun

Liu, National University of Singapore|Fei Wang,, National University of Singapore|Jia Si, National University of Singapore|Raghav Sharma, National University of Singapore

Spin torque magnetic random access memory is emerging as key enabling low-power technologies, which already spread over markets from embedded memories to the Internet of Things. In addition, spin torque devices can offer alternative solutions for unconventional computing and energy harvesting. We present our recent progresses in spin-orbit torque (SOT) devices, an experimental Ising computer based on magnetic tunnel junctions, and an energy harvesting system based on electrically connected multiple spin-torque oscillators (STOs).

38 | NC | Ferroelectrics and Beyond
1:30 PM – 4:55 PM, Grand Ballroom B
Co-Chairs: Catherine Graves, Google DeepMind and Thomas Kämpfe, Fraunhofer IPMS

In this session, we focus on ferroelectric technologies for compute-in-memory across a wide range of applications and integration concepts. The first paper shows an impressive multilevel (256 level) 3D-FeNAND and compares storage density, throughput and energy between 2D and 3D for multiply-accumulate operations. Next, we see very promising device characteristics of high endurance and density in antiferroelectric FETs (AFeFET) based on IGZO-channels for compute-in-memory. The third paper is our invited talk reviewing the tradeoffs between energy, model accuracy, and security across different NVM technologies (RRAM, FeFET, and MRAM). The fourth paper shows a BEOL-integrated stacked FeFET to enable pairwise coupling in various Ising problems. Next, we have a paper showing charge-trap FeFET devices to emulate short and long term memory for dynamic object trajectory prediction. The sixth paper demonstrates a ferroelectric capacitive (Fe-cap) memory array, exploring resonant adiabatic writes and multiply-accumulates for lower energy operation. Finally, our last paper proposes a FE-latch-based tunable RNG for random step probabilities when solving optimization problems with FeMFET devices.

01:30 PM
38-0 | Welcome

01:35 PM
38-1 | Analog Computation in Ultra-High Density 3D FeNAND for TB-level Hyperscale AI Models,
Jae-Gil Lee, SK hynix Inc.|Won-Tae Koo, SK hynix Inc.|Geonhui Lee, SK hynix Inc.|Jihun Kim, SK hynix Inc.|Woocheol Lee, SK hynix Inc.|Hyung Dong Lee, SK hynix Inc.|Sunghyun Yoon, SK hynix Inc.|Sung-In Hong, SK hynix Inc.|In-Ku Kang, SK hynix Inc.|Joongsik Kim, SK hynix Inc.|Hyejung Choi, SK hynix Inc.|Soo Gil Kim, SK hynix Inc.|Seho Lee, SK hynix Inc.|Jaeyun Yi, SK hynix Inc.|Seon Yong Cha, SK hynix Inc.

For the first time, we demonstrated the ultra-high density 3D ferroelectric NAND (FeNAND) arrays for analog computation of hyperscale AI models. Interface trap density of gate stacks was controlled to induce multi-level weight conductance states (≥ 256 levels/cell) of 3D FeNAND cells. Then, we confirmed the high accuracy (87.8%) of analog multiply–accumulate operations in 3D FeNAND arrays. Our 3D FeNAND arrays improved A-CiM cell density by a factor of 4,000x than 2D arrays, thereby they can provide 1,000x higher compute efficiency (TOPS/mm^2).

02:00 PM

38-2 | First demonstration of AFeFET Based Capacitor-Less eDRAM Computing-in-Memory Featuring 4.84 Mb/mm2 High Memory Density, 105 s Long Retention Time, and >1010 High Endurance, Hongtao Zhong, Tsinghua University|Zijie Zheng, National University of Singapore|Leming Jiao, National University of Singapore|Zuopu Zhou, National University of Singapore|Chen Sun, National University of Singapore|Wenjun Tang, Tsinghua University|Zhonghao Chen, Tsinghua University|Yuye Kang, National University of Singapore|Kaizhen Han, National University of Singapore|Vijaykrishnan Narayanan, Pennsylvania State University|Huazhong Yang, Tsinghua University|Thomas Kämpfe, Fraunhofer IPMS|Kai Ni, University of Notre Dame|Xiao Gong, National University of Singapore|Xueqing Li, Tsinghua University

This paper, for the first time, reports the AFeFET based capacitor-less eDRAM Computing-in-Memory (CiM) The highlights include: (i) First fabricated AFeFET-based CiM cell, i.e., 1T1AF eDRAM cell, with Amorphous-Indium-Gallium-Zinc-Oxide (a-IGZO) channel length (L_{CH}) of 25 nm; (ii) Proposed Almost-Refresh-Free (ARF) operation using the positive hysteresis window of AFeFETs with much longer retention time; (iii) Cluster design with locally shared computing units; (iv) High measured endurance over 10^{10} cycles for AFeFETs. Results show that the proposed 1T1AF eDRAM CiM achieves high memory/compute density,ultra-long retention time, and a high Cifar-10 accuracy, showing great potential for dense and robust eDRAM CiM designs.

02:25 PM
38-3 | The Energy-Accuracy-Security Trade-off in Resistive In-memory Architectures (Invited), Naresh Shanbhag, University of Illinois at Urbana-Champaign|Saion Roy, University of Illinois at Urbana-Champaign

This is the first work to experimentally characterize the fundamental energy-accuracy-security trade-off in embedded non-volatile memory (eNVM)-based in-memory computing (IMC) architectures. The intrinsically low compute accuracy of eNVM-based IMCs compromises its compute energy and density but offers potential resilience against security attacks. This paper overviews key factors affecting compute accuracy, experimentally characterizes the energy-

03:15 PM
38-4 | Towards 3D CMOS+X Ising Machines: Addressing the Connectivity Problem with Back-end-of-line FeFETs, Tanvir Haider Pantha, The University of Texas at Dallas|Abhishek Khanna, Micron Technology|Huacheng Ye, Western Digital Corporation|Shaila Niazi, University of California, Santa Barbara|Biswadeep Chakraborty, Georgia Institute of Technology|Ethan G Weinstock, Georgia Institute of Technology|Nithin Babu, Georgia Institute of Technology|Saibal Mukhopadhyay, Georgia Institute of Technology|Suman Datta, Georgia Institute of Technology|Kerem Çamsari, University of California, Santa Barbara|Sourav Dutta, The University of Texas at Dallas

Many real-world problems require high connectivity, which lie beyond the scope of today's CMOS-based Ising machine hardware. We address the connectivity bottleneck by using programmable BEOL FeFETs. We experimentally demonstrate, for the first time, 10 node, 24 coupling Ising Machine. Each coupling is realized using four dual-gated BEOL FeFETs supporting positive, negative and 3-bit weighted connections. We experimentally demonstrate the computing capability across three tasks: (a) combinatorial optimization problem of finding ground state Ising spin configuration with sparse, dense, spin glass and weighted

connection topology, (b) fast Boltzmann sampling for generating equilibrium samples and (c) energy-based learning for image reconstruction.

03:40 PM

38-5 | Experimental Demonstration of A CT-FeFET Array with Intrinsic Long-Short-Term Plasticity for Low-Cost Trajectory Prediction, Chao Li, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University, Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences|Jie Yu, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University|Xumeng Zhang, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University|Zhaohao Zhang, Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences|Fangduo Zhu, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University|Siyuan Ouyang, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University|Pei Chen, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University|Lingli Cheng, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University|Gaobo Xu, Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences|Qingzhu Zhang, Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences|Huaxiang Yin, Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences|Qi Liu, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University, Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences|Ming Liu, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University, Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences

Anticipative tracking is a vital function in the auto-driving field, supported by long short-term memory networks. Static IMC technology accelerates the computing of long-term parameters, while the operation of short-term parameters poses great buffer overhead. Inspired by the fused long short-term synaptic plasticity in biology, here, we proposed a dynamic IMC strategy based on a charge-trapping FeFET array with intrinsic long short-term plasticity. We further demonstrated a dynamic IMC neuromorphic system based on such an array for performing anticipative autonomous driving tracking, achieving more than 1000× and 4× improvements than GPU in power consumption and memory overhead.

04:05 PM

38-6 | Experimental Demonstration of Resonant Adiabatic Writing and Computing in Ferroelectric Capacitive Memory Array for Energy-Efficient Edge AI, Jin Luo, Peking University|Bingrui Song, Peking University|Yuxin Lin, Peking University|Zhiyuan Fu, Peking University|Boyi Fu, Peking University|Weikai Xu, Peking University|Linxiao Shen, Peking University|Yuan Wang, Peking University|Qianqian Huang, Peking University|Ru Huang, Peking University

This work reports the first experimental demonstration of resonant adiabatic writing and computing for C-CIM based on 3D-stackable FeCap array, enabling significantly reduced dynamic power consumption and resistive dissipation for weight update and MAC operation. Further co-optimizing the proposd design with layer-wise normalization algorithm, high-accuracy pattern recognition is demonstrated with record-high energy efficiency, highlighting its great potential for edge AI application.

04:30 PM
38-7 | Novel Ferroelectric-based Ising Machine Featuring Reconfigurable Arbitrary Ising Graph and Controllable Annealing through Device-Algorithm Co-Optimization, Weikai Xu, Peking University|Jin Luo, Peking University|Zhiyuan Fu, Peking University|Runze Han, Peking University|Shengyu Bao, Peking University|Kaifeng Wang, Peking University|Qianqian Huang, Peking University|Ru Huang, Peking University

This work proposed a FE-based Ising machine (FE-Ising) through device-algorithm co-optimization. For the Ising topology, a novel interaction (*J*)-centric topology is proposed, which enables reconfigurable arbitrary Ising graph. For hardware implementation of *J*-centric FE-Ising, a compact *J* unit composed of n-type and p-type 1T1C FeFET is further proposed and experimentally demonstrated with robust device reliability and small variability. Moreover, for spin (σ) update and controllable annealing, the novel FE-based programmable inverter and tunable RNG are also proposed and experimentally presented. Based on the FE-Ising, the solving processes of max-cut problem are demonstrated with significantly enhanced speed, success probability, and energy-efficiency.

40 | PMA | Device Physics in Wide-Bandgap Power Devices
1:30 PM – 5:20 PM, Continental 4
Co-Chairs: Ho-Young Cha, Hongik University and Takuya Maeda, The University of Tokyo

This session includes 8 papers that describe fundamental device physics in WBG semicondcutor power devices. The first 4 papers describe the physics in WBG semiconductor MOSFETs. The first paper, by Kenji Ito from Toyoto Central R&D Labs., Inc., reports the high channel mobility and stable E-mode operation in AlSiO/AlN/m-plane p-GaN MOSFETs. The 2nd paper, by Zaitian Han from University of Science and Technology of China, reports the channel mobility of 205 cm2/Vs in a 1.4 kV vertical GaN-on-GaN MISFET. The 3rd paper, by Tsurugi Kondo from Fuji Electric Co. Ltd., reports drastic enhancement of mobility in GaN MOSFETs with a graded AlGaN buried-channel. The 4th paper, by Xilun Chi from Kyoto Univeristy, reports the unique electron trapping and its impacts on electron mobility in SiC MOSFETs. The 5th paper, by Xinyi Wen from Stanford University, reports wrap-around gate, normally-off, dispersion-free GaN CAVETs. The 6th paper, by Sirui Feng from Hong Kong Univerity of Science and Technology, reports an all-GaN semiconducting-gate HEMT for inherent gate-level high-voltage protection and synchronous switching. The 7th paper, Dr. Xin Yang from Virginia Tech, reports the characterization of Si, SiC and GaN power devices at deep cryogenic temperature down to 0.1 K. The final paper is the invited talk, by Christian Koller, reports on catalyzing innovation: bridging system efficiency to fundamental device physics in GaN power devices.

01:30 PM
40-0 | Welcome

01:35 PM
40-1 | High channel mobililty and stable E-mode operation in AlSiO/AlN/m-plane p-type GaN MOSFETs with little temperature dependence of the threshold voltage, Kenji Ito, Toyota Central R&D Lab., Inc.|Tetsuo Narita, Toyota Central R&D Lab., Inc.|Masakazu Kanechika, Nagoya University|Hiroko Iguchi, Toyota Central R&D Lab., Inc.|Shiro Iwasaki, Toyota Central R&D Lab., Inc.|Daigo Kikuta, Toyota

Central R&D Lab., Inc.|Emi Kano, Nagoya University|Nobuyuki Ikarashi, Nagoya University|Kazuyoshi Tomita, Nagoya University|Jun Suda, Nagoya University|Tetsuo Kachi, Nagoya University

The trench-gate MOSFET having a AlSiO/AlN/*p*-type GaN gate structure is systematically compared to the planer MOSFET. The *m*-plane channel exhibits the effective mobility over 180 $cm^2V^{-1}s^{-1}$and demonstrates the advantage of the stable enhancement-mode operation with little temperature dependence by eliminating the polarization and the pyroelectric effects.

02:00 PM
40-2 | Achieving 205 cm2 V-1s-1 Inversion Channel Mobility in 1.4 kV Vertical GaN-on-GaN MISFET With Nitride Gate Dielectric, Shu Yang, University of Science & Technology of China, University of Science & Technology of China
Speakers: Zaitian Han, University of Science & Technology of China

A vertical GaN trench MISFET with an inversion channel mobility of ~205 cm^2 $V^{-1}s^{-1}$ was realized. The channel mobility was improved by introducing AlN to reduce the interface state density and Coulomb scattering. The device showed a current density of 1200 A/cm^2 and achieved a withstand voltage of ~1440 V by modulating the p-body region doping concentration.

02:25 PM
40-3 | Drastic Mobility Enhancement of GaN MOSFETs with Graded AlGaN Buried-Channel Formed by Aluminum Thermal Diffusion, Tsurugi Kondo, Fuji Electric Co., Ltd.|Katsunori Ueno, Fuji Electric Co., Ltd.|Ryo Tanaka, Fuji Electric Co., Ltd.|Takuro Inamoto, Fuji Electric Co., Ltd.|Shinya Takashima, Fuji Electric Co., Ltd.

We demonstrate the drastic mobility enhancement of GaN MOSFETs with graded AlGaN buried-channel formed by aluminum thermal diffusion.Effective channel mobility for the MOSFETs reached 80% of the bulk mobility of GaN at 175 °C.This study shows the possibility of realizing GaN-based power MOSFETs with a low on-resistance.

02:50 PM
40-4 | Unique electron trapping and its impacts on electron mobility in SiC n-channel MOSFETs, Xilun Chi, Kyoto University|Koji Ito, Kyoto University|Takeru Suto, Hitachi, Ltd. R&D Group|Akio Shima, Hitachi, Ltd. R&D Group|Mitsuaki Kaneko, Kyoto University|Tsunenobu Kimoto, Kyoto University

The electron trapping and scattering mechanisms in SiC MOSFETs remain unknown due to the lack of a comprehensive understanding of the interface defects. In this study, we clarified that the majority of the interface defects exist not at the exact interface but in the SiC side (a few nm from the interface) of the MOS system by several different approaches.By considering electron trapping and scattering caused by these interface defects, we developed the first set of physics-based models that can explain both the experimental Hallmobilities and gate characteristics of SiC MOSFETs across a wide range of temperature.

03:40 PM
40-5 | Wrap-Around Gate delivering 600V/1.0 mΩ·cm², Normally-Off, Dispersion-Free CAVETs with Record-High Gate Swing, Xinyi Wen, Stanford University|Hayao Kasai, Stanford University, Research Institute for Advanced Material and Devices, Corporate R&D Group, Kyocera|Koukichi Fujita, Research

Institute for Advanced Material and Devices, Corporate R&D Group, Kyocera|Tsuyoshi Yamasaki , Research Institute for Advanced Material and Devices, Corporate R&D Group, Kyocera|Tatsuro Sawada, Research Institute for Advanced Material and Devices, Corporate R&D Group, Kyocera| Maliha Noshin, Stanford University|Chuanzhe Meng, Stanford University|Srabanti Chowdhury, Stanford University

A normally-off vertical GaN-on-GaN trench-CAVET with wrap-around gate (WG-CAVET) was demonstrated, offering a large V_{TH} of 6.5V and record high gate swing of 40 V to prevent faulty turn-on and ensure compatibility with gate-driver designs. MIS gate wrapped-around the 2DEG channel three-dimensionally through a periodic-groove-structure, enhancing gate controllability and mitigating dispersion by acting as a field plate. WG-CAVET achieved high current of 4.8kA/cm^2, low $R_{ON,SP}$ of 1.0mΩ·cm^2, and 600V breakdown using a 5-μm-thick drift layer. No dispersion was observed. Dynamic $R_{ON}$was only 1.11, much smaller compared to the lateral counterpart. large-area multi-gate-finger WG-CAVET was scaled for Ampere-level high-current operations.

04:05 PM
40-6 | An All-GaN Semiconducting-Gate HEMT for Inherent Gate-Level High-Voltage Protection and Synchronous Switching with Photoelectrically Enhanced Conductivity, Haochen Zhang, The Hong Kong University of Science and Technology|Sirui Feng, The Hong Kong University of Science and Technology|Tao Chen, The Hong Kong University of Science and Technology|Li Zhang, The Hong Kong University of Science and Technology|Wenjie Song, The Hong Kong University of Science and Technology |Song Yang, The Hong Kong University of Science and Technology |Yutao Geng, The Hong Kong University of Science and Technology|Zheyang Zheng, The Hong Kong University of Science and Technology|Kevin Chen, The Hong Kong University of Science and Technology

We demonstrate a normally-off n-GaN/p-GaN/AlGaN/GaN HEMT with an n-GaN semiconducting gate (SG) overlaying 2DEG channel as intrinsic gate (IG) and connected to extrinsic electrode (XG) outside active region. SG is fully depleted at on-state and decouples IG from further increase in XG's voltage. Therefore, SG-HEMT can tolerate extremely high-voltage external gate transients (500-μs 1.5 kV). Moreover, SG allows a peripheral 340-nm LED to create excessive holes in IG, leading to higher 2DEG density and enhanced conductivity (42.6%-reduced on-resistance). With the LED driven synchronously with the gate-drive signal, the proposed SG-HEMT exhibits quick turn-off transients and immaterial changes to OFF-state characteristics.

04:30 PM
40-7 | First Characterization of Si, SiC and GaN Power Deivces at Deep Cryogenic Temperatures down to 0.1 K, Xin Yang, Virginia Tech|Matthew Porter, Virginia Tech|Zineng Yang, Virginia Tech|Zichen Xi, Virginia Tech|Qiang Li, Virginia Tech|Linbo Shao, Virginia Tech|Yuhao Zhang, Virginia Tech

We characterize the static and dynamic switching performance of Si, SiC and GaN power devices at deep cryogenic temperatures down to 0.1 K for the first time. This characterization is enabled by employing a dilution refrigerator, which is an advanced tool for quantum research, connected with a custom circuit setup. All three devices largely retain breakdown voltage and can perform hard switching at 0.1 K, but they exhibit very different conduction and switching characteristics. The new physics behind are also unveiled. These breakthrough results open the door for developing deep cryogenic power electronics for quantum, healthcare, and space applications.

04:55 PM
40-8 | Catalyzing Innovation: Bridging System Efficiency to Fundamental Device Physics (Invited), Christian Koller, Infineon|Matthias Kasper, Infineon|Boris Butej, KAI GmbH|Dominik Wieland, Infineon|Borja Alberdi, Infineon|Oliver Haeberlen, Infineon|Clemens Ostermaier, Infineon

We demonstrate two GaN-HEMT applications from system-level point of view and the benefit of employing GaN. We further discuss reliability concerns in GaN and shine light into the dynamic saturation current. Finally, we show recent developments in understanding the device physics during operation in terms of on-resistance degradation and hard-failure.

41 | ODI | Advanced Image Sensors
1:30 PM – 5:20 PM, Continental 6
Co-Chairs: Frederic Lalanne, ST Microelectronics and Kazuko Nishimura, Panasonic Holdings Corporation

This session includes 6 papers on latest image sensor technologies developments. To be noticed this year the multiple ways of stacking layer with new features. The first stack involves a dedicated AI image processing layer based on neural networks for a 50 Mpix sensor. The second one shows progress on small pixel noise with 2-layer pixel and additional intermediate interconnection. Third stack, very innovative with organic pixel on top of conventional Si based ITOF pixel for true single device RGB-Z sensor. All three papers are authored by Sony Semiconductors. InAs QD image sensors are also reported for the first time as a lead-free option for SWIR imaging by both IMEC and Sony Semiconductors Also progress in conventional IR global shutter with newly nitrated MIM capacitor and optimized DTI filling for crosstalk and QE improvement is presented by Samsung semiconductor.

01:30 PM
41-0 | Welcome

01:35 PM
41-1 | A Novel 1/1.3-inch 50 Megapixel Three-wafer-stacked CMOS Image Sensor with DNN Circuit for Edge Processing, Ryoichi Nakamura, Sony Semiconductor Solutions Corp|Hidenobu Tsugawa, Sony Semiconductor Solutions Corp|Hajime Yamagishi, Sony Semiconductor Solutions Corp|Yutaro Fujisaki, Sony Semiconductor Solutions Corp|Yosuke Suda, Sony Semiconductor Solutions Corp|Yukihiro Tatsumi, Sony Semiconductor Solutions Corp|Kan Shimizu, Sony Semiconductor Solutions Corp|Yoshihisa Kagawa, Sony Semiconductor Solutions Corp|Kenta Ono, Sony Semiconductor Solutions Corp|Yosuke Horie, Sony Semiconductor Solutions Corp|Ryoji Koganei, Sony Semiconductor Solutions Corp|Hiroshi Nakano, Sony Semiconductor Solutions Corp|Kazumi Kobayashi, Sony Semiconductor Solutions Corp|Takumi Kamibayashi, Sony Semiconductor Solutions Corp|Nobutatsu Araki, Sony Semiconductor Manufacturing Corp|Kenichi Saito, Sony Semiconductor Manufacturing Corp|Ryoma Suzue, Sony Semiconductor Manufacturing Corp|Wataru Otsuka, Sony Semiconductor Solutions Corp|Hayato Iwamoto, Sony Semiconductor Solutions Corp

This study reports the first ever 3-wafer-stacked CMOS image sensor with DNN circuit. The sensor was fabricated using wafer-on-wafer-on-wafer process and DNN circuit was placed on the bottom wafer to ensure heat dissipation. This device can incorporate the HDR function and enlarge the pixel array area to remarkably improve image-recognition.

02:00 PM

41-2 | Low Dark Noise and 8.5k e− Full Well Capacity in a 2-Layer Transistor Stacked 0.8µm Dual Pixel CIS with Intermediate Poly-Si Wiring, Yosuke Satake, Sony Semiconductor Solutions Corporation|Yusuke Tanaka, Sony Semiconductor Solutions Corporation|Shinya Sato, Sony Semiconductor Solutions Corporation|Masayuki Takase, Sony Semiconductor Solutions Corporation|Mizuki Hoyano, Sony Semiconductor Solutions Corporation|Shuhei Kasukawa, Sony Semiconductor Solutions Corporation|Manabu Tomita, Sony Semiconductor Solutions Corporation|Yoshiaki Kikuchi, Sony Semiconductor Solutions Corporation|Junpei Yamamoto, Sony Semiconductor Manufacturing Corporation|Kai Tokuhiro, Sony Semiconductor Manufacturing Corporation|Kazuya Furumoto, Sony Semiconductor Manufacturing Corporation|Hikari Sugino, Sony Semiconductor Manufacturing Corporation|Yusuke Murakawa, Sony Semiconductor Manufacturing Corporation|Soichiro Yamazaki, Sony Semiconductor Manufacturing Corporation|Hiroshi Mizuno, Sony Semiconductor Manufacturing Corporation|Hiroshi Tomita, Sony Semiconductor Manufacturing Corporation|Noriteru Yamada, Sony Semiconductor Manufacturing Corporation|Tomoyuki Hirano, Sony Semiconductor Solutions Corporation|Yoshiaki Kitano, Sony Semiconductor Solutions Corporation

This paper demonstrates a 2-layer transistor pixel stacked CMOS image sensor with the world's smallest 0.8µm dual pixel. We improved the layout flexibility with intermediate poly-Si wiring technique. Our advanced 2-layer pixel device achieved low input-referred random noise of 1.3 e^-rms and high full well capacity of 8.5k e^-.

02:25 PM

41-3 | A High-Performance 2.2µm 1-Layer Pixel Global Shutter CMOS Image Sensor for Near-Infrared Applications, Tae-Min Kim, Samsung Electronics|Jungsan Kim, Samsung Electronics|Seungho Lee, Samsung Electronics|Yongsoon Park, Samsung Electronics|Jong Uk Kim, Samsung Electronics|Sangjin Choi, Samsung Electronics|Hyoeun Kim, Samsung Electronics|SeungKuk Kang, Samsung Electronics|Sang Hoon Song, Samsung Electronics|Hoonil Yang, Samsung Electronics|Somin Park, Samsung Electronics|Taehyoung Kim, Samsung Electronics|Yoonjay Han, Samsung Electronics|Suji Hwang, Samsung Electronics|Tae-Yon Lee, Samsung Electronics|Hongki Kim, Samsung Electronics|Seung-Sik Kim, Samsung Electronics|Heesung Shim, Samsung Electronics|Jonghyun Go, Samsung Electronics|Jae-Kyu Lee, Samsung Electronics|Chang-Rok Moon, Samsung Electronics|Jaihyuk Song, Samsung Electronics

A high performance and low cost 2.2µm 1-layer pixel near infrared (NIR) global shutter (G/S) CMOS image sensor (CIS) was demonstrated. In order to improve quantum efficiency (QE), thick silicon with high aspect ratio full-depth deep trench isolation (FDTI) and backside scattering technology are implemented. Furthermore, thicker sidewall oxide for deep trench isolation and oxide filled FDTI were applied to enhance a modulation transfer function (MTF). In addition, 3-dimensional metal-insulator-metal capacitors were introduced to suppress temporal noise (TN). As a result, we have demonstrated industry-leading NIR G/S CIS with 2.71e^- TN, dark current of 8.8e^-/s, 42% QE and 58% MTF.

03:15 PM

41-4 | First Demonstration of 2.5D Out-of-Plane-Based Hybrid Stacked Super-Bionic Compound Eye CMOS Chip with Broadband (300-1600 nm) and Wide-Angle (170°) Photodetection, Yunfei Xie, zhejiang university|Yang Xu, zhejiang university|Xiaochen Wang, zhejiang university|Jing He, Westlake University|zhixiang zhang, zhejiang university|Hao Ning, zhejiang university|Srikrishna Chanakya

Bodepudi, zhejiang university|Jiye Li, Westlake University|Zongwen Li, zhejiang university|QianQian Zhang, zhejiang university|Yance Chen, zhejiang university|Zijian Pan, zhejiang university|Yuan Ma, zhejiang university|Yue Dai, zhejiang university|Jian Chai, zhejiang university|Muhammad Abid Anwar, zhejiang university|Bin Yu, zhejiang university|Liaoyong Wen, Westlake University|Yongliang Xie, zhejiang university|Youshui He, zhejiang university|Jiangming Lin, zhejiang university

We propose a hybrid stacked CMOS bionic chip. The surface employs a fabrication process involving binary-pore anodic aluminum oxide (AAO) templates and integrates monolayer graphene (Gr) to mimic the compound eyes, thereby enhancing detection capabilities in the ultraviolet and visible ranges. Utilizing a 2.5D out-of-plane architecture, it achieves a wide-angle detection effect (170°) equivalent to curved surfaces while enhancing absorption in the 1550 nm communication band to nearly 100%. Additionally, through-silicon via (TSV) technology is integrated for wafer-level fabrication, and a CMOS 0.18-μm integrated readout circuit is developed, achieving the super-bionic compound eye chip based on hybrid stacked integration.

03:40 PM

41-5 | Pseudo-direct LiDAR by deep-learning-assisted high-speed multi-tap charge modulators (Invited), Keiichiro Kagawa, Shizuoka University|Keita Yasutomi, Shizuoka University|Michitaka Yoshida, Japan Society for the Promotion of Science|Daisuke Hayashi, Shizuoka University|De Xing Lioe, Shizuoka University|Shoji Kawahito, Shizuoka University|Hajime Nagahara, Osaka University

A virtually direct LiDAR system based on an indirect ToF image sensor and charge-domain temporal compressive sensing combined with deep learning is demonstrated. This scheme has high spatio-temporal sampling efficiency and offers advantages such as high pixel count, high photon-rate tolerance, immunity to multipath interference, constant power consumption regardless of incident photon rates, and motion artifact-free. The importance of increasing the number of taps of the charge modulator is suggested by simulation.

04:05 PM

41-6 | A Color Image Sensor Using 1.0-μm Organic Photoconductive Film Pixels Stacked on 4.0-μm Si Pixels for Near-Infrared Time-of-Flight Depth Sensing, Tomohiro Ohkubo, Sony Semiconductor Solutions Corporation|Nobuhiro Kawai, Sony Semiconductor Solutions Corporation|Kimiyasu Shiina, Sony Semiconductor Solutions Corporation|Kei Fukuhara, Sony Semiconductor Solutions Corporation|Ryotaro Takaguchi, Sony Semiconductor Solutions Corporation|Tetsuro Takada, Sony Semiconductor Solutions Corporation|Yoshito Nagashima, Sony Semiconductor Manufacturing Corporation|Takahito Niwa, Sony Semiconductor Manufacturing Corporation|Masahiro Joei, Sony Semiconductor Solutions Corporation|Kensaku Maeda, Sony Semiconductor Solutions Corporation|Tomoyuki Hirano, Sony Semiconductor Solutions Corporation|Atsushi Suzuki, Sony Semiconductor Solutions Corporation|Hideaki Togashi, Sony Semiconductor Solutions Corporation|Tetsuji Yamaguchi, Sony Semiconductor Solutions Corporation|Yusuke Oike, Sony Semiconductor Solutions Corporation

We have developed an image sensor capable to simultaneously acquire high-resolution RGB images with good color reproduction and parallax-free ranging information by 1.0-μm organic photoconductive film RGB pixels stacked on 4.0-μm NIR silicon pixels for iToF depth sensing.

04:30 PM

41-7 | Pb-free Colloidal InAs Quantum Dot Image Sensor for Infrared, Osamu Enoki, Sony Semiconductor Solutions Corporation|Hiroshi Kato, Sony Semiconductor Solutions Corporation|Yuta Okabe, Sony Semiconductor Solutions Corporation|Shuichi Takizawa, Sony Semiconductor Solutions Corporation|Tomonari Nakada, Sony Semiconductor Solutions Corporation|Yusuke Moriya, Sony Semiconductor Solutions Corporation|Kensaku Maeda, Sony Semiconductor Solutions Corporation|Hayato Iwamoto, Sony Semiconductor Solutions Corporation

We developed an image sensor using colloidal InAs quantum dot (QD) for photoconversion. After spincoating the QDs on a wafer and standard semiconductor processing, the sensor exhibited infrared sensitivity and imaging capability. This approach facilitates easier production of lead-free infrared sensors for consumer use.

04:55 PM
41-8 | Lead-Free Quantum Dot Photodiodes for Next Generation Short Wave Infrared Optical Sensors, Stefano Guerrieri, ams OSRAM|Wenya Song, imec|Zeger Hens, Ghent University|Valeriia Grigel, QustomDot|Roelof Steeno, ChemStream|Jing Bai, Ghent University|Yuhao Deng, Ghent University|Ezat Kheradmand, Ghent University|Jaqueline de Oliveira Rocha, Ghent University|Igor Nakonechnyi, QustomDot|Willem Walravens, QustomDot|Isabel Pintor Monroy, imec|Itai Lieberman, imec|Arman Uz Zaman, imec|JooHyoung Kim, imec|Tristan Weydts, imec|Marina Vildanova, imec|Pawel Malinowski, imec

Colloidal quantum dot sensors are disruptingimaging beyond the spectral limits of silicon. In this paper,we present imagers based on InAs QDs as alternative for 1stgeneration Pb-based stacks. New synthesis method yields 9nm QDs optimized for 1400 nm and solution-phase ligandexchange results in uniform 1-step coating. Initial EQE is17.4% at 1390 nm on glass and 5.8% EQE on silicon(detectivity of 7.4 × 109 Jones). Using metal-oxide transportlayers and >300 hour air-stability enable compatibility withfab manufacturing. These results are a starting point towardsthe 2nd generation quantum dot SWIR imagers.

Coffee Break
2:50 PM – 3:40 PM
East Lounge

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