Tutorial 2: Advanced Packaging Technologies for Heterogeneous Integration

Speaker: Ravi Mahajan and Sairam Agraharam (Intel)

Abstract:

Advanced packaging technologies are critical enablers of Heterogeneous Integration (HI) because of their importance as compact, power efficient platforms. This tutorial will start by describing the role of advanced packaging in the overall HI landscape using the HI roadmap as a reference. The tutorial will then describe the key physical and performance attributes of advanced packaging architectures and describe their evolution. Different packaging architectures will be compared primarily on the basis of their physical interconnect capabilities. Key features in leading edge 2D and 3D technologies, such as EMIB, Silicon Interposer, Foveros and Co-EMIB will be described and a roadmap for their evolution will be presented. This will be followed by a high-level discussion of Assembly and Test flows. Challenges and opportunities in developing advanced package architectures will be discussed. The scope of the discussion will include design for performance (i.e. ensuring efficient power delivery, high-speed signaling and thermal management), thermo-mechanical robustness, manufacturing considerations, materials and reliability. Reference will also be made to key enabling fields such as modeling, metrologies and equipment. The tutorial will conclude with a discussion of overall opportunities and challenges in driving the advanced package roadmap forward.

Speaker's Bio:

Ravi Mahajan is an Intel Fellow responsible for Assembly and Packaging Technology Pathfinding for future silicon nodes. Ravi joined Intel in 1992 after earning Ph.D. in Mechanical Engineering from Lehigh University. He holds the original patents for silicon bridges that became the foundation for Intel's EMIB technology. His early insights have also led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques used for thermo-mechanical stress model validation. His contributions during his Intel career have earned him numerous industry honors, including the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 "Outstanding Service and Leadership to the IEEE" Awards from IEEE Phoenix Section & Region 6 and most recently the 2020 Richard Chu ITherm Award For Excellence. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. He has been long associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was named Intel Fellow in 2017.

Sairam Agraharam is a Senior Principal Engineer responsible for developing and enabling successful die package integration with high yield/reliability, new first level interconnect schemes/pitch scaling, and novel heterogeneous package architectures/process flows for Intel products. Through his nearly two decade long career, Sai has been instrumental in the successful resolution of many chip-package design, materials, process and reliability interactions with Cu bump based first level interconnect and low-K dielectrics, resulting in successful deployment of scaled packaging technologies. He led the teams that enabled Intel's first lead-free / halogen free packages and successfully integrated Intel's first thick metal passivation architecture. He played a pivotal role in the development and successful implementation of novel heterogeneous package architectures such as EMIB and Foveros in Intel products and continues to take leadership roles as a technologist for future scaling. Sairam joined Intel in 2000 after receiving his Ph. D in Chemical engineering from Georgia Institute of technology. He has 20 patents spanning the areas of die-package ILD stress reduction, novel packages and package interconnect architectures.