2020 IEDM Technical Program

Session 1 - Plenary 1: Monday, 8:00 a.m.
Future Logic Scaling: Towards Atomic Channels and Deconstructed Chips, S. B. Samavedam, imec

Session 2: Advanced Logic Technology - High-mobility Channel devices
Monday, December 14, 9:30 a.m. - 10:20 a.m.
Anabela Veloso, Imec
Yao-Jen Lee, TSRI

9:30 a.m.
2.1 Toward high-performance and reliable Ge channel devices for 2 nm node and beyond (Invited), Hiroaki Arimura, Elena Capogreco, Anurag Vohra, Clement Porret, Roger Loo, Erik Rosseel, Andriy Hikavyy, Daire Cott, Guillaume Boccardi, Liesbeth Witters, Geert Eneman, Jerome Mitard, Nadine Collaert, Naoto Horiguchi, imec

This paper describes our recent research progress on high-mobility Ge-channel n/pFETs. We will show the improved device performance and reliability of Ge fin and gate-all-around nanowire FETs through the optimization of key challenging modules such as gate stack, junction and contact.

9:40 a.m.
2.2 Gate-All-Around Strained $Si_{0.4}Ge_{0.6}$ Nanosheet PMOS on Strain Relaxed Buffer for High Performance Low Power Logic Application, Ashish Agrawal, Siddharth Chouksey, Willy Rachmady, Suresh Vishwanath, Susmita Ghose, Manan Mehta, Jessica Torres, Adedapo Oni, Xiao-Jun Weng, Han Li, Devin Merrill, Matthew Metz, Anand Murthy, Jack Kavalieros, Intel Corporation

Short channel High Performance, gate-all-around strained $Si_{0.4}Ge_{0.6}$ nanosheet PMOSFET with aggressively scaled dimensions is demonstrated. This result is obtained with the combination of novel Si-cap-free gate oxide with EOT=9.1A, record high hole mobility=450 cm^2/Vs, low R_{EXT}=150 Ω-μm. Record high I_{ON}=508 μA/μm at 100 nA/μm is demonstrated for L_G=25nm at V_{CC}=0.5V.

9:50 a.m.
2.3 Stacked Gate-All-Around Nanosheet pFET with Highly Compressive Strained $Si_{1-x}Ge_x$ Channel, Shogo Mochizuki, Maruf Bhuiyan, Huimei Zhou, Jingyun Zhang, Erin Stuckert, Juntao Li, Kai Zhao, Miaomiao Wang, Veeraraghavan Basker, Nicolas Loubet, Dechao Guo, Bala Haran, Huiming Bu, IBM Research

Stacked Gate-All-Around (GAA) nanosheet pFETs with compressively strained $Si_{1-x}Ge_x$ channel have been fabricated to explore their electrical benefits. The Si_{1-x}GexNS channel structure with high crystalline quality and 1GPa compressive stress has been realized for the first time.

10:00 a.m.
2.4 First Demonstration of Uniform 4-Stacked $Ge_{0.9}Sn_{0.1}$ Nanosheets with Record I_{ON} =73μA at V_{OV}=V_{DS}= -0.5V and Low Noise Using Double $Ge_{0.95}Sn_{0.05}$ Caps, Dry Etch, Low Channel Doping, and High S/D Doping, Yu-Shiang Huang, Chung-En Tsai, Chien-Te Tu, Jyun-Yan Chen, Hung-Yu Ye, Fang-Liang Lu, C. W. Liu, National Taiwan University

The 4-stacked $Ge_{0.9}Sn_{0.1}$ uniform nanosheets sandwiched by double $Ge_{0.95}Sn_{0.05}$ caps are realized by dry etching. The carriers separated from dielectrics reduce the scattering. Low GeSn doping (<1E17 cm^{-3}) and

heavily S/D doping (~2E21 cm^{-3}) improve the performance. The record I_{ON}=73uA per stack (910uA/um per channel footprint) at V_{OV}=V_{DS}=-0.5V is achieved among GeSn 3D FETs.

10:10 a.m.
2.5 Subband Engineering by Combination of Channel Thickness Scaling and (111) Surface Orientation in InAs-On-Insulator nMOSFETs, Kei Sumita, Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi, The Univerisity of Tokyo

A (111) surface orientation InAs channel combined with an ultra-thin-body structure is proposed to overcome the performance limitation of III-V nMOSFETs by utilizing L valley conduction. We experimentally demonstrate mobility enhancement by thinning (111) InAs-On-Insulator channels and clarify the inherent superiority of InAs channels from the viewpoint of interface traps.

Session 3: Emerging Device and Compute Technology - Emerging Devices for Extending Moore's Law
Monday, December 14, 9:30 a.m. - 10:30 a.m.
K. Nagashio, The University of Tokyo
Q. Liu, Chinese Academy of Sciences

9:30 a.m.
3.1 Sources of variability in scaled MoS_2 FETs, Quentin Smets, Devin Verreck, Yuanyuan Shi*, Goutham Arutchelvan*, Benjamin Groven, Xiangyu Wu*, Surajit Sutar, Sreetama Banerjee, Ankit Nalin Mehta*, Dennis Lin, Inge Asselberghs, Iuliana Radu, imec, KU Leuven

Through advances in growth, cleaning, and device fabrication, our scaled MoS2 FET flow has reached sufficient maturity to study variability. The scaling of σVT with device dimensions is found nearly on par with state-of-the-art Si finFETs. We identify second layer islands as a significant contributor to SS degradation and variability.

9:40 a.m.
3.2 Reliability of Ultrathin High-κ Dielectrics on Chemical-vapor Deposited 2D Semiconductors, Zhihao Yu, Hongkai Ning*, Chao-Ching Cheng**, Weisheng Li*, Lei Liu*, Wanqing Meng*, Zhongzhong Luo*, Taotao Li*, Songhua Cai*, Peng Wang*, Wen-Hao Chang***, Chao-Hsin Chien***, Yi Shi*, Yong Xu, Lain-Jong Li**, Xinran Wang*, Nanjing University of Posts and Telecommunications, *Nanjing University, **Taiwan Semiconductor Manufacturing Company (TSMC), ***National Chiao Tung University

This is the first work to report the high-κ dielectric reliability on MoS_2. By PTCDA crystal as an interface layer, we demonstrated excellent reliability of HfO_2/PTCDA gate stack, including E_{BD} over 8.9 MV/cm, E_{BD}^{10yrs} over 6.5 MV/cm and ultra-low BD rate, all of which show better reliability than HfO_2/Si.

9:50 a.m.
3.3 Pinning-Free Edge Contact Monolayer MoS_2 FET, Terry Hung, Shih-Yun Wang*, Chih-Piao Chuu, Yun-Yan Chung, Ang-Sheng Chou, Feng-Shew Huang*, Tac Chen, Ming-Yang Li, Chao-Ching Cheng, Jin Cai, Chao-Hsin Chien, Wen-Hao Chang*, H.-S. Philip Wong, Lain-Jong Li, Taiwan Semiconductor Manufacturing Company (TSMC), *National Chiao Tung University

Experiments in this work reveal that the fabrication processes for metal MoS_2 contact strongly affect the electrical characteristics such as Schottky barrier height. It is the in-situ 2D etching and metal deposition that we obtained Fermi-level pinning-free Ni-MoS_2 side contact transistor devices.

10:00 a.m.
3.4 Sub-1nm EOT WS_2-FET with I_{DS} > 600µA/µm at V_{DS}=1V and SS < 70mV/dec at L_G=40nm, Chin-Sheng Pang, Peng Wu, Joerg Appenzeller, Zhihong Chen, Purdue University

Statistics of sub-1nm EOT WS_2-FETs with different channel thicknesses were evaluated. A record-high on-state current > 600 (µA/µm) and ultra-low contact resistance of 500 (Ω*µm) were achieved at a much-scaled overdrive voltage. Excellent off-state behaviors including small threshold voltage variations, near-ideal subthreshold slope, and small drain-induced barrier lowering were realized.

10:10 a.m.
3.5 Sub-0.5 nm Interfacial Dielectric Enables Superior Electrostatics: 65 mV/dec Top-Gated Carbon Nanotube FETs at 15 nm Gate Length, Gregory Pitner, Zichen Zhang*, Qing Lin*, Sheng-Kai Su, Carlo Gilardi*, Chenghsuan Kuo*, Harshil Kashyap*, Theo Weiss*, Zouchangwan Yu*, Tzu-Ang Chao, Lain-Jong Li, Subhasish Mitra*, H.-S. Philip Wong*, Jin Cai, Andrew Kummel*, Prab Bandaru*, Matthias Passlack, TSMC, *University of California, San Diego, **Stanford University

For superior electrostatic control, carbon nanotubes (CNTs) with 0.35 nm interfacial dielectric (k=7.8) and 2.5 nm ALD dielectric (k=24) are demonstrated. Top-gated 15-nm gate length CNT FETs have 65 mV/dec sub-V_T slope and 20 mV/V DIBL. TCAD modeling projects 68 mV/dec for CNFET with 10 nm L_G and 250 CNT/µm.

10:20 a.m.
3.6 Dual gate synthetic WS_2 MOSFETs with 120µS/µm Gm 2.7µF/cm^2 capacitance and ambipolar channel, Dennis Lin, Xiangyu Wu, Daire Cott, Devin Verreck, Benjamin Groven, Stephanie Sergeant, Quentin Smets, Surajit Sutar, Inge Asselberghs, Iuliana Radu, imec

We have engineered dual-gate WS2 transistors with scaled top/back gate-stacks for advanced logic applications. With a 2ML WS_2 channel, it reaches 210µA/um Id and 2.7µF/cm^2 capacitance, with >10^8 Ion/off , 120µS/um Gm and a steep turn-on. This design enables us to explore EOT scaling, ambipolar I-V/C-V on CVD WS_2 channel.

Session 4: Modeling and Simulation - Ferroelectric switching dynamics and device applications
Monday, December 14, 9:30 a.m. - 10:30 a.m.
Asif I. Khan, Georgia Institute of Technology
Anne S. Verhulst, IMEC

9:30 a.m.
4.1 Multiscale Simulation of Ferroelectric Tunnel Junction Memory Enabled by van der Waals Heterojunction: Comparison to Experiment and Performance Projection, Ning Yang, Hungyu Chen*, Jiang-Bin Wu*, Tong Wu, Jun Cao**, Xi Ling**, Han Wang*, Jing Guo, University of Florida, *University of Southern California, Los Angeles, **Boston University

By combining multiscale simulations from atomistic ab initio to quantum transport device simulations with experimental studies, atomically thin van der Waals (vdW) heterojunctions are investigated for ferroelectric tunnel junction (FTJ) device application. The simulation results explain experimentally observed device characteristics, and project device performance potentials of vdW heterojunction FTJs.

9:40 a.m.
4.2 Ferroelectric Switching in FEFET:Physics of the Atomic Mechanism and Switching Dynamics in $HfZrO_x$, HfO_2 with Oxygen Vacancies and Si dopants, Sergiu Clima, Barry O'Sullivan, Nicolo

Ronchi, Marie Garcia Bardon, Kaustuv Banerjee, Geert Van den Bosch, Geoffrey Pourtois**, Jan Van Houdt*, imec, *and with University of Leuven, **and with University of Antwerp

We show that only Pbcm mechanism obeys the ferroelectric switching physics, whereas $P4_2/nmc$ mechanism does not, nevertheless it is an important antiferroelectric mechanism. Constraints relaxation leads to 90° polarization rotation/domain deactivation. Si/V_O-doped material switch faster than undoped $HfO_2/HfZrO_x$. Arrhenius model/intrinsic material switching overestimates the switching speed extracted from experiments.

9:50 a.m.
4.3 Ferroelectric Thickness Dependent Domain Interactions in FEFETs for Memory and Logic: A Phase-field Model based Analysis, Atanu Kumar Saha, Mengwei Si, Kai Ni*, Suman Datta**, Peide Ye, Sumeet Gupta, Purdue University, *Rochester Institute of Technology, **University of Notre Dame

We present a phase-field simulation framework for ferroelectric (FE)-FET which captures multi-domain effects. Our results signify that as T_{FE} is reduced from 10nm to 5nm, denser domain patterns emerge. If T_{FE} is scaled further from 3nm to 1.5nm, effective permittivity of the gate stack increases due to multi-domain electrostatic interactions.

10:00 a.m.
4.4 Examination of the Interplay Between Polarization Switching and Charge Trapping in Ferroelectric FET, Shan Deng, Zhouhang Jiang, Sourav Dutta, Huacheng Ye, Wriddhi Chakraborty, Santosh Kurinec, Suman Datta, Kai Ni, Rochester Institute of Technology, *University of Notre Dame

The interplay between polarization switching and charge trapping in FeFET is investigated through characterization and modeling. The charge gap in quasi-static split-CV and small-signal CV is fundamental and not indicative of trapped charge. A comprehensive FeFET model is developed to estimate trapped charge density by reproducing measured charge release dynamics.

10:10 a.m.
4.5 Depolarization Field Induced Instability of Polarization States in HfO_2 Based Ferroelectric FET, Zheng Wang, Muhammad Mainul Islam, Panni Wang, Shan Deng*, Shimeng Yu, Asif Khan, Kai Ni*, Georgia Institute of Technology, *Rochester Institute of Technology

We are demonstrating that: 1) polarization states lose its stability with scaling in HfO_2 based FeFET through multi-step degradation and potentially cause memory window collapse; 2) the instability is induced by the temperature-activated accumulation of switching probability under depolarization field, causing domain switching within the retention time at operating temperatures.

10:20 a.m.
4.6 BEOL-Compatible Multiple Metal-Ferroelectric-Metal (m-MFM) FETs Designed for Low Voltage (2.5 V), High Density, and Excellent Reliability, Meng-Hui Yan, Ming-Hung Wu, Hsin-Hui Huang, Yu-Hao Chen, Yueh-Hua Chu, Tian-Li Wu, Po-Chun Yeh*, Chih-Yao Wang*, Yu-De Lin*, Jian-Wei Su*, Pei-Jer Tzeng*, Shyh Shyuan Sheu*, Wei-Chung Lo*, Chih-I Wu*, Tuo-Hung Hou, National Chiao Tung University, *Industrial Technology Research Institute

A SPICE model considering dynamic ferroelectric switching and charge injection is established to co-optimize memory window, write speed, endurance, and retention of MFMFET. A novel m-MFMFET utilizing multiple MFMs achieves a high current on-off ratio $>10^4$ when programming at ±2.5V for 3ms without compromising 10-year retention and MFM-equivalent endurance.

Session 5: Power Devices and Systems - Recent Advances in Power Electronic Devices
Monday, December 14, 9:30 a.m. - 10:30 a.m.
Tomoko Matsudai, Toshiba Electronic Devices & Storage Corporation
Sei-Hyung Ryu, Wolfspeed--a Cree company

9:30 a.m.
5.1 Development of High-Voltage Vertical GaN PN Diodes (Invited), Robert Kaplar, Brendan Gunning, Andy Allerman, Mary Crawford, Jack Flicker, Andy Armstrong, Luke Yates, Andrew Binder, Jeremy Dickerson, Greg Pickrell, Paul Sharps, Travis Anderson*, James Gallagher*, Alan Jacobs*, Andrew Koehler*, Marko Tadjer*, Karl Hobart*, Mona Ebrish*, Matt Porter**, Rafael Martinez***, Ke Zeng, Dong Ji***, Srabanti Chowdhury, Ozgur Aktas^, Jim Cooper^^, Sandia National Labs, *NRL/Naval Research Lab, **Naval Post Graduate School, ***Stanford University, ^EDYNX, ^^Sonrisa Research Inc.

This paper describes the development of vertical GaN PN diodes. A centerpiece is the creation of a foundry that incorporates epitaxy, metrology, device design, processing, and characterization, and reliability and failure analysis. A parallel effort aims to develop very high voltage GaN PN diodes for use as grid protection devices.

9:40 a.m.
5.2 Demonstration of a ~40 kV Si Vacuum Transistor as a Practical High Frequency and Power Device, Winston Chern, Girish Rughoobur, Ahmad Zubair, Nedeljko Karaulac, Avilash Cramer*, Rajiv Gupta**, Tomas Palacios, Akintunde Akinwande, Massachusetts Institute of Technology, *Harvard-MIT Division of Health Sciences and Technology, **Mass General Hospital Department of Radiology

We demonstrate for the first time a vacuum transistor fabricated using Si operating with ~40 kV applied bias. Based upon the experimentally demonstrated principle, we illustrate the intrinsic benefits of using a vacuum drift region through benchmarking and find that vacuum outperforms all semiconductors for high frequency and power applications.

9:50 a.m.
5.3 3.3 kV Back-Gate-Controlled IGBT (BC-IGBT) Using Manufacturable Double-Side Process Technology, Takuya Saraya, Kazuo Ito, Toshihiko Takakura, Munetoshi Fukui, Shinichi Suzuki, Kiyoshi Takeuchi, Masanori Tsukuda^^^, Katsumi Satoh*, Tomoko Matsudai**, Kuniyuki Kakushima***, Takuya Hoshii***, Kazuo Tsutsui***, Hiroshi Iwai***, Atsushi Ogura^, Wataru Saito^^, Shin-ichi Nishizawa^^, Ichiro Omura^^^, Hiromichi Ohashi***, Toshiro Hiramoto, The Univerisity of Tokyo, *Mitsubishi Electric Corp., **Toshiba Electronic Devices & Storage Corp., ***Tokyo Institute of Technology, ^Meiji University, ^^ Kyushu University, ^^^Kyushu Institute of Technology

Back-gate-controlled IGBT (BC-IGBT) is experimentally demonstrated. By using the back side MOS gate, more than 60% reduction of turn-off loss was achieved. A manufacturable process using double side lithography has been developed. BC-IGBT will provide a new technological option for expanding the frequency / voltage range of Si power devices.

10:00 a.m.
5.4 5 kV Multi-Channel AlGaN/GaN Power Schottky Barrier Diodes with Junction-Fin-Anode, Ming Xiao, Yunwei Ma, Zhonghao Du*, Xiaodong Yan*, Ruizhe Zhang, Kai Cheng**, Kai Liu**, Andy Xie***, Edward Beam***, Yu Cao***, Han Wang*, Yuhao Zhang, Virginia Polytechnic Institute and State University, *University of Southern California, Los Angeles, **Enkris Semiconductor Inc, ***Qorvo

This work demonstrates multi-kilovolt Schottky barrier diodes (SBDs) on multi-channel AlGaN/GaN materials, using a new anode architecture with p-n junction wrapping around fins. Our device shows 5.2 kV breakdown voltage and 13.5 mOhmcm2 on-resistance. Large-area 4.8 kV, 1 A GaN multi-channel SBDs are also demonstrated for the first time.

10:10 a.m.
5.5 Field-induced Acceptor Ionization in Enhancement-mode GaN p-MOSFETs, Nadim Chowdhury, Qingyun Xie, John Niroula, Nitul Rajput*, Kai Cheng**, Han Wui Then***, Tomas Palacios, Massachusetts Institute of Technology, *Khalifa University, **Enkris Semiconductor Inc, ***Intel Corporation

This work demonstrates self-aligned p-MOSFET with a $GaN/Al_{0.2}Ga_{0.8}N$ (20 nm)/GaN heterostructure grown by metal-organic-chemical vapor deposition (MOCVD) on 6-inch Si substrate . Significant field-induced acceptor ionization was found in these devices at high drain voltages thereby achieving current density as high as 100 mA/mm.

10:20 a.m.
5.6 Diamond Semiconductor Devices, state-of-the-art of material growth and device processing (Invited), Hitoshi Umezawa, National Institute of Advanced Industrial Science and Technology (AIST)

Diamond is known as an ultimate semiconductor material because of its superior properties and it is expected to be employed in next-generation power electronic devices. In this paper, state of the art of diamond semiconductor devices, especially power devices and harsh environmental devices including wafer technologies will be introduced.

Session 6: Memory Technology - Charge Based Memories
Monday, December 14, 11:00 a.m. - 11:50 a.m.
Yingda Dong, Micron
Pranav Kalavade, Intel

11:00 a.m.
6.1 Past and Future of 3D Flash (Invited), Johann Alsmeier, Masaaki Higashitani, Sunhom Steve Paak, Siva Sivaram, Western Digital Corp.

3D Flash has displaced 2D Flash as the mainstream technology for NAND devices. This change brought significant increase in complexity during development and manufacturing. The paper reviews in detail the emergence of 3D Flash, continuous increase in productivity and performance and gives an outlook for future challenges and innovations needed.

11:10 a.m.
6.2 Capacitance Boosting by Anti-Ferroelectric Blocking Layer in Charge Trap Flash Memory Device, Eui Joong Shin, Sung Won Shin, Seung Hwan Lee, Tae In Lee, Min Ju Kim, Hyun Jun Ahn, Jae Hwan Kim, Wan Sik Hwang*, Jaeduk Lee**, Byung Jin Cho, KAIST (Korea Advanced Institute of Science and Technology), *Korea Aerospace University, **Samsung Electronics

We demonstrate for the first time that the use of an anti-ferroelectric film for the blocking layer of a charge trap flash (CTF) device significantly improves memory performance. It is found that a capacitance boosting effect by the anti-ferroelectric layer is the origin of the performance enhancement.

11:20 a.m.

6.3 A Vertical Split-Gate Flash Memory Featuring High-Speed Source-Side Injection Programming, Read Disturb Free, and 100K Endurance for Embedded Flash (eFlash) Scaling and Computing-In-Memory (CIM), Tzu-Hsuan Hsu, Hang-Ting Lue, Po-Kai Hsu, Teng-Hao Yeh, Pei-Ying Du, Guan-Ru Lee, Chia-Jung Chiou, Keh-Chung Wang, Chih-Yuan Lu, Macronix International Co., Ltd.

We develop a vertical split-gate Flash memory to enable eFlash scaling. The device features much smaller cell size than typical planar split-gate Flash. This device can support both regular eFlash and CIM. We can provide a flexible, tunable Icell support accurate DNN. Good TOPS/W >30 and high TOPS/mm^2 ~1 is achieved.

11:30 a.m.
6.4 3D AND: A 3D Stackable Flash Memory Architecture to Realize High-Density and Fast-Read 3D NOR Flash and Storage-Class Memory, Hang-Ting Lue, Guan-Ru Lee, Teng-Hao Yeh, Tzu-Hsuan Hsu, Chieh (Roger) Lo, Cheng-Lin Sung, Wei-Chen Chen, Chia-Tze Huang, Kuan-Yuan Shen, Meng-Yen Wu, Pishan Tseng, Min-Feng Hung, Chia-Jung Chiu, Kuang-Yeu Hsieh, Keh-Chung Wang, and Chih-Yuan Lu, Macronix International Co., Ltd.

We demonstrate a 3D stackable AND-type Flash memory architecture for high-density and fast-read non-volatile memory solution. The device is based on a gate-all-around (GAA) macaroni thin-body device, with two vertical buried diffusion lines to connect all memory cells in a parallel way to achieve 3D AND-type array.

11:40 a.m.
6.5 Industry's First Recessed Gate Transistor Technology for Sense Amplifier Circuit in DRAM: Phenomena of Randomly Threshold Voltage High Flying and Subthreshold Swing Degradation, Dongyean Oh, Heejung Yang, Seonyong Cha, Seungchul Lee, Sunjgkye Park, Jinkook Kim, SK hynix

We have fabricated a recessed gate (RG) transistor for sense amplifier in DRAM for the industyr's first. RG shows better performance of VT mismatch than planar transistor. New phenomenon of random VT high flying in defective RG and the swing degradation of RG were investigated by experiment and TCAD simulation.

11:50 a.m.
6.6 A Stacked Embedded DRAM array for LPDDR4/4X using Hybrid Bonding 3D Integration with 34GB/s/1Gb 0.88pJ/b Logic-to-Memory Interface, Bai Fujun, Jiang Xiping, Wang Song, Yu Bing, Tan Jie, Zuo Fengguo, Wang Chunjuan, Wang Fan, Long Xiaodong, Yu Guoqing, Fu Ni, Li Qiannan, Li Hua, Wang Kexin, Duan Huifu, Bai Liang, Jia Xuerong, Li Jin, Li Mei, Wang Zhengwen, Hu Sheng*, Zhou Jun*, Zhan Qiong*, Sun Peng*, Yang Daohong*, Cheichan Kau*, David Yang**, Ching-Sung Ho**, Sun Hongbin***, Lv Hangbing^, Liu Ming^, Kang Yi^^, Ren Qiwei, Xi'an UniIC Semiconductors Co., Ltd, *Wuhan Xinxin Semiconductor Manufacturing Co., Ltd., **Powerchip Semiconductor Manufacturing Corporation, ***Xi'an Jiaotong University, ^Institute of Microelectronics of the Chinese Academy of Sciences, ^^University of Science and Technology of China

Stacked Embedded DRAM(SEDRAM) was developed on LPDDR4/4X product using Hybrid Bonding. In SEDRAM, array wafer and logic wafer were fabricated separately and face-to-face connected through ultra-high-density, low-resistance Hybrid Bonding. SEDRAM offers an approach to DRAM development and accomplishes an high-bandwidth logic-to-memory interface with low power consumption.

Session 7: Optoelectronics, Displays, and Imaging Systems - Integrated Photonics
Monday, December 14, 11:00 a.m. – 12:10 p.m.
Anna Lena Giesecke, AMO GmbH

Chang-Won Lee, Hanbat National University

11:00 a.m.
7.1 Electrically Reconfigurable Active Metasurface for 3D Distance Ranging, Sun Il Kim, Junghyun Park, Byung Gil Jeong, Duhyun Lee, Jungwoo Kim, Changgyun Shin, Chang Bum Lee, Tatsuhiro Otsuka, Sangwook Kim, Ki-Yeon Yang, Yong-Young Park, Jisan Lee, Inoh Hwang, Jaeduck Jang, Kyoungho Ha, Hyuck Choo, Byoung Lyong Choi*, Sung-Woo Hwang, Samsung Electronics, *Sungkyunkwan University

We successfully demonstrate a 3-dimensional depth scan using an electrically-tunable active metasurface, which is an array of plasmonic resonators with an active indium-tin-oxide layer. Our active device can steer a beam with a positive side-mode suppression ratio. These are very promising results for small and high speed 3D depth sensing.

11:10 a.m.
7.2 Single-Chip Beam Scanner with Integrated Light Source for Real-Time Light Detection and Ranging (Late News), Jisan Lee, Dongjae Shin, Bongyong Jang, Hyunil Byun, Changbum Lee, Changgyun Shin, Inoh Hwang, Dongshik Shim, Eunkyung Lee, Jinmyung Kim, Kyunghyun Son, Tatsuhiro Otsuka, Kyoungho Ha, Hyuck Choo, Samsung Electronics

We present a single-chip solution for a solid-state Light Detection and Ranging (LIDAR) achieving 10-m ranging at 20 fps by a two dimensional beam scanner integrated with a fully functional 32-channel optical phased array, 36 optical amplifiers, and a tunable laser, all on a 7.5×3-mm^2 chip fabricated using III-V-on-silicon processes.

11:20 a.m.
7.3 Ge Photodiode with -3 dB OE Bandwidth of 110 GHz for PIC and ePIC Platforms, Stefan Lischke, Anna Peczek*, Falk Korndörfer, Christian Mai, Hansjoerg Haisch**, Michael Königsmann**, Mike Rudisile**, Daniel Steckler, Florian Goetz, Mirko Fraschke, Steffen Marschmeyer, Andreas Krüger, Yuji Yamamoto, Detlef Schmidt, Ulrike Saarow, Patric Heinrich, Aleksandra Kroh, Markus Schubert, Jens Katzer, Philipp Kulse, Andreas Trusch, Lars Zimmermann, IHP – Leibniz-Institut für innovative Mikroelektronik, *IHP Solutions GmbH, **Keysight Technologies Deutschland GmbH

We present a germanium photodiode with -3 dB bandwidth of ≥110 GHz. This performance is achieved by a novel construction where the germanium is sandwiched in between two in-situ doped silicon layers. A responsivity of >0.6 A/W (-2 V, 1550 nm) is achieved, while the dark current is ~300 nA.

11:30 a.m.
7.4 Prospects for photonic implementations of neuromorphic devices and systems (Invited), Bert Jan Offrein, Jacqueline Geler-Kremer, Jonas Weiss, Roger Dangel, Pascal Stark, Ankita Sharma, Stefan Abel, Folkert Horst, IBM Research – Zurich

Analog signal processing is one of the promising paths to enhance performance and power efficiency of neural network inference and training. Recently, analog optical neuromorphic computing concepts also gained increasing interest. We discuss properties of photonic systems in view of neuromorphic computing, applications thereof and present corresponding devices and subsystems.

11:40 a.m.
7.5 On-chip Phase Change Optical Matrix Multiplication Core, Xuan Li, Nathan Youngblood*, Wen Zhou, Johannes Feldmann**, Jacob Swett, Samarth Aggarwal, C. David Wright***, Wolfram Pernice**,

Harish Bhaskaran, University of Oxford, *University of Pittsburgh, **University of Münster, ***University of Exeter

We demonstrated a non-volatile photonic matrix computation core which contains a 3-by-3 photonic phase change in-memory computing matrix to carry out matrix vector multiplication. We demonstrated the functionality of this matrix as the linear convolution layer in a convolutional neural network (CNN) and demonstrated simple pattern recognition.

11:50 a.m.
7.6 The Memristor Laser, Bassem Tossoun, Xia Sheng, Di Liang, John Paul Strachan, Hewlett Packard Enterprise

Here we demonstrate the first-ever tunable laser with non-volatile tuning. A GaAs on Si quantum dot laser is integrated with an AlO_2 memristor, which lies on top of a silicon microring waveguide. The memristor switches the microring laser output resonant wavelength between two wavelengths in a non-volatile manner.

12:00 p.m.
7.7 Plasmonics: breaking the barriers of silicon photonics for high-performance chip-to-chip interconnects, Charles Lin, Divya Prasad*, Saurabh Sinha*, Brian Cline*, Amr S. Helmy, University of Toronto, *Arm Research

A plasmonic technology that overcomes the integration and temperature barriers of Si photonics is presented. Our amorphous-based, backend-compatible devices experimentally demonstrate >10× improvement in footprint and bandwidth while withstanding temperature fluctuation up to 100ºC, potentially enable 67.3×, 67.6× and 3.5× enhancement in chip-to-chip interconnect bandwidth density, latency, and energy-per-bit respectively.

Session 8: Microwave, Millimeter Wave, and Analog Technology - Compound Semiconductor Devices and Technologies
Monday, December 14, 11:00 a.m. - 11:50 a.m.
Sorin Voinigescu, University of Toronto
David Meyer, Naval Research Laboratory

11:00 a.m.
8.1 GaN-on-Si mm-wave RF Devices Integrated in a 200mm CMOS Compatible 3-Level Cu BEOL (Invited), Bertrand Parvais, AliReza Alian, Uthayasankaran Peralagu, Raul Rodriguez, Sachin Yadav, Ahmad Khaled, Rana Elkashlan, Vamsi Putcha, Arturo Sibaya-Hernandez, Ming Zhao, Piet Wambacq, Nadine Collaert, Niamh Waldron, imec

Millimetre-wave GaN-on-Si AlGaN HEMTs integrated with a 3 level Cu damascene BEOL flow on 200mm Si <111> wafers are demonstrated. Optimizations of the gate metal stack, contact resistance and gate length scaling to 110nm result in devices with a peak g_m of 430 mS/mm and an f_{MAX} of 135 GHz.

11:10 a.m.
8.2 Substrate RF Losses and Non-linearities in GaN-on-Si HEMT Technology, Sachin Yadav, Pieter Cardinael*, Ming Zhao, Komal Vondkar, Ahmad Khaled, Raul Rodriguez, Bjorn Vermeersch, Sergej Makovejev**, Enrique Ekoga**, Alexandre Pottrain**, Niamh Waldron, Jean-Pierre Raskin*, Bertrand Parvais, Nadine Collaert, imec, *UCLouvain, **Incize

The impact of GaN Epitaxy and HEMT fabrication process on the substrate RF losses and linearity is studied using the effective substrate resistivity and 2nd harmonic power FOM. CPWs on fully-processed, GaN-on-HR (3-6 kΩ·cm), 200 mm CZ-Si wafers achieve *H2* levels ~ -85 dBm (P_{out}~15 dBm) with ρ_{eff}~1 kΩ·cm.

11:20 a.m.
8.3 GaN/AlN p-channel HFETs with I_{max} >420 mA/mm and ~20 GHz f_T/f_{MAX}, Kazuki Nomoto, Reet Chaudhuri, Samuel Bader*, Lei Li, Austin Hickman, Shimin Huang, Hyunjea Lee, Takuya Maeda, Han Wui Then*, Marko Radosavljevic*, Paul Fischer*, Alyosha Molnar, James Hwang, Huili Grace Xing, Debdeep Jena, Cornell University, Kavli Institute for Nanoscale Science, Cornell University, *Intel Corporation

The first p-channel nitride transistors that break the GHz speed barrier are demonstrated. By leveraging the unique single-channel high-density polarization-induced 2DHG at the GaN/AlN heterostructure, the best-in-class contact resistances, and scaled T-gate design, p-channel transistor on-currents of 428 mA/mm are observed, with cutoff frequencies in the 20 GHz regime.

11:30 a.m.
8.4 L_g = 19 nm $In_{0.8}Ga_{0.2}As$ composite-channel HEMTs with f_T = 738 GHz and f_{max} = 492 GHz, Hyeon-Bhin Jo, Seung-Won Yun, Jun-Gyu Kim, Do-Young Yun, In-Geun Lee, Dae-Hyun Kim, Tae-Woo Kim*, Sang-Kuk Kim**, Jacob Yun**, Ted Kim**, Takuya Tsutsumi***, Hiroki Sugiyama***, Hideaki Matsuzaki***, Kyoungpook National University, *University of Ulsan, **QSI, ***NTT Device Technology Laboratories

We present L_g = 19 nm $In_{0.8}Ga_{0.2}As$ composite-channel high-electron mobility transistors (HEMTs) with outstanding DC and high-frequency characteristics. The device with L_g = 19 nm displayed an excellent combination of R_{ON} = 271 Ω-µm, g_{m_max} = 2.5 mS/µm and f_T/f_{max} = 738/492 GHz.

11:40 a.m.
8.5 Ballistic Mobility and Injection Velocity in Nanoscale InGaAs FinFETs, Xiaowei Cai, Alon Vardi, Jesús Grajal*, Jesús del Alamo, Massachusetts Institute of Technology, *Universidad Politécnica de Madrid

This work presents an experimental study of ballistic transport in nanoscale InGaAs FinFETs with fin widths down to 9 nm. Mobility and injection velocity are extracted using techniques immune to underestimation caused by oxide trapping. We find that transport in short channel devices is not degraded by fin width narrowing.

Session 9: Reliability of Systems and Devices - Reliability challenges from transistors to products
Monday, December 14, 11:00 a.m. – 12:10 p.m.
Kirsten Weide-Zaage, Leibniz Universität Hannover
Charlie Slayman, Cisco

11:00 a.m.
9.1 A fast Wafer Level Reliability (fWLR) Monitoring concept as a continuous reliability indicator for wafer mass production (Invited), A. Martin, A. Mitchell, M. Traving, S. Wegner, A. Norman-Elvenich, H. Mayr, H. Nielen, Infineon Technologies AG

Fast Wafer Level Reliability (fWLR) Monitoring includes highly accelerated reliability stresses in the range of seconds, which are performed daily on specifically designed test structures usually placed in the scribe line of productive wafers.

11:10 a.m.

9.2 A Reliability Enhanced 5nm CMOS Technology Featuring 5th Generation FinFET with Fully-Developed EUV and High Mobility Channel for Mobile SoC and High Performance Computing Application, J.C. Liu, Subhadeep Mukhopadhyay, Amit Kundu, S.H. Chen, H.C. Wang, D.S. Huang, J.H. Lee, M.I. Wang, Ryan Lu, S.S. Lin, Y.M. Chen, Huiling Shang, P.W. Wang, H.C. Lin, Geoffrey Yeap, Jun He, TSMC

To keep up with the dominance in the field of leading semiconductor technology innovation, TSMC has announced the risk production of its most advanced 5nm CMOS logic node [1] using the full-fledged EUV and high mobility channel (HMC) FinFETs

11:20 a.m.

9.3 Reliability on Evolutionary FinFET CMOS Technology and Beyond (Invited), Kihyun Choi, Hyun Chul Sagong, Minjung Jin, Jiang Hai, Miji Lee, TaeYoung Jeong, Myung Soo Yeo, Hyewon Shim, Da Ahn, Wooyeon Kim, Yongjeung Kim, JuneKyun Park, Hwasung Rhee, Euncheol Lee, Samsung Electonics

Extensive analysis from intrinsic to extrinsic reliability on evolutionary FinFET CMOS technology was demonstrated. Intrinsic reliability such as HCI, BTI, and TDDB showed similar behavior across Fin technology generations. FinFET self-heating and BEOL Joules heating were characterized. The extrinsic failure could be predicted by wafer level TDDB mass testing.

11:30 a.m.

9.4 Characterization Scheme for Plasma-Induced Defect due to Stochastic Lateral Straggling in Si Substrates for Ultra-Low Leakage Devices, Yoshihiro Sato, Takayoshi Yamada, Kazuko Nishimura, Masayuki Yamasaki, Masashi Murakami, Keiichiro Urabe*, Koji Eriguchi*, Panasonic Corporation, *Kyoto University

This study demonstrates a new characterization scheme to assess the density and profile of defects in the lateral direction and to verify their impacts using CMOS image sensor-based structures. We present a 3D (vertical and lateral) defect map as well as possible optimization strategies for ultra-low leakage devices.

11:40 a.m.

9.5 An Improved Model on Buried-Oxide Damage for Total-Ionizing-Dose Effect on HV SOI LDMOS, Zhangyi'an Yuan, Ming Qiao, Xinjian Li, Xin Zhou, Zhaoji Li, Bo Zhang, University of Electronic Science and Technology of China

Experimental results indicates that N_{ot} generated in SOI/BOX interface even if the electric field plays a negative role. The improved model on BOX damage induced by TID considering this set of N_{ot} and its saturation effect is proposed and adopted in simulation to predict the post-irradiation HV SOI LDMOS behavior.

11:50 a.m.

9.6 Multiphonon-Electron Coupling Enhanced Defect Generation and Breakdown Mechanism in MOL New Spacer Dielectrics for 7nm/5nm Technology Nodes and Beyond, Ernest Y. Wu, Richard Southwick III, Sanjay Mehta, Baozhen Li, Miaomiao Wang, IBM Research

We investigate multiphonon-electron coupling enhanced defect generation process and breakdown (BD) in middle-of-line (MOL) spacer dielectrics (Si_3N_4, SiBCN, and SiOCN). We demonstrate defect

generation process follows a universal process independent of thickness. By extracting the defect information at BD, we establish a physics-based BD model with new defect generation rate.

12:00 p.m.
9.7 Custom Silicon at Facebook: A Datacenter Infrastructure Perspective on Video Transcoding and Machine Learning, Prahlad Venkatapuram, Zhao Wang, Chandra Mallipedi, Facebook

This paper describes several important aspects of the Application Specific Integrated Circuits (ASIC) development efforts happening at Facebook to serve its hyperscale datacenter networks. Motivations, key features, benefits and challenges for custom silicon development supporting machine learning algorithms and video processing are introduced. Power strategies and reliability considerations are also addressed.

Session 10 – Plenary 2: Tuesday, 8:00 a.m.
Memory Technology: Innovations needed for continued technology scaling and enabling advanced computing systems (Invited), Naga Chandrasekaran, Micron

Session 11: Memory Technology - STT-MRAM Technology
Tuesday, December 15, 9:30 a.m. - 10:30 a.m.
Guohan Hu, IBM
Jung-Hyuk Lee, Samsung

9:30 a.m.
11.1 MRAM in Microcontroller and Microprocessor Product Applications (Invited), Thomas Jew, NXP Semiconductors

MRAM is finally establishing itself as a viable non-volatile memory (NVM) technology and solution for advanced Microcontrollers and even Microprocessors. Multiple foundries are making investments to bring production capabilities on-line, demonstrating MRAM memory solutions. MRAM applications and use cases in advanced Microcontrollers and Microprocessors.

9:40 a.m.
11.2 28-nm 0.08 mm^2/Mb Embedded MRAM for Frame Buffer Memory, Shinhee Han, Jongmin Lee, Hyemin Shin, Junghyuk Lee, Kiseok Suh, Kyungtae Nam, Baesung Kwon, Minkwon Cho, Joonmyoung Lee, Junho Jeong, Jeong-Heon Park, Sechung Oh, Soon Oh Park, Sohee Hwang, Suksoo Pyo, Hyuntaek Jung, Yongsung Ji, Junghoon Bak, Daeshik Kim, Wooseung Ham, Yongjae Kim, Kilho Lee, Kangho Lee, Yoonjong Song, Gwan-Hyeob Koh, Youngki Hong, Gitae Jeong, Samsung Electronics Co.

We present the world-first demonstration of 28-nm embedded MRAM for frame buffer memory. Compared to SRAM that is commonly used for frame buffer memory, eMRAM provides 47% area saving. Required read disturbance and endurance margins for frame buffer applications with sufficient read/write speed have been verified.

9:50 a.m.
11.3 JEDEC-Qualified Highly Reliable 22nm FD-SOI Embedded MRAM For Low-Power Industrial-Grade, and Extended Performance Towards Automotive-Grade-1 Applications, Vinayak Bharat Naik, Kazutaka Yamane, Tae Young Lee, Jae-Hyun Kwon, Robin Chao, Jiahao Lim, Nyuk Leong Chung, Behtash Behin-Aein, Lee Yong Hau, Dinggui Zeng, Yuichi Otani, Chunsung Chiang, Yentsai Huang, Lejan Pu, Suk Hee Jang, Wah Peng Neo, Hemant Dixit, Sivabalan K, Lian Choo Goh, Eng-Huat Toh, Timothy Ling, Jay Hwang, Jia Wen Ting, Liying Zhang, Rachel Low, Lei Zhang, Choongay Lee, N. Balasankaran, F. Tan, K. W. Gan, H. Yoon, G. Congedo, J. Mueller,2 B. Pfefferling,2 O. Kallensee, A.

Vogel, V. Kriegerstein, T. Merbeth, C.S. Seet, S. Ong, J. Xu, J. Wong, Y.S. You, S.T. Woo, T.H. Chan, E. Quek, S.Y. Siah, Globalfoundries

We demonstrate JEDEC-qualified, mass-production ready 22nm-FD-SOI 40Mb embedded-MRAM for low-power industrial-grade (-40~125°C), and extended-performance towards Auto-Grade-1 (-40~150°C) applications. From design-process co-optimization, achieved ~47% reduced read power, 20yrs data-retention, 1M read-cycles under 500Oe, 1M endurance-cycles, stand-by magnetic immunity of ~500Oe at 150°C, and ~4kOe using shield-in package at 25°C, 48hrs .

10:00 a.m.
11.4 A Reflow-capable, Embedded 8Mb STT-MRAM Macro with 9nS Read Access Time in 16nm FinFET Logic CMOS Process, Yi-Chun Shih, Chia-Fu Lee, Yen-An Chang, Po-Hao Lee, Hon-Jarn Lin, Yu-Lin Chen, Chieh-Pu Lo, Ku-Feng Lin, Tien-Wei Chiang, Yuan-Jen Lee, Kuei-Hung Shen, Roger Wang, Wayne Wang, Harry Chuang, Eric Wang, Yu-Der Chih, Jonathan Chang, Taiwan Semiconductor Manufacturing Company

An 8Mb STT-MRAM macro in 16nm FinFET Logic CMOS process is presented. The macro achieves solder-reflow tolerance, short write pulse of 50nS, and read access time of 9nS from -40C to 125C and Vdd=0.8V±10%. The bit-error-rate has achieved zero fail-bit-count for the 8Mb macro at 50-percentile at wafer level.

10:10 a.m.
11.5 A 14 nm Embedded STT-MRAM CMOS Technology, D. Edelstein*, M. Rizzolo, D. Sil, A. Dutta, J. DeBrosse, M. Wordeman, A. Arceo, I. C. Chu, J. Demarest, E. R. J. Edwards, E. R. Evarts, J. Fullam, A. Gasasira, G. Hu, M. Iwatake, R. Johnson, V. Katragadda, T. Levin, J. Li, Y. Liu, C. Long, T. Maffitt, S. McDermott, S. Mehta, V. Mehta, D. Metzler, J. Morillo, Y. Nakamura, S. Nguyen, P. Nieves, V. Pai, R. Patlolla, R. Pujari, R.
Southwick, T. Standaert, O. van der Straten, H. Wu, C.-C. Yang, D. Houssameddine, J. M. Slaughter, and D. C. Worledge., IBM Research

We present the first Embedded STT MRAM (eMRAM) technology in a 14 nm CMOS node. A novel integration supports the highest density (0.0273 um^2 cells), MTJ bbetween M1-M2, and only 3 added masks. We demonstratel functionality, write performance down to 4 ns, magnetoresistance, switching voltage, retention, and endurance cycling.

10:20 a.m.
11.6 Advanced MTJ Stack Engineering of STT-MRAM to Realize High Speed Applications, Tae Young Lee, Kazutaka Yamane, Yuichi Otani, Dinggui Zeng, Jae-Hyun Kwon, Jiahao Lim, Vinayak Bharat Naik, Lee Yong Hau, Robin Chao, Nyuk Leong Chung, Timothy Ling, Suk Hee Jang, Lian Choo Goh, Jay Hwang, Lei Zhang, Rachel Low, Nivetha Balasankaran, Funan Tan, Jia Wen Ting, Joy Chang, Chim Seng Seet, Stanley Ong, Young Seon You, Swee Tuck Woo, Tze Ho Chan, Soh Yun Siah, Globalfoundries Singapore Pte. Ltd.

We demonstrate superior data retention of 1month at 125°C with improved switching efficiency at 10ns write without back-hopping failure. The macro shows operating temperature (-40~150°C) and zero fail bit count with ECC-on. The tight switching voltage distribution and the coherent switching are essential for fast switching and back-hopping margin improvement.

Session 12: Emerging Device and Compute Technology - Applications for 2D materials and carbon nanotubes beyond simple CMOS transistors
Tuesday, December 15, 9:30 a.m. - 10:30 a.m.

Helen Li, Duke University
Thomas Muller, Vienna University of Technology

9:30 a.m.
12.1 High Drive and Low Leakage Current MBC FET with Channel Thickness 1.2nm/0.6nm, Xiaohe Huang, Chunsen Liu, Zhaowu Tang, Senfeng Zeng, Liwei Liu, Xiang Hou, Huawei Chen, Jiayi Li, Yu-Gang Jiang, David Wei Zhang, Peng Zhou, Fudan University

We demonstrate a 2-levels-stacked multi-bridge-channels (MBC) FET with channel thickness only 1.2/0.6nm. The normalized drive current per level is comparable to the latest 7-levels-stacked Si MBC FET. This ultrathin MBC FET demonstrates a very low leakage current per level, only 6.5% of the value of the Si MBC FET.

9:40 a.m.
12.2 3D Integration of Vertical-Stacking of MoS_2 and Si CMOS Featuring Embedded 2T1R Configuration Demonstrated on Full Wafers, C. J. Su, M. K. Huang*, K. S. Lee**, V. P. H. Hu***, Y. F. Huang^, B. C. Zheng^, C. H. Yao^, N. C. Lin, K. H. Kao*, T. C. Hong**, P. J. Sung, C. T. Wu, T. Y. Yu, K. L. Lin, Y. C. Tseng**, C. L. Lin^, Y. J. Lee, T. S. Chao*, J. Y. Li1***, W. F. Wu, J. M. Shieh, Y. H. Wang* and W. K. Yeh, Taiwan Semiconductor Research Institute, *National Cheng Kung University, **National Chiao Tung University, ***National Taiwan University, ^Feng Chia University

A 3D-stacking of MoS_2 and Si CMOS integrated with embedded RRAM is proposed. CMOS inverter and Ti/MoS_2/p^+-Si RRAM with ON/OFF ratio of 10^6 are demonstrated. Surface modification is the key to form uniform stacked MoS_2 multi-channels and enhanced resistive-switching endurance. This work offers the co-existence of CMOS and NVM functions.

9:50 a.m.
12.3 0.5T0.5R - Introducing an Ultra-Compact Memory Cell Enabled by Shared Graphene Edge-Contact and *h*-BN Insulator, Chao-Hui Yeh, Dujiao Zhang, Wei Cao, Kaustav Banerjee, University of California, Santa Barbara

In this work, we experimentally demonstrate, in a manufacture-friendly process, a hybrid memory device to replace the traditional 1T1R memory unit. Record performance (<10 ns switching speed), energy (~0.07 pJ/bit) and area efficiency, as well as great retention (10^6 s) and endurance (>1000), have been achieved.

10:00 a.m.
12.4 Scaling MoS_2 NCFET to 83 nm with Record-low Ratio of $SS_{ave}/SS_{Ref.}$=0.177 and Minimum 20 mV Hysteresis, Guanhua Yang, Jiebin Niu, Congyan Lu, Rongrong Cao*, Jiawei Wang, Ying Zhao, Xichen Chuai, Mengmeng Li, Di Geng, Nianduan Lu, Qi Liu, Ling Li, Ming Liu, Chinese Academy of Sciences, *National University of Defense Technology

For the first time, we experimentally prove that MoS_2 NCFET can benefit from device scaling. In the short-channel device, ultra-low SS is demonstrated without suffering from hysteresis. The average SS improvement factor of MoS_2 NCFET w. r. t. reference FET, reaches a record-low value of 0.177 among all 2D NCFETs.

10:10 a.m.
12.5 Monolayer MoS_2 Steep-slope Transistors with Record-high Sub-60-mV/decade Current Density Using Dirac-source Electron Injection, Maomao Liu, Hemendra Nath Jaiswal, Simran Shahi,

Sichen Wei, Yu Fu, Chaoran Chang, Anindita Chakravarty, Fei Yao, Huamin Li, The State University of New York at Buffalo

For the first time, a 2D monolayer MoS_2 steep-slope transistor based on novel Dirac-source electron injection was demonstrated, which shows the minimum subthreshold swing of 29 mV/decade and a record-high sub-60-mV/decade current density over 1 µA/µm, compared to any 2D or 3D tunneling transistors or negative capacitance transistors.

10:20 a.m.
12.6 The demonstration of Carbon Nano-Tubes (CNTs) as a promising high Aspect Ratio (>25) Through Silicon Vias (TSVs) material for the vertical connection in the high dense 3DICs, P.-Y. Lu, C.-M. Yen, S.-Y. Chang, Y.-J. Feng, C. Lien, Chun-Wei Yao*, M.-H. Lee**, Ming-Han Liao, National Taiwan University, *Lamar University, **National Taiwan Normal University

With the evaluation of the total system-level electrical performance including bandwidth density, power density, and reliability, CNTs as the high aspect ratio (>25) and small diameter (<5mm) Through Silicon Vias (TSVs) is demonstrated for the application of future high-dense 3DICs system from both mechanical and electrical points of view.

Session 13: Modeling and Simulation - Emerging Non-Volatile Memories and 3D Integration
Tuesday, December 15, 9:30 a.m. - 10:30 a.m.
Wei-Chen Chen, MXIC
Thierry Poiroux, CEA-LETI

9:30 a.m.
13.1 Thermal Modeling of 3D Polylithic Integration and Implications on BEOL RRAM Performance (Invited), Ankit Kaul, Xiaochen Peng, Sreejith Kochupurackal Rajan, Shimeng Yu, Muhannad S Bakir, Georgia Institute of Technology

We present thermal evaluation of a BEOL-embedded chiplet integration scheme. The impact of 3D integration and cooling on RRAM reliability is quantified by image recognition accuracy over time for a DNN hardware model. Worst-case accuracy drop at 10 years was estimated as 82% for air-cooling compared to 2% for liquid-cooling.

9:40 a.m.
13.2 Atomic-Device Hybrid Modeling of Relaxation Effect in Analog RRAM for Neuromorphic Computing, Feng Xu, Bin Gao, Yue Xi, Jianshi Tang, Huaqiang Wu, He Qian, Tsinghua University

Conductance relaxation effect in analog RRAM devices poses a great challenge in building neuromorphic system with high accuracy. We develop a new atomic-device hybrid modeling technique to investigate the physical mechanism of resistive switching and relaxation effect in amorphous-HfOx based analog RRAM, that provides valuable guidelines for improving RRAM reliability.

9:50 a.m.
13.3 Modeling of virgin state and forming operation in embedded phase change memory (PCM), M. Baldo, O. Melnic, M. Scuderi*, G. Nicotra*, M. Borghi**, E. Petroni**, A. Motta**, P. Zuliani**, A. Redaelli** and D. Ielmini, Politecnico di Milano and IU.NET, *CNR-IMM, **STMicroelectronics

Embedded PCM show optimized performance thanks to Ge enrichment of the GeSbTe material. However, excess Ge tends to segregate in the virgin state, which requires an initial forming process for

initializing the PCM device. This work presents the detailed energy landscape model for embedded PCMs before forming and after forming.

10:00 a.m.
13.4 Technology-Array-Algorithm Co-Optimization of RRAM for Storage and Neuromorphic Computing: Device Non-idealities and Thermal Cross-talk (Invited), Yimao Cai, Zongwei Wang, Zhizhen Yu, Yaotian Ling, Qingyu Chen, Yunfan Yang, Shengyu Bao, Lindong Wu, Lin Bao, Runsheng Wang, Ru Huang, Peking University

This paper presents the modeling of device non-idealities, including parameter variations and time-dependent fluctuation (TDV), and the simulation of array thermal crosstalk. We also investigate the impact of non-idealities and thermal issues on storage and neuromorphic computing from the device, array, and algorithm perspectives, providing guidelines for the technology-circuit-algorithm co-optimization.

10:10 a.m.
13.5 TCAD Device Technology Co-Optimization Workflow for Manufacturable MRAM Technology, Hemant Dixit, Vinayak Bharat Naik, Kazutaka Yamane, Tae Young Lee, Jae-Hyun Kwon, Behtash Behin-Aein, Steven Soss, William Taylor, Globalfoundries

TCAD device technology co-optimization workflow is presented, which allows stack engineering to qualify technology specific design targets. Implications of etch and integration steps on STT switching and Write Error Rates are discussed. Results obtained provide critical insight for optimizing the WER for futuristic MRAM technology in Last Level Cache applications.

10:20 a.m.
13.6 Spin-Orbit-Torque Material Exploration for Maximum Array-Level Read/Write Performance, Yu-Ching Liao, Piyush Kumar, Mahendra DC*, Xiang Li, Delin Zhang**, Jian-Ping Wang**, Shan X. Wang, Daniel C. Ralph***, Azad Naeemi, Georgia Institute of Technology, *Stanford University, **University of Minnesota, ***Cornell University

This paper presents a comprehensive study on the impact of spin-orbit-torque (SOT) material parameters on array-level read and write operations for in-plane and out-of-plane magnetic random access memory (MRAM) devices. The results offer important guidelines for material development for this technology.

Session 14: Sensors, MEMS, and Bioelectronics - Biomedical Micro/Nano-Devices
Tuesday, December 15, 9:30 a.m. - 10:30 a.m.
Wen Li, Michigan State University
Luca Berdondini, Fondazione Istituto Italiano di Tecnologia

9:30 a.m.
14.1 Neuro-electronic devices and nanotools to interact with neuronal networks (Invited), Sergio Martinoia, Andrea Andolfi, Lorenzo Muzzi, Marietta Pisano, Andrea Spanu*, Roberto Raiteri, University of Genova, *University of Cagliari

Neuro-electronic interfaces play a fundamental role for studying brain functions and cellular mechanisms of information processing. Here we present a new concept in which electronic devices are integrated with models of neuronal networks of human origin together with nanotools for electrophysiological activity recording and stimulation.

9:40 a.m.

14.2 Thin-Film Transistor Platform for Electrophysiological and Electrochemical Characterization of Cells, Anne-Claire Eiler, Pierre-Marie Faure*, Junichi Sugita, Satoshi Ihida, Dongchen Zhu, Yasuyuki Sakai, Katsuhito Fujiu, Kikuo Komori** Hiroshi Toshiyoshi, Agnes Tixier-Mita, The University of Tokyo, * ENSEIRB-MATMECA, **Kindai University

This paper presents a transparent Thin-Film Transistor integrated sensors platform for 2D electrophysiological and electrochemical measurements for investigation of cardiomyocyte electrical activity. The integration of electrochemical sensors allows complete electrical, chemical, and optical analyses of large cell cultures, tissues, or organoids, which opens the door to lab-on-a-chip devices using sensors.

9:50 a.m.
14.3 High-resolution neurostimulation and optogenetic electrophysiology with PEDOT:PSS-coated graphene, Feng Sun, Zheshun Xiong, Jinyoung Park, Guangyu Xu, University of Massachusetts Amherst

We present a 28-µm pitched PEDOT:PSS-coated graphene microelectrode array (MEA) that achieves 1-order higher resolution than prior graphene MEAs in both neurostimulation and optogenetic electrophysiology. Our array features 100% yield, low impedance (sub-100kΩ), low light-induced artifact (sub-2µV), and high charge-injection-capacity (>1.31 mC/cm^2), suggesting its possible use for high-precision multi-modal neurointerfacing.

10:00 a.m.
14.4 Flexible Bootstrapped Cascode System with Feedback for Capacitive Through-Substrate Electric Potential Measurements with a 55 dB Relative Gain, Julio Costa, Arash Pouryazdan, Robert Prance, Helen Prance, Niko Münzenrieder, University of Sussex

Measuring electric potentials using encapsulated flexible sensors is advantageous when the signal source is soft or irregular, such as the human brain. Here, we show an a-IGZO based bootstrapped capacitive electric potential sensor exhibiting a relative gain of 55 dB and a bandwidth between 450 Hz and 19 kHz.

10:10 a.m.
14.5 Nanophotonic sensor implants with 3D hybrid periodic-amorphous photonic crystals for wide-angle monitoring of long-term *in-vivo* intraocular pressure, Radwanul Siddique, Lukas Liedtke*, Haeri Park, Siyoung Lee**, Hamza Raniwala*, Doyoung Park**, Donghui Lim**, Hyuck Choo*, Samsung Semiconductor, Inc., *Caltech, **Samsung Medical Centre

We developed a nanophotonic-based optomechanical sensor and reported the smallest intraocular(IOP) pressure implant for Glaucoma management. The sensor consists of nanostructured biocompatible silicone with hybrid photonic crystals for generating wide-angle(±40° pressure-dependent NIR resonance (0.1 nm/mmHg). Using IOP-sensing implants and handheld detector, we successfully tracked 6-months long IOP in-vivo in rabbits.

Session 15: Advanced Logic Technology - 3D technologies
Tuesday, December 15, 11:00 a.m. – 12:00 p.m.
Ying Li, Lam Research
Stefan Schulz, Fraunhofer ENAS & TU Chemnitz

11:00 a.m.
15.1 A high-density logic-on-logic 3DIC design using face-to-face hybrid wafer-bonding on 12nm FinFET process, Saurabh Sinha, Shawn Hung, Daniel Fisher*, Xiaoqing Xu, Chien-Ju Chao, Pranavi

Chandupatla, Frank Frederick, Heath Perry, Daniel Smith*, Alberto Cestero*, John Safran*, Vetrivel Ayyavu, Mudit Bhargava, Rahul Mathur, Divya Prasad, Robert Katz*, Albert Kinsbruner*, John Garant*, Jorge Lubguban*, Sarah Knickerbocker*, Vilmarie Soler*, Brian Cline, Robert Christy, Teresa McLaurin, Norman Robson*, Daniel Berger*, Arm Inc., *Globalfoundries

A 3D test-vehicle showcasing a synchronous cache coherent mesh interconnect design operational at 2.4 GHz using 5.76µm pitch face-to-face wafer-bond 3D connections on a 12nm FinFET process is presented. A 3D aggregate bandwidth of 307 GB/s, a bandwidth density of 3.4 TB/s/mm^2, and energy efficiency of 0.02 pJ/bit is demonstrated.

11:10 a.m.
15.2 3D-optimized SRAM Macro Design and Application to Memory-on-Logic 3D-IC at Advanced Nodes, Rongmei Chen, Pieter Weckx, Shairfe Muhammad Salahuddin, Soon-Wook Kim, Giuliano Sisto, Geert Van der Plas, Michele Stucchi, Rogier Baert, Peter Debacker, Myunghee Na, Julien Ryckaert, Dragomir Milojevic, Eric Beyne, imec

We present SRAM macro optimizations at 3nm and 2nm nodes using our demonstrated sub-1um 3D hybrid-bonding technology. 3D-optimized macros are designed to reduce macro external delay with performance improvement more than 70% observed. A Memory-on-Logic design using 3D-optimized macros achieves 33% system performance gain with respect to a 2D implementation.

11:20 a.m.
15.3 How 3D integration technologies enable advanced compute node for Exascale-level High Performance Computing ? (Invited), Denis Dutoit, Perceval Coudrain*, Pierre-Yves Martinez, Pascal Vivet, Jean Charbonnier*, Arnaud Garnier*, Didier Lattard, Severine Cheramy*, Eric Guthmuller, Anthony Philippe, Yvain Thonnart, Fabien Clermidy, CEA-List, *CEA-Léti

Supercomputers will soon achieve Exascale-level computing performances mainly thanks to the introduction of innovative hardware technologies around the processors. This article explains architectural and performance evolutions and describes how 3D integration technologies have allowed heterogeneity and increased bandwidth that are decisive for hardware innovations contributing to Exascale.

11:30 a.m.
15.4 System exploration and technology demonstration of 3D Wafer-to-Wafer integrated STT-MRAM based caches for advanced Mobile SoCs, Manu Perumkunnil, Farrukh Yasin, Siddharth Rao, Shairfe Muhammad Salahuddin, Dragomir Milojevic, Geert Van der Plas, Julien Ryckaert, Eric Beyne, Arnaud Furnemont, Gouri Sankar Kar, imec

This paper analyzes 3D partitioned STT-MRAM caches in an advanced Mobile SoC based on the process demonstration of the first ever functional 3D Wafer-to-Wafer (W2W) integrated STT devices. We show that these caches can lead to 30% performance improvement at 17% power and 15% footprint reduction for our target SoC.

11:40 a.m.
15.5 First Demonstration of heterogeneous Complementary FETs utilizing Low-Temperature (200 °C) Hetero-Layers Bonding Technique (LT-HBT), T.-Z. Hong, W.-H. Chang*, A. Agarwal***, Y.-T. Huang^, C.-Y. Yang***, T.-Y. Chu***, H.-Y. Chao***, Y. Chuang^^, S.-T. Chung**, J.-H. Lin^^^, S.-M. Luo^^^, C.-J. Tsai^^^, M.-J. Li^^^, X.-R. Yu***, N.-C. Lin, T.-C. Cho, P.-J. Sung, C.-J. Su, G.-L. Luo, F.-K. Hsueh, K.-L. Lin, H. Ishii*, T. Irisawa*, T. Maeda*, C.-T. Wu, W. C.-Y. Ma^^^, D.-D. Lu*** K.-H. Kao***, Y.-J. Lee, H. J.-H. Chen^, C.-L. Lin+, R. W. Chuang***, K.-P. Huang++, S. Samukawa+++, Y.-M. Liˇ, J.-H. Tarngˇ, T.-S. Chao**, M. Miuraˇˇ, G.-W. Huang, W.-F. Wu, J.-Y. Li^^,

J.-M. Shieh, Y.-H. Wang***, W.-K. Yeh, Taiwan Semiconductor Research Inst., *Natl. Inst. of Adv. Ind. Sci. Tech. (AIST), **Natl. Chiao Tung University, ***Natl. Cheng Kung University, ^ Natl. Chi Nan University, ^^Natl. Taiwan University, ^^^ Natl. Sun Yat-Sen University, + Feng Chia University, ++MMSL, +++Tohoku University, ˋNatl. Chiao Tung University, ˇHitachi High-Technologies Corp.

We demonstrate hCFETs with Ge and Si channels. The 3D channel stacking integration employs a low-temperature (200 °C) hetero-layers bonding technique by surface activating chemical treatment, enabling Ge channels bonded onto Si wafers. Wafer-scale LT-HBT has been proven, showing new opportunities for the ultimate device footprint scaling with heterogeneous integration.

11:50 a.m.
15.6 Low Temperature and Ion-Cut Based Monolithic 3D Process Integration Platform Incorporated with CMOS, RRAM and Photo-Sensor Circuits, Hoonhee Han, Rino Choi*, Seong-Ook Jung**, Sung Woo Chung***, Byung Jin Cho^, S.C. Song^^, Changhwan Choi, Hanyang University, *Inha University, *Yonsei University, **Korea University, ***KAIST (Korea Advanced Institute of Science and Technology), ^Qualcomm

We demonstrated low temperature (< 500℃) and H^+-cut based monolithic 3D (M3D) integration using current sensor, CMOS ring-oscillator circuits, RRAM and photodetector. Upper layer transfer is affected by ion implantation process, ILD, surface treatment, oxide CMP and annealing. Frequency and current of integrated M3D devices are well-modulated by light exposure.

Session 16: Optoelectronics, Displays, and Imaging Systems - Image Sensors
Tuesday, December 15, 11:00 a.m. - 12:00 p.m.
Boyd Fowler, OmniVision
Jae-Kyu Lee, Samsung Electronics

11:00 a.m.
16.1 A 4.6µm, 512×512, Ultra-Low Power Stacked Digital Pixel Sensor with Triple Quantization and 127dB Dynamic Range, Chiao Liu, Lyle Bainbridge, Andrew Berkovich, Song Chen, Wei Gao, Tsung-Hsun Tsai, Kazuya Mori*, Rimon Ikeno, Masayuki Uno*, Toshiyuki Isozaki*, Yu-Lin Tsai**, Isao Takayanagi*, Junichi Nakamura*, Facebook Inc, *Brillnics Japan Inc., **Brillnics Inc.

A 512x512 digital pixel sensor (DPS) in stacked CIS process for ultra-low power, ultra-wide dynamic range mobile computer vision applications is presented. Each 4.6µm DPS pixel has an ADC and 10-bit SRAM. We introduce a single exposure triple quantization (3Q) scheme to achieve 127dB DR while consuming 5.3mW at 30fps.

11:10 a.m.
16.2 A 0.8 µm Nonacell for 108 Megapixels CMOS Image Sensor with FD-Shared Dual Conversion Gain and 18,000e- Full-Well Capacitance, Youngsun Oh, Munhwan Kim, Wonchul Choi, Hana Choi, Honghyun Jeon, Junho Seok, Yujung Choi, Jaejin Jung, Kwisung Yoo, Donghyuk Park, Yitae Kim, Kyoung-min Koh, Jesuk Lee, Chang-Rok Moon, JungChakAhn, Samsung Electronics Co., Ltd.

A 0.8µm-pitch 108 megapixels ultrahigh-resolution CMOS image sensor has been demonstrated for mobile applications. The Nonacell was developed with odd-number shared pixel, and the FWC was secured up to 18,000e-. 3 active binning mode to achieve 12 megapixels resolution, ensuring excellent low- and high-illuminance SNR.

11:20 a.m.

16.3 A 64M CMOS Image Sensor using 0.7um pixel with high FWC and switchable conversion gain, Y. Jay Jung, Vincent Venezia, Sangjoo Lee, Chun Yung Ai, Yibo Zhu, King W. Yeung, Geunsook Park, Woonil Choi, Zhiqiang Lin, Wu-Zang Yang, Alan Chih-Wei Hsiung, Lindsay Grant, OmniVision Technologies, Inc.

This paper presents a 64MP, backside-illuminated, imager using 0.7um pixel-pitch with 7.0ke- FWC. Switchable-conversion-gain was also demonstrated to have high 18.0ke- FWC in 4-Cell mode. Several new processes were implemented to overcome pixel performance degradation. As a result, this high-FWC imager achieves low dark-noise and high QE, comparable to 0.8um.

11:30 a.m.
16.4 A Global Shutter Wide Dynamic Range Soft X-ray CMOS Image Sensor with BSI Pinned Photodiode, Two-stage LOFIC and Voltage Domain Memory Bank, Hiroya Shike, Rihito Kuroda, Ryota Kobayashi, Maasa Murata, Yasuyuki Fujihara, Manabu Suzuki, Taku Shibaguchi*, Naoya Kuriyama*, Jun Miyawaki**, Tetsuo Harada***, Yuichi Yamasaki^, Takeo Watanabe***, Yoshihisa Harada***, Shigetoshi Sugawa, *Tohoku University, **LAPIS Semiconductor Co., Ltd., ***The University of Tokyo, ^University of Hyogo

A prototype soft X-ray CMOS image sensor (sxCMOS) with BSI pinned photodiode with a 45µm-thick Si substrate, two-stage LOFIC and voltage domain memory bank with high density capacitors is presented. The fabricated chip demonstrated a high QE toward soft X-ray with a single exposure 129dB dynamic range by global shutter.

11:40 a.m.
16.5 Imaging in Short-Wave Infrared with 1.82 µm Pixel Pitch Quantum Dot Image Sensor, Jiwon Lee, Epimitheas Georgitzikis, Yunlong Li, Ziduo Lin, Jihoon Park, Itai Lieberman, David Cheyns, Murali Jayapala, Andy Lambrechts, Steven Thijs, Richard Stahl, Pawel Malinowski, imec

High pixel density SWIR image sensor with 1.82 µm pixel pitch is presented. PbS QD photodiode is monolithically integrated on custom CMOS readout. We show through-silicon vision and lens-free imaging (LFI) examples. To our knowledge, this is the smallest pitch SWIR pixel ever reported and the first QD-based LFI system.

11:50 a.m.
16.6 A Back Illuminated 10µm SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm, K. Ito, Y. Otake, Y. Kitano, A. Matsumoto, J. Yamamoto, T. Ogasahara, H. Hiyama, R. Naito*, K. Takeuchi*, T. Tada*, K. Takabayashi*, H. Nakayama*, K. Tatani, T. Hirano, and T. Wakano, Sony Semiconductor Solutions, *Sony Semiconductor Manufacturing

We developed a BI 10um SPAD array sensor using pixel-level Cu-Cu bonding and metal-buried Full Trench Isolation. Using a 7um thick Si layer, a fine-tuned potential and process, over 14% PDE at λ=940nm and the best in class DCR were achieved. Low timing jitter and suppressed X-talk were also demonstrated.

Session 17: Microwave, Millimeter Wave, and Analog Technology - System and technology for mm-wave applications
Tuesday, December 15, 11:00 a.m. – 12:00 p.m.
Nadine Collaert, imec
Scott Johnson, GLOBALFOUNDRIES

11:00 a.m.

17.1 Portable Multi-Spectral Imaging: Devices, Vertical Integration, and Applications (Invited), Alberto Valdes-Garcia, Petar Pepeljugoski, Ivan Duran, Jean-Olivier Plouchart, Mark Yeck, Huijuan Liu, IBM T. J. Watson Research Center

Advances in semiconductor and packaging technologies have downsized sensing devices including visible-domain/IR and mmWave radars. This paper discusses challenges and opportunities associated with portable multi-spectral imaging systems, where data from across the EM spectrum is captured, processed, and displayed simultaneously. A prototype system, experimental data, and potential applications are discussed.

11:10 a.m.
17.2 Millimeter-Wave Band CMOS RF Phased-Array Transceiver IC Designs for 5G Applications (Invited),
H.-C. Park, D. Kang, J. Lee, D. Minn, Y. Aoki, K. Kim, S. Lee, D. Lee, S. Kim, J. Kim, W. Lee, C. Kim, S. Park, J. Park, B. Suh, J. Jang, M. Kim, K. Min, S. Jeon, A.-S. Ryu, Y. Kim, J. H. Lee, J. Son and S.-G. Yang, Samsung Electronics

This paper presents design challenges and solutions for the fifth-generation (5G) phased-array transceiver ICs in millimeter-wave (mm-wave) frequency bands. A 28nm bulk CMOS device technology is selected to integrate multiple RF phased-array elements in a single-chip to achieve high transmitter (TX) EIRP

11:20 a.m.
17.3 Si and SOI CMOS technologies for millimeter wave wireless applications (Invited), Baudouin Martineau, Didier Belot, CEA-Léti

This paper presents an overview of Si and SOI CMOS technologies for millimeter-wave applications. Implementations of CMOS-only, partially depleted and fully depleted SOI technologies are compared for the different blocks constituting an integrated RF system.

11:30 a.m.
17.4 mmWave and sub-THz Technology Development in Intel 22nm FinFET (22FFL) Process, Qiang Yu, Said Rami, James Waldemer, Yunzhe Ma, Vijaya Neeli, Jeffrey Garrett, Guannan Liu, Jabeom Koo, Mauricio Marulanda, Saurabh Morarka, Surej Ravikumar, Yi-Shin Yeh, Jessica Chou, Thomas Brown, Triveni Rane, Carlos Nieva, Dyan Ali, Sameer Joglekar, Mark Armstrong, Jeremy Wahl, Leif Paulson, Georgios Dogiamis, Nathan Monroe*, Ruonan Han*, Hyung-Jin Lee, Hui Fu, Bernhard Sell, Eric Karl, Ying Zhang, Intel Corporation, *Massachusetts Institute of Technology

This paper presents the recent mmWave and subTHz oriented technology developments as part of RF DTCO efforts in Intel 22nm FinFET process. Several BEOL and FEOL improvements have been implemented to enable high performance, innovative mmWave and sub-THz circuits and systems.

11:40 a.m.
17.5 Organic Package Substrates Using Lithographic Via Technology for RF to THz Applications, Aleksandar Aleksov, Georgios Dogiamis, Telesphor Kamgaing, Adel Elsherbini, Johanna Swan, Kristof Darmawikarta, Sai Boyapati, Jack Holloway*, Ruonan Han*, Intel Corporation, *Massachusetts Institute of Technology

RF substrate packages were built using organic dielectric layers and Copper interconnects employing lithographically defined vias as a new manufacturing paradigm. Using this lithographic via technology we demonstrated filters, triplexes, wave-guides, launchers and other structures operating from 1GHz to >300GHz. Measurement results for selected structures are presented and discussed.

11:50 a.m.
17.6 Surface Wave and Lamb Wave Acoustic Devices on Heterogenous Substrate for 5G Front-Ends, Hongyan Zhou, Shibin Zhang, Zhongxu Li, Kai Huang, Pengcheng Zheng, Jinbo Wu, Chen Shen, Liping Zhang, Tiangui You, Lianghui Zhang*, Kang Liu*, Huarui Sun*, Hongtao Xu**, Xiaomeng Zhao, Xin Ou, Chinese Academy of Sciences, *Harbin Institute of Technology, **Fudan University

We demonstrate here the surface wave and Lamb wave acoustic devices on heterogeneous substrate are very promising for high frequency, wideband and high power 5G front-ends. Groups of the acoustic devices with scalable resonances from 2.0 to 4.72 GHz were fabricated on lithium niobate on silicon carbide heterogeneous substrate.

Session 18: Memory Technology - Ferroelectric Memory
Tuesday, December 15, 11:00 a.m. – 12:00 p.m.
Masaharu Kobayashi, The University of Tokyo
Jan van Houdt, imec/KU Leuven

11:00 a.m.
18.1 HfO_2-based FeFET and FTJ for Ferroelectric-Memory Centric 3D LSI towards Low-Power and High-Density Storage and AI Applications (Invited), Masumi Saitoh, Reika Ichihara, Marina Yamaguchi, Kunifumi Suzuki, Keisuke Takano, Keisuke Akari, Kota Takahashi, Yuta Kamiya, Kazuhiro Matsuo, Yuuichi Kamimuta, Kiwamu Sakuma, Kensuke Ota, Shosuke Fujii, Kioxia Corporation

We present the recent progress in HfO_2-based ferroelectric-FET (FeFET) and ferroelectric-tunnel-junction (FTJ) memory. A huge amount of interface trap charges coupled to spontaneous polarization significantly alters the operating model of FeFET irrespective of dopants. Performance and reliability of reinforcement learning with FTJ array are enhanced by improving the FTJ characteristics.

11:10 a.m.
18.2 Implication of Channel Percolation in Ferroelectric FETs for Threshold Voltage Shift Modeling, Yang Xiang, Marie Garcia Bardon*, Ben Kaczer*, Md Nur Kutubul Alam, Lars-Åke Ragnarsson*, Guido Groeseneken, Jan Van Houdt, KU Leuven, *imec

Understanding the ΔV_{TH}-V_G trend in doped-HfO_2-based FeFETs is of crucial interest. We present a domain-percolation-based ferroelectric V_{TH}-shift model. We highlight our semi-quantitative reproduction of the measured ΔV_{TH}-V_G "turnaround" (with traps). Trapping is simulated by Two-State Non-radiative Multi-Phonon model. Based on percolation, we predict that gate length downscaling intrinsically reduces V_{PGM}.

11:20 a.m.
18.3 A Novel Hybrid High-Speed and Low Power Antiferroelectric HSO Boosted Charge Trap Memory for High-Density Storage, Tarek Ali, Konstantin Mertens, Ricardo Olivo, Matthias Rudolph, Sebastian Oehler, Kati Kühnel, David Lehninger, Franz Müller, Maximilian Lederer, Raik Hoffmann, Philipp Schramm, Kati Biedermann, Alireza M. Kia, Joachim Metzger*, Robert Binder*, Malte Czernohorsky, Thomas Kämpfe, Johannes Müller*, Konrad Seidel, Jan Van Houdt**, Lukas M. Eng***, Fraunhofer IPMS Center Nanoelectronic Technologies, *GLOBALFOUNDRIES Fab1 LLC and Co. KG, **imec-ESAT-KU Leuven, ***Institut für Angewandte Physik, Technische Universität Dresden

We report on antiferroelectric (AFE) hybrid charge trap (CT) memory with amplified tunnel oxide field via dynamic AFE hysteresis dipole switching. Memory window (4.5V), switching speed ($<1\mu s$), 10 years

retention, and 10^5 endurance are reported. The HSO/HZO with tailored (FE,AFE) hysteresis are explored for low power and high-speed-boosted CT memory.

11:30 a.m.
18.4 Impact of Oxygen Vacancy Content in Ferroelectric HZO films on the Device Performance, Terence Mittmann, Monica Materano, Sou-Chi Chang*, Ilya V. Karpov*, Thomas Mikolajick, Uwe Schroeder, NaMlab gGmbH, *Intel Corporation

The impact of the oxygen content on Hf0.5Zr0.5O2 based ferroelectric capacitors are evaluated in terms of crystalline phase formation and electrical properties. Outstanding device performance and good reliability are demonstrated for the devices with the highest polar orthorhombic phase fraction which only can be reached for an optimized oxygen content.

11:40 a.m.
18.5 High Speed Memory Operation in Channel-Last, Back-gated Ferroelectric Transistors, Abhishek A. Sharma, Brian S. Doyle, Hui Jae Yoo, I-Cheng Tung, Jack Kavalieros, Matthew Metz, Miriam Reshotko, Prashant Majhi, Tobias Brown-Heft, Yu-Jin Chen, Van H. Le, Intel Corporation, TCAD

Ferroelectric transistors with 76 nm back-gate length with independently processed gate dielectric and channel to minimize parasitic interfaces are demonstrated. A 3σ memory window for fast programing time of 10 ns and instantaneous read-after-write, operating at 1.8 V and having high 10^{12} cycle endurance are presented for the first time.

11:50 a.m.
18.6 Application and Benefits of Target Programming Algorithms for Ferroelectric HfO_2 Transistors, Haidi Zhou, Johannes Ocker, Andrea Padovani*, Milan Pesic*, Martin Trentzsch**, Stefan Dünkel**, Halid Mulaosmanovic***, Stefan Slesazeck***, Luca Larcher*, Sven Beyer**, Stefan Müller, Thomas Mikolajick***, Ferroelectric Memory GmbH, *Applied Materials Inc., **GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, ***NaMlab gGmbH

We demonstrate how a target programming algorithm can improve the FeFET endurance performance and variability for small device geometries. With this technique the V_t can be targeted, which is essential for multilevel cells and in-memory computing. The influence of switching, trapping and detrapping on the target programming algorithm is presented.

Session 19 - Plenary 3: Wednesday, 8:00 a.m.
Symbiosis of Semiconductors, AI and Quantum Computing (Invited), S.W. Hwang, Samsung Advanced Institute of Technology

Session 20: Advanced Logic Technology - Scaling booster
Wednesday, December 16, 9:30 a.m. - 10:30 a.m.
Charles Chu, AMAT
Fadoua Chafik, Qualcomm

9:30 a.m.
20.1 Performance-Power Management Aware State-of –the-Art 5nm FinFET Design(5LPE) with Dual CPP from Mobile to HPC Application, Jaehun Jeong, Young Gun Ko, Kihwang Son, Sung Won Kim, Ju Youn Kim, Jeongmin Choi, Hyungjong Lee, Ho Lee, Sihyung Lee*, Chunghwan Shin*, Heebum Hong, Sung-il Jo, Youngho Lee, Byungha Choi, Jaechul Kim, Minseong Lee, Kyunghoon Jung, Yuri Yasuda-Masuoka, Jong Mil Youn, Gitae Jeong, Samsung Electronics

We demonstrate state of the art 5nm technology (5LPE) having co-optimization process for Dual Critical Poly-Pitch technology to maximize Product Power-Performance-Area by separating both high speed and low power blocks. 5LPE successfully has 10% speed gain or 20% power gain and 0.75x logic area over ourprevious 7nm technology.

9:40 a.m.
20.2 Buried Bitline for sub-5nm SRAM Design, Rahul Mathur, Mudit Bhargava, Shairfe Muhammad Salahuddin*, Pieter Schuddinck*, Julien Ryckaert*, Senthil Annamalai**, Anshul Gupta*, YK Chong, Saurabh Sinha, Brian Cline, Jaydeep Kulkarni***, Arm Inc., *imec, **Synopsys, Inc, ***The University of Texas at Austin

Buried power rails can improve the performance and density of standard cells at sub-5nm nodes. We propose the use of buried rails for bitlines in SRAMs. DTCO is performed using 3D-field solvers and the optimized BBL-SRAM shows gains in accesstime of 11%, writetime of 31%, and dynamic power of 4%.

9:50 a.m.
20.3 Buried Power Rail Scaling and Metal Assessment for the 3 nm Node and Beyond, Anshul Gupta, Olalla Varela Pedreira, Zheng Tao, Hans Mertens, Dunja Radisic, Nicolas Jourdan, Katia Devriendt, Nancy Heylen, Shouhua Wang, Bilal Chehab, Doyoung Jang, Geert Hellings, Farid Sebaai, Christophe Lorant, Lieve Teugels, Antony Peter, BT Chan, Filip Schleicher, Ingrid Demonie, Philippe Marien, Alfonso Sepulveda, Olivier Richard, Nishanth Nagesh, Alicja Lesniewska, Frederic Lazzarino, Julien Ryckaert, Pierre Morin, E. Altamirano-Sanchez, G. Murdoch, J. Bömmels, S. Demuynck, M. H Na, Z. Tőkei, S. Biesemans, E. Dentoni Litta, N. Horiguchi, imec vzw

Buried power rail(BPR)/Via-to-BPR(VBPR) module scaling to FP24nm/CPP42nm is reported. A self-aligned dual-damascene Contact-to-Active(M0A)/VBPR patterning results are presented. W, Ru BPR resistance benchmarking is presented. Impact of pre-clean, TiN liner thickness and via height on measured VBPR resistance, and analysis by TCAD simulations is discussed. W-Ru contact shows excellent EM performance.

10:00 a.m.
20.4 Interconnect scaling challenges, and opportunities to enable system-level performance beyond 30 nm pitch (Invited), Griselda Bonilla, Nicholas Lanzillo, Chao-Kun Hu, Christopher Penny, Arvind Kumar, IBM Research

On-chip interconnects are fundamental to semiconductor functionality. We discuss the scaling challenges and opportunities to continue to offer increased system performance, especially as computing systems become heterogeneous. Continued focus must shift from traditional scaling and device performance towards providing the high interconnectivity needed to support heterogeneous systems.

10:10 a.m.
20.5 Supervia Process Integration and Reliability Compared to Stacked Vias Using Barrierless Ruthenium, V. Vega-Gonzalez, H. Puliyalil, J. Versluijs, A. Leśniewska, O. Varela-Pereira, R. Baert, S. Paolillo, S. Decoster, F. Schleicher, D., Montero, J. Bekaert, E. Kesters, Q. T. Le, C. Lorant, , L. Teugels, N. Heylen, N. Jourdan, Z. El-Mekki, M. van der Veen, I. Ciofi, B. Briggs, J. Heijlen, L. Dupas, B. De-Wachter, E. Vancoille, T. Webers, H. Vats, L. Rynders, M. Cupak, J. Uk-Lee, Y. Drissi, L. Halipre, A.-L. Charley, P. Verdonck, T. Witters, S. V. Gompel, Y. Kimura, I. Demonie, F. Lazzarino, M Ercken, R. Kim, D. Trivkovic, K. Croes, P. Leray, M. Jaysankar, C. Wilson., G. Muroch, Z. Tokei, imec

The integration of high-aspect-ratio supervias into a 3 nm node test vehicle, bypassing an intermediate 21 nm pitch layer, is demonstrated. A maximum aspect ratio of 3.8 was achieved with ~2.4 times lower resistance than the alternative stacked-via configuration. Thermal shock and time-dependent-dielectric-breakdown tests were performed.

10:20 a.m.

20.6 3-D Self-aligned Stacked NMOS-on-PMOS Nanoribbon Transistors for Continued Moore's Law Scaling, Cheng-Ying Huang, Gilbert Dewey, Ehren Mannebach, Anh Phan, Patrick Morrow, Willy Rachmady, I-Cheng Tung, Nicole Thomas, Urusa Alaan, Rajat Paul, Nafees Kabir, Brian Krist, Adedapo Oni, Manan Mehta, Michael Harper, Peter Nguyen, Ryan Keech, Suresh Vishwanath, Kai Loon Cheong, Jun Sung Kang, Aaron Lilak, Matthew Metz, Scott Clendenning, Bob Turkot, Richard Schenker, Hui Jae Yoo, Marko Radosavljevic, J. Kavalieros, Intel Corporation

We demonstrate 3-D self-aligned stacked NMOS-on-PMOS multiple Si-nanoribbon transistors with successful integration of vertically-stacked dual source/drain and dual-metal-gate processes. Both NMOS and PMOS show high performance and superior short-channel control. A functional CMOS inverter is demonstrated with well-balanced voltage-transfer-characteristics. This novel transistor architecture is promising to continue Moore's law scaling.

Session 21: Emerging Device and Compute Technology - Beyond CMOS devices for low power and their physics

Wednesday, December 16, 9:30 a.m. - 10:20 a.m.
Woo-Bin Song, Samsung
Iuliana Radu, imec

9:30 a.m.

21.1 Vertical Gate-All-Around Tunnel FETs Using InGaAs Nanowire/Si with Core-Multishell Structure, Katsuhiro Tomioka, Hironori Gamo, Junichi Motohisa, Takashi Fukui, Graduate School of Information Science and Technology, and Research Center for Integrated Quantum Electronics (RCIQE)

We present vertical gate-all-around (VGAA) tunnel FETs (TFETs) using InGaAs nanowire/Si heterojunction with modulation doped core-multishell NW structures. The VGAA TFETs showed current enhancement with a steep subthreshold slope (SS). The minimum SS was 21 mV/decade and high transconductance efficiency was around 520/V, which exceeded theoretical limit for FETs.

9:40 a.m.

21.2 Vertical NV-NEM Switches in CMOS Back-End-of-Line: First Experimental Demonstration and Array Programming Scheme, Urmita Sikder, Lars Tatum, Ting-Ta Yen*, Tsu-Jae King Liu, University of California, Berkeley, *Texas Instruments

Metallic interconnect layers in a standard 65 nm CMOS back-end-of-line (BEOL) process is leveraged to implement vertical non-volatile nano-electromechanical (NEM) switches. A reconfigurable look-up table (LUT) is implemented with an array of NEM switches utilizing the NV characteristics. A row/column addressing scheme is proposed for programming arrays of NEM switches.

9:50 a.m.

21.3 A Novel Super-Steep Slope (~0.015mV/dec) Gate-Controlled Thyristor (GCT) Functional Memory Device to Support the Integrate-and-Fire Circuit for Spiking Neural Networks, Cheng-Lin Sung, Hang-Ting Lue, Ming-Liang Wei, Shu-Yin Ho, Han-Wen Hu, Pei-Ying Du, Wei-Chen Chen, Chieh (Roger) Lo, Teng-Hao Yeh, Keh-Chung Wang, Chih-Yuan Lu, Macronix International Co., Ltd.

A novel thyristor functional memory is designed for analog neuromorphic circuit with advantages of super-steep slope (S.S.~0.015mV/dec), large ON/OFF ratio (> 5 orders), and tunableV_{th} range (0~3V). It can provide good energy efficiency , good error tolerance to Vth variations, and smaller circuit area than that using conventional CMOS devices.

10:00 a.m.
21.4 Dynamics of $HfZrO_2$ Ferroelectric Structures: Experiments and Models, Taekyong Kim, Jesús del Alamo, Dimitri Antoniadis, Massachusetts Institute of Technology

The switching dynamics of FE-HZO structures and parasitic effects are investigated. No NC behavior is observed in MFM with intrinsic Q-V that is simulated well with a novel dynamic model. In MFIM, for the first time, we report hysteretic NC behavior that can be modeled by a dynamic L-K model.

10:10 a.m.
21.5 All-electrical control of scaled spin logic devices based on domain wall motion, Eline Raymenants, Danny Wan, Sebastien Couet, Laurent Souriau, Arame Thiam, Diana Tsvetanova, Yann Canvel, Asselberghs Inge, Marc Heyns, Dmitri Nikonov*, Ian Young, Stefania Pizzini**, Van Dai Nguyen, Iuliana Radu, imec, *Intel Corporation, **University Grenoble-Alpes

Spin logic devices using domain wall motion offer flexible architectures for logic operation. We demonstrate full electrical control of such nanoscale devices having a novel magnetic tunnel junction and realize a logic AND gate. This 300mm wafer proof-of-concept offers potential solutions for enabling domain wall devices for novel computing architectures.

Session 22: Modeling and Simulation - Novel Channel Materials and Atomistic Modeling
Wednesday, December 16, 9:30 a.m. - 10:30 a.m.
Cory E Weber, Intel
Philippe Blaise, Silvaco

9:30 a.m.
22.1 Applicability of Shockley-Read-Hall Theory for Interface States, Bernhard Ruch, Markus Jech*, Gregor Pobegen, Tibor Grasser*, KAI GmbH, *Institute for Microelectronics TU Wien

Even though the Shockley Read Hall (SRH) model neglects atomic reconfiguration upon charge transitions, it has been successfully used for decades to describe the dynamics of interface states. Using ab initio models of dangling bonds together with non-radiative multi-phonon theory, we explore why the SRH model often gives excellent approximation.

9:40 a.m.
22.2 Design Principle of Channel Material for Oxide-Semiconductor Field-Effect Transistor with High Thermal Stability and High On-current by Fluorine Doping, Hiroki Kawai, Hirokazu Fujiwara, Junji Kataoka, Nobuyoshi Saito, Tomomasa Ueda, Toshiyuki Enda, Takamitsu Ishihara, Keiji Ikeda, Kioxia Corporation

We propose material design guideline of oxide semiconductor FET (OS-FET) by Fluorine doping to InGaZnO based on first-principles calculation, and experimentally demonstrate excellent FET characteristics. Our OS-FET exhibits both high thermal stability and high on-current at optimum F doping concentration which are required for co-integration with Si-CMOS as BEOL transistor.

9:50 a.m.
22.3 Large scale plane-wave based density-functional theory simulations for electronic devices (Invited), Lin-Wang Wang, Meng Ye*, Yueyang Liu*, Xiangwei Jiang*, Lawrence Berkeley National Laboratory, *Institute of Semiconductors, Chinese Academy of Sciences

Large-scale plane-wave density-functional theory simulation is developed to study a wide range of problems in ultra-scaled transistors, including realistic MOS interface full-device simulation with thousands of atoms, dielectric interfacial defects induced charge trapping instability, as well as electron excitation induced interfacial Si-H bond breaking.

10:00 a.m.
22.4 Cold Source Engineering towards Sub-60mV/dec p-Type Field-effect-transistors (pFETs): Materials, Structures, and Doping Optimizations, Qianwen Wang, Pengpeng Sang, Xiaolei Ma, Fei Wang, Wei Wei, Weiqiang Zhang, Yuan Li, Jiezhi Chen, Shandong University

For the first time, we systematically investigate the strategy for designing CS-FETs in terms of CS materials, heterojunction structures, and doping optimization. An excellent SS of 24 mV/dec over four decades of current ($10^{-4} \sim 10^{0}$ μA/μm) is obtained from the p-type MoS_2 -FET with n-doped graphene as the injection source.

10:10 a.m.
22.5 Introducing 2D-FETs in Device Scaling Roadmap using DTCO, Zubair Ahmed, Aryan Afzalian, Tom Schram, Doyoung Jang, Devin Verreck, Quentin Smets, Pieter Schuddinck, Bilal Chehab, Surajit Sutar, Goutham Arutchelvan, Assawer Soussou*, Inge Asselberghs, Alessio Spessot, Iuliana Radu, Bertrand Parvais, Julien Ryckaert, Myunghee Na, imec, *Coventor

2D-FETs, with their superior electrostatic control, are introduced in the device scaling roadmap using an ab-initio calibrated, experimentally validated physical compact model. A DTCO approach is used, highlighting realistic process and device architecture requirements for 2D-FET technology to extend the technology roadmap to multiple advanced nodes.

10:20 a.m.
22.6 A New Surface Potential Based Compact Model for Independent Dual Gate a-IGZO TFT: Experimental Verification and Circuit Demonstration, Jingrui Guo, Ying Zhao, Guanhua Yang, Xichen Chuai, Wenhao Lu*, Dongyang Liu, Qian Chen, Xinlv Duan, Shijie Huang, Yue Su, Di Geng, Nianduan Lu, Tao Cui *, Jin Jang**, Ling Li, Ming Liu, IMECAS, *Chinese Academy of Sciences, **Kyung Hee University

For the first time, we proposed a surface potential-based compact model of the independent Dual Gate a-IGZO TFTs, where percolation conduction, trap-limited conduction and variable rang hopping transport theories in the extended and localized states are both considered via Schroder method.

Session 23: Power Devices and Systems - Reliability and robustness in Wide Band Gap devices
Wednesday, December 16, 9:30 a.m. - 10:30 a.m.
Gerhard Prechtl, Infineon Technologies Austria AG
Marina Antoniou, University of Warwick

9:30 a.m.
23.1 E-mode *p*-GaN Gate HEMT with *p*-FET Bridge for Higher V_{TH} and Enhanced V_{TH} Stability,

Mengyuan Hua, Junting Chen, Chengcai Wang, Ling Liu, Lingling Li, Junlei Zhao, Zuoheng Jiang, Jin Wei*, Li Zhang**, Zheyang Zheng**, and Kevin J. Chen**, Southern University of Science and Technology, *Peking University, **The Hong Kong University of Science and Technology

A novel *p*-GaN gate HEMT featuring a normally-on *p*-FET bridge connecting source and gate has been demonstrated on the commercial GaN-on-Si platform. The *p*-FET-bridge HEMT allows tuning V_{TH} in a wide-range without degrading subthreshold swing. Stable V_{TH} is also achieved while retaining the gate metal/p-GaN Schottky junction and its advantages.

9:40 a.m.
23.2 1.2 kV Vertical GaN Fin JFETs with Robust Avalanche and Fast Switching Capabilities, Jingcun Liu, Ming Xiao, Yuhao Zhang, Subhash Pidaparthi*, Hao Cui*, Andrew Edwards*, Lek Baubutr*, Wolfgang Meier*, Charles Coles*, Cliff Drowley*, Virginia Polytechnic Institute and State University, *NexGen Power Systems, Inc.

This work, for the first time, demonstrates a 1.2 kV, 4 A, normally-off vertical GaN fin-channel JFET. The device shows one of the highest Baliga's figure-of-merits and demonstrates the first avalanche robustness in all vertical GaN transistors, as well as ~10 ns rise/fall time in 600V/4A switching.

9:50 a.m.
23.3 Dynamic Breakdown Voltage of GaN Power HEMTs, Ruizhe Zhang, Joseph Kozak, Qihao Song, Ming Xiao, Jingcun Liu, Yuhao Zhang, Virginia Polytechnic Institute and State University, Virginia Polytechnic Institute and State University

This work develops a new method to measure the transient breakdown voltage (BV) in ultra-short pulses, and for the first time, measures the BV of 600/650-V GaN power HEMTs down to 25 ns pulses. New BV behaviors and ruggedness are found for GaN HEMTs and the physics are fully revealed.

10:00 a.m.
23.4 Gate Oxide Instability and Lifetime in SiC MOSFETs under a Wide Range of Positive Electric Field Stress, Munetaka Noguchi, Akihiro Koyama, Toshiaki Iwamatsu, Hiroyuki Amishiro, Hiroshi Watanabe, Naruhisa Miura, Mitsubishi Electric Corporation

For the first time, we analyzed the electron capture in SiO_2 under high oxide electric field stress for SiC MOSFETs. The amount of charges injected into gate oxide was found to be a criterion for threshold voltage drift. Additionally, power-law model is presented to express the lifetime under PBTI testing.

10:10 a.m.
23.5 A Novel Insight on Interface Traps Density (Dit) Extraction in GaN-on-Si MOS-c HEMTs, William Vandendaele, Simon Martin, Marie-Anne Jaud, Alexis Krakovinsky, Laura Vauche, Cyrille Le Royer, Jérôme Biscarrat, Abygael Viey, Romain Gwoziecki, Roberto Modica*, Ferdinando Iucolano*, Marc Plissonnier, Fred Gaillard, CEA-Léti, *STMicroelectronics

This paper aims to investigate the interface traps density (Dit) extraction on MOS gate stacks processed on GaN-on-Si substrates. Systematic CGV (Capacitance-Conductance) measurements coupled with TCAD under different frequencies and temperatures on various Al_2O_3UID-GaN MOS capacitors were carried out to determine limitations of Gp/w method and propose a new one

10:20 a.m.
23.6 Carbon-related pBTI degradation mechanisms in GaN-on-Si E-mode MOSc-HEMT, Abygael Viey, William Vandendaele, Marie-Anne Jaud, Louis Gerrer, Xavier Garros, Jacques Cluzel, Simon

Martin, Alexis Krakovinsky, Jérôme Biscarrat, Romain Gwoziecki, Marc Plissonnier, Fred Gaillard, Roberto Modica*, Ferdinando Iucolano*, Matteo Meneghini**, Gaudenzio Meneghesso**, Gerard Ghibaudo***, CEA LETI, *STMicroelectronics, **University of Padova, ***University Grenoble-Alpes

We showed that pBTI degradation involves C_N and Al_2O_3 trap populations close to Al_2O_3/GaN interface. The CET-map approach enabled V_{TH} drifts modelling and trap populations study. The temperature-dependent CET-maps analysis gives an E_a=0.8-0.9eV related to C_N traps, and a range between 0.7 and 1.5eV ascribed to an Al_2O_3 defects band.

Session 24: Memory Technology - Emerging memory (PCRAM/RRAM/MRAM)
Wednesday, December 16, 11:00 a.m. – 12:00 p.m.
Huai-Yu Cheng, Macronix/IBM
Etienne Nowak, CEA-LETI

11:00 a.m.
24.1 Advanced Technology and Systems of Cross Point Memory (Invited), Al Fazio, Intel Corporation

Cross point memories are ideally suited to fill computer memory hierarchy gaps of memory capacity-cost and storage performance. System innovations exploiting the capability of 3D XPoint based cross point memory challenge historical notions of separate semantics of memory and storage, significantly boosting system performance.

11:10 a.m.
24.2 High Density Embedded PCM Cell in 28nm FDSOI Technology for Automotive Micro-Controller Applications, F. Arnaud, P. Ferreira, F. Piazza, A. Gandolfo, P. Zuliani, P. Mattavelli, E. Gomiero, G. Samanni, J. Jasse, C. Jahan*, J.P. Reynard, R. Berthelon, O. Weber, A.Villaret, B. Dumont, J.C. Grenier, R. Ranica, C. Gallon, C. Boccaccio, A. Souhaite*, L. Desvoivres*, D. Ristoiu, L. Favennec, V. Caubet, S. Delmedico, N. Cherault, R. Beneyton, S. Chouteau, P.O.Sassoulas, L. Clement, P. Boivin, D. Turgis, F. Disegni, J.L. Ogier, X. Federspiel, O. Kermarrec, M. Molgg , A.Viscuso , R. Annunziata, A. Maurelli, P. Cappelletti, E. Ciantar, STMicroelectronics, *CEA-LETI

Enhanced 28nm FDSOI-PCM solution using Bipolar Junction Transistor selector co-integrated with triple gate oxide devices for automotive microcontroller designs. Leveraging FDSOI substrate, Super-STI scheme was developed enabling 0,019um2 PCM cell. Automotive grade-0 reliability criteria were achieved on 16MB, including soldering temperature with wide reading window after 250K writing at 165°C.

11:20 a.m.
24.3 First Demonstration of OxRRAM Integration on 14nm FinFet Platform and Scaling Potential Analysis towards Sub-10nm Node, Xiaoxin Xu, Jie Yu, Tiancheng Gong, Jianguo Yang, Jiahao Yin, Da Nian Dong, Qing Luo, Jing Liu, Zhaoan Yu, Qi Liu, Hangbing Lv, Ming Liu, Chinese Academy of Sciences

The OxRRAM integrated at 14nm FinFET platform was demonstrated. The scalability potential towards 10nm and beyond was analysis by considering the programing voltage, current and stability factors. As an attempt, a design rule and array architecture was proposed to implement the OxRRAM on 5nm FinFET platform.

11:30 a.m.

24.4 Demonstration of narrow switching distributions in STT-MRAM arrays for LLC applications at 1x nm node, Eric Edwards, Guohan Hu, Stephen Brown, Chris D'Emic, Matthias Gottwald, Pouya Hashemi, Hyunsung Jung, Juhyun Kim, Gen Lauer, Janusz Nowak, Jonathan Sun, Thitima Suwannasiri, Philip Trouilloud, Seonghoon Woo, Daniel Worledge, IBM-Samsung MRAM Alliance, IBM TJ Watson Research Center

We demonstrate STT-MRAM arrays achieving 2.8e-10 WER performance for 3 ns write duration at 40 nm MTJ diameter. The write voltage distribution at a WER of 1e-6 is 3.7% for W0 and 4.5% for W1, sufficient to meet the write voltage distribution requirement for LLC applications at 1x nm nodes.

11:40 a.m.
24.5 High-density SOT-MRAM technology and design specifications for the embedded domain at 5nm node, Mohit Gupta, Manu Perumkunnil, Kevin Garello, Siddharth Rao, Farrukh Yasin, Gouri Sankar Kar, Arnaud Furnemont, imec

SOT-MRAM offers the possibility to realize ultra-high-speed Non-Volatile-memory technology without endurance issues. We explore different bit-cell architectures to deduce the most optimum solutions. Our projections shows HP-SOT-MRAM can achieve Read/Write (RD/WR) frequency ≈1.05/0.71GHz with 40% bit-cell area-reduction (compare-to 122-SRAM), HD-SOT can achieve RD/WR frequency ≈1.1/0.45GHz with 37.5% area-reduction (compare-to 111-SRAM).

11:50 a.m.
24.6 High-Performance Shape-Anisotropy Magnetic Tunnel Junctions down to 2.3 nm, Butsurin Jinnai, Junta Igarashi, Kyota Watanabe, Takuya Funatsu, Hideo Sato, Shunsuke Fukami, Hideo Ohno, Tohoku University

We show scalability down to 2.3 nm of shape-anisotropy MTJs employing a multilayered ferromagnetic structure, and observe notable device performance increase in data retention and switching at X-nm scale. The results show that shape-anisotropy MTJ provides a route to high-density and high-performance STT-MRAMs in the era of the ultimate scaling.

Focus Session 25: Emerging Device and Compute Technology - Device technologies for cryogenic electronics
Wednesday, December 16, 11:00 a.m. – 12:20 p.m.
Uygar Avci, Intel
Jin Cai, TSMC

11:00 a.m.
25.1 CMOS Cryo-Electronics for Quantum Computing (Invited), Jan Craninckx, Anton Potocnik, Bertrand Parvais*, Alexander Grill**, Subramanian Narasimhamoorthy, Steven Van Winckel, Steven Brebels, Massimo Mongillo, Ruoyu Li, Bogdan Govoreanu, Iuliana Radu, imec, *also with VUB, **also with KULeuven

To enable performant quantum computers, classical interface electronics must be integrated closer to the milli-Kelvin qubits. This paper presents recent state-of-the-art in cryo-electronics research, shows how nanoscale CMOS technology is well suited for this task when properly modeled, and discusses a 4K superconducting dispersive readout circuit and a mK RF-multiplexer.

11:10 a.m.
25.2 Cryo-CMOS Interfaces for Large-Scale Quantum Computers (Invited), Fabio Sebastiano, Jeroen van Dijk, Pascal 't Hart, Bishnu Patra, Job van Staveren, Xiao Xue, Carmina García Almudever,

Giordano Scappucci, Menno Veldhorst, Lieven Vandersypen, Andrei Vladimirescu, Stefano Pellerano, Masoud Babaie, Edoardo Charbon, Delft University of Technology, Institut Superieur d'Electronique de Paris, UC Berkeley, Intel, EPFL

Cryogenic CMOS (cryo-CMOS) is a viable technology for the control interface of the large-scale quantum computers able to address non-trivial problems. In this paper, we demonstrate state-of-the-art cryo-CMOS circuits and systems for such application and we discuss the challenges still to be faced on the path towards practical quantum computers.

11:20 a.m.
25.3 Cryo-CMOS Compact Modeling (Invited), Christian Enz, Arnout Beckers, Farzan Jazaeri, EPFL

This paper highlights some of the challenges faced for the modeling of MOSFET devices for operation at cryogenic temperature with a special focus on the threshold voltage and the subthreshold swing which are key for the compact model to scale correctly with temperature from room temperature down to cryogenic temperature.

11:30 a.m.
25.4 Chip Design for Future Gravitational Wave Detectors (Invited), Filip Tavernier, Alberto Gatti, Ciana Barretto, ESAT-MICAS KU Leuven

Advanced gravitational wave detectors have to operate under extreme conditions of temperature and/or radiation. In this paper, we discuss the limitations of existing device models required for the design of custom chips for these systems. Specific limitations are highlighted for the Einstein Telescope and LISA design cases.

11:40 a.m.
25.5 A Low-Power CMOS Quantum Controller for Transmon Qubits (Invited), Joseph Bardin, University of Massachusetts, Amherst and Google

Large-scale quantum computers will require scalable control electronics, which may have to operate at temperatures as low as 4 K. We review the design and characterization of a control IC for use with transmon qubits, including a series of quantum control experiments and a discussion of future work.

11:50 a.m.
25.6 III-V HEMTs for Cryogenic Low Noise Amplifiers (Invited), Jan Grahn, Eunjung Cha, Arsalan Pourkabirian, Jörgen Stenarson*, Niklas Wadefalk*, Chalmers University of Technology, *Low Noise Factory AB

Progress on optimizing the InP HEMT for cryogenic low-noise amplifier operation below 1 mW dc power dissipation, of interest for qubit readout electronics, is reported. We also report on how to electrically stabilize the cryogenic two-finger InP HEMT making it possible to design cryogenic low-noise amplifiers up to mm-wave.

12:00 p.m.
25.7 Superconductive Single Flux Quantum Logic Devices and Circuits: Status, Challenges, and Opportunities (Invited), Massoud Pedram, University of Southern California

With switching speeds in hundreds of GHz and energy dissipation of 10^{-19} Joules per JJ transition, single flux quantum (SFQ) circuits can provide the speed and energy efficiency for beyond-Exascale

computing. This article provides a review of the basic SFQ technology and reports recent advances in SFQ optimizations using qPALACE.

12:10 p.m.
25.8 Phonon blocked junction refrigerators for cryogenic quantum devices (Invited), Mika Prunnila, vtt

Refrigeration is an important enabler of quantum technology. Bulky cryostats are utilized in reaching sub-1K regime required by many quantum devices and miniaturized cooling solutions would revolutionize the field. Here, we investigate the performance limits of phonon blocked semiconductor-superconductor junction refrigerators, which could provide a viable route to such miniaturization.

Session 26: Sensors, MEMS, and Bioelectronics - Sensors and Advanced materials for Microsystems
Wednesday, December 16, 11:00 a.m. – 11:50 a.m.
Rakesh Kumar, Skyworks
Tatsuo Nakagawa, Hitachi, Ltd.

11:00 a.m.
26.1 Sub-10mK-Resolution Thermal-Bolometric Integrated FET-Type Sensors Based on Layered Bi_2O_2Se Semiconductor Nanosheets, Qifeng Cai, Shuo Liu, Minzhi Du*, Lei Xu, Chunyan Zhao, Congwei Tan, Teng Tu, Kun Zhang*, Hailin Peng, Xing Zhang, Ming Li, Ming He, Ru Huang, Peking University, *Donghua University

We fabricated high-sensitivity thermal-bolometric integrated FET-type sensors based on novel layered Bi_2O_2Se semiconductor nanosheets. A record-high temperature resolution of 1.5 mK was attained. Outstanding sensitivity, no hysteresis, and broad-temperature stability were also demonstrated. Furthermore, the stochastic resonance decoupling model was proposed for the first time to extract the coupled signals.

11:10 a.m.
26.2 Functional Metamaterial Devices Enabled by Microsystems (Invited), Xin Zhang, Xiaoguang Zhao*, Boston University and Dept. of Radiology

Metamaterials represent a class of artificially engineered materials, which exhibit unprecedented properties enabled by their constituent subwavelength unit cells. Microsystem technology provides a platform to achieve functional metamaterial devices by covering all requisite processes (fabrication/packaging/system integration). We report our progress in constructing functional devices by integrating metamaterials with microsystems technology.

11:20 a.m.
26.3 Energy Harvesting in the Back-End of Line with CMOS Compatible Ferroelectric Hafnium Oxide, Clemens Mart, Sukhrob Abdulazhanov, Malte Czernohorsky, Thomas Kämpfe, David Lehninger, Konstantinos Falidas, Sophia Eßlinger, Kati Kühnel, Sebastian Oehler, Matthias Rudolph, Maciej Wiatr*, Sabine Kolodinski*, Robert Seidel*, Wenke Weinreich, Lukas M.Eng**, Fraunhofer IPMS Center Nanoelectronic Technologies, *Globalfoundries Fab 1 LLC, ** Technische Universität Dresden

We demonstrate the feasibility of thermal energy recovery in the back end of line employing CMOS-compatible ferroelectric hafnium oxide. Our energy harvesting approach exceeds the efficiency limit of commonly-used thermoelectric materials, without using a heat switch. The abundance in CMOS manufacturing make HfO_2-based ferroelectrics promising candidates for integrated energy harvesting.

11:30 a.m.
26.4 Self-Temperature-Compensated GaN MEMS Resonators through Strain Engineering up to 600 K, Liwen Sang, Huanying Sun, Xunlin Yang*, Tiefu Li**, Bo Shen, Meiyong Liao, National Institute for Materials Science, *Peking University, **Tsinghua University

Intrinsically, MEMS resonators have a large temperature coefficient of frequency (TCF). The present methods for low TCF markedly degraded the quality factors of the resonators. Here, we demonstrate a novel self-temperature-compensated strategy with an ultra-low TCF without losing the quality factors up to 600 K by using elastic strain engineering.

11:40 a.m.
26.5 Highly Sensitive Amplifier Circuit Consisting of Complementary pFET-type and Resistor-type Gas Sensors, Yujeong Jeong, Wonjun Shin, Seongbin Hong, Gyuweon Jung, Jinwoo Park, Dongkyu Jang, Donghee Kim, Dongseok Kwon, Byung-Gook Park, Jong-Ho Lee, Seoul National University

We propose a highly efficient amplifier circuit in which a resistor-type gas sensor is used as a complementary load to convert the sensing current of the FET-type gas sensor into a voltage.

Focus Session 27: Power Devices and Systems - GaN and SiC projections - From device to system integration
Wednesday, December 16, 11:00 a.m. – 12:20 p.m.
Tomas Palacios, Massachusetts Institute of Technology
Mihaela Wolf, Ferdinand-Braun-Institut Berlin

11:00 a.m.
27.1 Planar GaN Power Integration – The World is Flat (Invited), Kevin Chen, Jin Wei, Gaofei Tang, Han Xu, Zheyang Zheng, Li Zhang, Wenjie Song, The Hong Kong University of Science and Technology

Taking advantage of the high-density integration and high-yield process enabled by planar GaN heterojunction transistor technology, GaN power integration is expected to unlock the full potential of GaN power electronics. This paper presents recent progress in integration technology, design, GaN-specific device modeling, with discussion on some future development.

11:10 a.m.
27.2 Progressing -190 °C to +500 °C Durable SiC JFET ICs From MSI to LSI (Invited), Philip Neudeck, David Spry, Michael Krasowski, Liangyu Chen*, Norman Prokop, Lawrence Greer, Carl Chang**, NASA Glenn Research Center, *Ohio Aerospace Institue, **Vantage Partners LLC

This invited paper describes prototype SiC JFET integrated circuit (IC) and packaging technology that has produced arguably the most harsh-environment durable electronics ever demonstrated. Recent on-going work focused on upscaling this “go anywhere” IC capability from MSI to large-scale integration (LSI) prototype via benchmark memory ICs is described.

11:20 a.m.
27.3 Advances in Research on 300mm Gallium Nitride-on-Si(111) NMOS Transistor and Silicon CMOS Integration (Invited), Han Wui Then, Marko Radosavljevic, Nachiket Desai, Robert Ehlert, Vinaykumar Hadagali, Kimin Jun, Pratik Koirala, Nicholas Minutillo, Roza Kotlyar, Adedapo Oni, Munzarin Qayyum, Johann Rode, Justin Sandford, Tushar Talukdar, Nicole Thomas, Heli Vora, Patrick Wallace, Mario Weiss, Xiao-Jun Weng, Paul Fischer, Intel Corporation

We demonstrate advances in 300mm GaN-on-Si(111) NMOS by achieving low R_{ON}330Ω-µm; high I $_{D,max}$ =1.7mA/µm; BV_{DS}=90V with excellent R_{ON} 660Ω-µm; record $f_T f_{MAX}$=200/350GHz; industry's best RF-switch R_{ON} C_{off}55fs; highest 28GHz power-amplifier PAE=65%@19.5dBm power. We discuss approaches to GaN-and-Si CMOS integration including poly-silicon CMOS, heterogeneous-epitaxy of GaN and Si(111) CMOS, wafer-to-wafer bonding, and 3D-monolithic Si(100) layer-transfer.

11:30 a.m.
27.4 GaN Power ICs: Reviewing Strengths, Gaps, and Future Directions (Invited), Olivier Trescases, Samantha Murray, Wan Lin Jiang, Mohammad Shawkat Zaman, University of Toronto

This paper reviews monolithic GaN integration for power ICs, focusing on current technological capabilities. We highlight opportunities for integrating low-voltage circuits alongside power devices, supporting converter operation. Simulations and experimental results from the imec 200V GaN-on-SOI and ON Semiconductor 650V GaN-on-Si processes provide quantitative insights for digital and analog circuitry.

11:40 a.m.
27.5 Monolithic GaN Power IC Technology Drives Wide Bandgap Adoption (Invited), Dan Kinzer, Navitas

Gallium Nitride power integrated circuits are ramping into high volume and showing unprecedented efficiency, density, and system cost advantages. The technology delivers a complement of scalable devices with models, and a full suite of verification tools. Innovative circuit designs enable complex functions without the benefit of CMOS, bipolars, or diodes.

11:50 a.m.
27.6 Gate Drive Concept for dv/dt Control of GaN GIT-Based Motor Drive Inverters (Invited), Eric Persson, Dana Wilhelm, Infineon Technologies Americas Corp.

This paper outlines how GaN transistors can be driven for precise slew-rate control to achieve lowest possible loss, while enabling short circuit safe operating area. This enables the integration of motor and drive for improved performance and density in common motor drive applications

12:00 p.m.
27.7 Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems "How to Handle a Double-Edged Sword (Invited), Johann Kolar, Jon Azurza Anderson, S. Miric, Michael Haider, Mattia Guacci, Michael Antivachis, Grayson Zulauf, David Menzi, Pascal Samuel Niklaus, Johann Minibock, Panteleimon Papamanolis, Gwendolyn Rohner, Neha Nain, Davide Cittanti*, Dominik Bortis, ETH Zurich, *Politecnico di Torino

Latest research results on three-phase WBG inverter systems with full-sinusoidal output voltage filtering are described. A new soft-switching modulation scheme for two-level inverters is introduced. Furthermore, a new Figure-of-Merit for determining maximum multi-level bridge-leg efficiency is defined and low-voltage GaN and Si devices are comparatively evaluated.

12:10 p.m.
27.8 A 16 kV PV Inverter Using Series-Connected 10 kV SiC MOSFET Devices (Invited), Rolando Burgos, Dong Dong, Xiang Lin, Lakshmi Ravi, Virginia Polytechnic Institute and State University

Panel Discussion

Thursday, December 17, 7:30 – 9:00 AM

What can electronics do to help solve grand societal challenges?

Following a year of global upheaval and acute challenges, this panel discussion will reflect on the place of electronics and the semiconductor industry in the world. It will bring together experts from across science and technology to discuss future directions for microelectronics and explore the role technology can play in addressing grand societal challenges and creating a more sustainable and equitable future. It will also consider the challenges involved in attracting the best students and how electronics education needs to evolve in order to suit the needs of the future. For 2020, we have partnered with the journals Nature and Nature Electronics to bring you this unique panel discussion.

Moderator: Ed Gerstner, Director of Journal Policy & Strategy, Springer Nature and Chair, Springer Nature Sustainable Development Goals Programme

Session 28: Memory Technology - 3D memories and selectors for novel applications
Thursday, December 17, 9:30 a.m. - 10:30 a.m.
Qiwei Ren, Xi'an UniIC Semiconductors Co., Ltd.
Sabina Spiga, CNR-IMM, via C. Olivetti 2, Agrate Brinza (MB)

9:30 a.m.
28.1 Anti-ferroelectric $Hf_xZr_{1-x}O_2$ Capacitors for High-density 3-D Embedded-DRAM, Sou-Chi Chang, Nazila Haratipour, Shriram Shivaraman, Tobias Brown-Heft, Jason Peck, Chia-Ching Lin, I-Cheng Tung, Devin Merrill, Huiying Liu, Che-yun Lin, Fatih Hamzaoglu, Matthew Metz, Ian Young, Jack Kavalieros, UygarAvci, Intel Corporation 3-D anti-ferroelectric $Hf_xZr_{1-x}O_2$ capacitors are demonstrated for eDRAM by showing (i) 10ns read/write operations, (ii) maximum operating voltage less than 1.8V, (iii) retention much longer 1ms, and (iv) endurance reaching 10^{12} cycles at 80C. Mechanisms behind endurance fatigue are discussed, and a novel architecture toward ultra-high density eDRAM is presented.

9:40 a.m.
28.2 Capacitor-less, Long-Retention (>400s) DRAM Cell Paving the Way towards Low-Power and High-Density Monolithic 3D DRAM, Attilio Belmonte, Hyungrock Oh, Nouredine Rassoul, Gabriele Luca Donadio, Jerome Mitard, Harold Dekkers, Romain Delhougne, Subhali Subhechha, Adrian Chasin, Michiel Van Setten, Luka Kljucar, Ming Mao, Harinarayanan Puliyalil, Murat Pak, LieveTeugels, Diana Tsvetanova, Kaustuv Banerjee, Laurent Souriau, Zsolt Tokei, Ludovic Goux, Gouri Sankar Kar, imec

We report for the first time a fully 300-mm stacking-compatible capacitor-less DRAM cell with >400s retention time by integrating two IGZO-TFTs in a 2T0C configuration. To achieve that, we optimize the single IGZO-TFT by engineering the materials surrounding the IGZO layer, resulting in optimal Vth reproducibility in a scaled device.

9:50 a.m.
28.3 Double-Gate W-Doped Amorphous Indium Oxide Transistors for Monolithic 3D Capacitorless Gain Cell eDRAM, Huacheng Ye, Jorge Gomez, Wriddhi Chakraborty, Samuel D Spetalnick*, Sourav Dutta, Kai Ni, Arijit Raychowdhury**, Suman Datta, University of Notre Dame, *Georgia Institute of Technology, **Rochester Institute of Technology

We demonstrate IWO double-gate transistors with 50nm channel length exhibiting subthreshold slope of 73mV/dec, record ID,SAT of 550µA/µm and high on-off ratio> 1x1012. We demonstrate IWO FET based capacitorless 2T gain cell embedded DRAM ideal for monolithic 3D integration exhibiting retention time 1s and 300ms at 25C and 85C respectively.

10:00 a.m.
28.4 Highly-stable (< 3% fluctuation) Ag-based Threshold Switch with Extreme-low OFF Current of 0.1 pA, Extreme-high Selectivity of 10^9 and High Endurance of 10^9 Cycles, Writam Banerjee, Ilya V. Karpov*, Ashish Agrawal*, Seonghun Kim, Seungwoo Lee, Sangmin Lee, Donghwa Lee, Hyunsang Hwang, Pohang University of Science and Technology, *Intel corporation

We demonstrate driving parameters to control the hybrid-filament in Ag-based threshold switching devices with extremely low OFF current (0.1 pA), extremely high selectivity 10^9 with stable threshold voltage (< 3% fluctuation), high endurance 10^9 with stable steep subthreshold slope ~ 1 mV/dec, and high device-yield.

10:10 a.m.
28.5 Monolithic 3D+-IC Based Massively Parallel Compute-in-Memory Macro for Accelerating Database and Machine Learning Primitives, Akshay Krishna Ramanathan, Srivatsa Srinivasa, Je-Min Hung, Chun-Ying Lee, Cheng-Xin Xue, Sheng-Po Huang, F.-K. Hsueh, Chang-Hong Shen, Jia Min Shieh, Wen Kuan Yeh, Mon-Shu Ho, Hariram Thirucherai Govindarajan, Jack Sampson, Meng-Fan Chang, Vijaykrishnan Narayanan, Pennsylvania State University, National Tsing Hua University, Taiwan Semiconductor Research Institute, National Applied Research Laboratories, National Chung Hsing University

This paper demonstrates Monolithic 3D+-IC based Compute-in-Memory (CiM) Macro performing massively parallel beyond-Boolean operations targeting database and machine learning applications. The proposed CiM technique supports data filtering, sorting, and sparse matrix-matrix multiplication (SpGEMM) operations. Our system exhibits up to 272x speedup and 151x energy savings compared to the ASIC baseline.

10:20 a.m.
28.6 A Machine-Learning-Resistant 3D PUF with 8-layer Stacking Vertical RRAM and 0.014% Bit Error Rate Using In-Cell Stabilization Scheme for IoT Security Applications, Jianguo Yang, Dengyun Lei, Deyang Chen, Jing Li**, Haijun Jiang, Qingting Ding*, Qing Luo*, Xiaoyong Xue**, Hangbing Lv*, Xiaoyang Zeng**, Ming Liu*, Zhejiang Lab, *Institute of Microelectronics of the Chinese Academy of Sciences, **Fudan University

A 3-dimensional vertical RRAM PUF with an in-cell stabilization scheme to improve both cost efficiency and reliability was proposed. The PUF brings excellent randomness with $8F^2$/bit and equivalent $1F^2$/bit for 8-layer stacking. The bit error rate is improved by >68X with the help of the in-cell stabilization circuit.

Session 29: Emerging Device and Compute Technology - Emerging technologies for in-memory and artificial intelligence
Thursday, December 17, 9:30 a.m. - 10:30 a.m.
Jean Anne C. Incorvia, University of Texas at Austin
Stefano Ambrogio, IBM Research

9:30 a.m.
29.1 Assessment and optimization of Analog-in-Memory-Compute architectures for DNN processing (Invited), Pouya Houshmand, Stefan Cosemans, Linyan Mei, Ioannis Papistas*, Debjyoti Bhattacharjee*, Peter Debacker*, Arindam Mallik*, Diederik Verkest*, Marian Verhelst, KU Leuven, *imec

This paper assesses the benefits of Analog-in-Memory-Compute (AiMC) solutions at the accelerator level, showing that AiMC can improve efficiency significantly, yet only when it's co-optimized with the memory hierarchy. The paper provides design guidelines to maximally exploit the opportunities in AiMC technology, and gives an outlook towards emerging memory technologies.

9:40 a.m.
29.2 Ultra Low Power Flexible Precision FeFET based Analog In-memory Computing, Taha Soliman, Franz Müller*, Tobias Kirchner, Tudor Hoffmann*, Heba Ganem, Emil Karimov*, Tarek Ali*, Maximilian Lederer*, Chirag Sudarshan**, Thomas Kämpfe*, Andre Guntoro, Norbert When**, Robert Bosch GmbH, *Fraunhofer IPMS, **TU Kaiserslautern

This paper presents an efficient crossbar design and implementation intended for analog compute-in-memory (ACiM) acceleration of artificial neural networks based on FeFET technology. The mixed signal blocks reduce the device-to-device variation and offer low area, low power and high throughput. The ACiM achieves a record peak performance of 13714 TOPS/W.

9:50 a.m.
29.3 A Scalable Design of Multi-Bit Ferroelectric Content Addressable Memory for Data-Centric Computing, Chao Li, Franz Müller*, Tarek Ali*, Ricardo Olivo*, Mohsen Imani**, Shan Deng***, Cheng Zhuo, Thomas Kämpfe*, Xunzhao Yin, Kai Ni***, Zhejiang University, *Fraunhofer IPMS Center Nanoelectronic Technologies, **University of California, Irvine, ***Rochester Institute of Technology, Zhejiang University

We propose a novel scalable and ultra-compact multi-bit CAM design based on 2FeFET1T structure. Successful functionality verification of a CAM cell and array on 2-bit FeFET and statistical verification of sufficient sensing margin for an 1x32 CAM array are demonstrated. Density and performance are greatly improved compared with SRAM CAM.

10:00 a.m.
29.4 Precision of synaptic weights programmed in phase-change memory devices for deep learning inference, S. R. Nandakumar, Irem Boybat, Jin-Ping Han*, Stefano Ambrogio**, Praneet Adusumilli*, Robert L. Bruce*, Matthew J. BrightSky*, Malte Rasch*, Manuel Le Gallo, Abu Sebastian, IBM Research Europe, *IBM T. J. Watson Research Center, **IBM Research-Almaden

We theoretically estimate and experimentally confirm the limits of achievable precision of states programmed in analog resistance memory-based in-memory computing hardware. Further, we demonstrate significant accuracy retention improvements on CIFAR-10, CIFAR-100, and PTB benchmarks by tuning the time of feedback when programming weights on PCM-based DNN inference hardware.

10:10 a.m.
29.5 3D RRAMs with Gate-All-Around Stacked Nanosheet Transistors for In-Memory-Computing, Sylvain Barraud, Mona Ezzadeen, Daphnée Bosch, Théophile Dubreuil, Nicollo Castellani, Valentina Meli, Jean-Michel Hartmann, Mehdi Mouhdach, Bernard Previtali, Bastien Giraud, Jean-philippe Noel, Gabriel Molas, Jean-Michel Portal*, Etienne Nowak, FrançoisAndrieu, CEA, Leti, University Grenoble Alpes, *

This work proposes a novel 1T1R 3D RRAM architecture combining two emerging technologies (GAA stacked-NS transistors/RRAMs). We show that a proper engineering of junctionless-GAA-transistors results in compliance currents of 150µA which are high enough to address OxRAM-arrays. This architecture, which offers a high write/read parallelism, can be leveraged for IMC.

10:20 a.m.

29.6 Fully Memristive SNNs with Temporal Coding for Fast and Low-power Edge Computing, Xumeng Zhang, Zuheng Wu, Jikai Lu*, Jinsong Wei, Jian Lu*, Jiaxue Zhu*, Jie Qiu**, Rui Wang*, Kaihua Lou*, Yongzhou Wang*, Tuo Shi*, Chunmeng Dou*, Dashan Shang*, Qi Liu, MingLiu, Fudan University, *Chinese Academy of Sciences, **Zhejiang Laboratory

In this work, for the first time, we demonstrate a LIF neuron based on a NbO_x device to meet the requirements for the hardware implementation of temporal coding SNNs. Then, we further experimentally demonstrated a fully memristive temporal coding SNN (256 × 5) to classify the Olivetti face patterns.

Session 30: Modeling and Simulation - Quantum and In-memory Computing
Thursday, December 17, 9:30 a.m. - 10:10 a.m.
Jing Guo, University of Florida
Bin Gao, Tsinghua University

9:30 a.m.

30.1 Challenges and perspectives in the modeling of spin qubits (Invited), Y. M. Niquet*, L. Hutin[2], B. Martinez Diaz, B. Venitucci, J. Li, V. Michal, G. Troncoso Fernández-Bada, H. Jacquinot[2], A. Amisse, A. Apra, R. Ezzouch, N. Piot, E. Vincent, C. Yu, S. Zihlmann, B. Brun-Barrière, V. Schmitt, E. Dumur, R. Maurand, X. Jehl, M. Sanquer, B. Bertrand[2], N. Rambal*, H. Niebojewski*, T. Bedecarrats*, M. Cassé*, E. Catapano*, P. A. Mortemousque*, C. Thomas*, Y. Thonnart*, G. Billiot*, A. Morel*, J. Charbonnier*, L. Pallegoix*, D. Niegemann**, B. Klemt**, M. Urdampilleta**, V. El Homsy**, M. Nurizzo**, E. Chanrion**, B. Jadot**, C. Spence**, V. Thiney**, B. Paz**, S. de Franceschi, M. Vinet*, T. Meunier**, University of Grenoble Alpes, CEA, *CEA-Leti, **CNRS

We discuss the status, challenges and perspectives of “Quantum CAD” for the design and exploration of spin qubits. We highlight the similarities and differences with conventional TCAD for micro-electronics, and focus on design, physics and variability of silicon-on-insulator qubits as an illustration.

9:40 a.m.

30.2 A Scalable One Dimensional Silicon Qubit Array with Nanomagnets, George Simion, Fahd Mohiyaddin, Ruoyu Li, Mohamed Shehata, Nard Dumoulin-Stuyck, Asser Elsayed, Florin Ciubotaru, Stefan Kubicek, Julien Jussot, BT Chan, Tsvetan Ivanov, Clement Godfrin, Alessio Spessot, Philippe Matagne, Bogdan Govoreanu, Iuliana Radu, imec

We present a scalable design and operation methodology for 1-D spin qubit arrays with nanomagnets . Each qubit in the array is independently addressable, with single and 2-qubit quantum gate fidelities that exceed 99% in the presence of realistic noise and fabrication errors. The scheme can be extended to 2D.

9:50 a.m.

30.3 Ab initio modelling framework for Majorana transport in 2D materials: towards topological quantum computing, Youseung Lee, Tarun Agarwal, Mathieu Luisier, ETH Zurich

We present an ab-initio modelling framework to simulate Majorana transport in 2D semiconducting materials, paving the way for topological qubits based on 2D nano-ribbons. By combining density-functional-theory and quantum transport calculations, we show that the signature of Majorana Zero-energy Modes (MZM) can be found in PbI₂and WSe₂ nano-ribbons.

10:00 a.m.

30.4 Benchmarking Monolithic 3D Integration for Compute-in-Memory Accelerators: Overcoming ADC Bottlenecks and Maintaining Scalability to 7nm or Beyond, Xiaochen Peng, Wriddhi Chakraborty*, Ankit Kaul, Wonbo Shim, Muhannad S Bakir, Suman Datta*, Shimeng Yu, Georgia Institute of Technology, *University of Notre Dame

We presents a benchmark framework of M3D integrated CIM accelerators. To overcome ADC overhead and scaling limitations in eNVM, we partition the circuit modules in hybrid tech-nodes across two stacked tiers. With versatile BEOL-compatible transistors and thermal profile for M3D integration, we reveal the benefits of a hybrid M3D architecture.

Session 31: Reliability of Systems and Devices - Reliability of Emerging Technologies
Thursday, December 17, 9:30 a.m. - 10:30 a.m.
Xavier Garros, CEA-LETI
Zhong Chen, University of Arkansas

9:30 a.m.
31.1 Reliability and Performance of CMOS-Compatible Multi-Level Graphene Interconnects Incorporating Vias, Kunjesh Agashiwala, Junkai Jiang, Chao-Hui Yeh, Kamyar Parto, Dujiao Zhang, Kaustav Banerjee, University of California, Santa Barbara and Xi'an Jiatong University

This work engineers a solid-phase CMOS-compatible growth technique to yield large-area multilayer graphene (MLG) on both dielectric and metallic substrates, and subsequently demonstrates subtractive-etching enabled multi-level MLG interconnects with vias. We show that these structures offer excellent reliability and performance characteristics, making them an ideal candidate for sub-10 nm nodes.

9:40 a.m.
31.2 Atomic Hydrogen Exposure to Enable High-Quality Low-Temperature SiO_2 with Excellent pMOS NBTI Reliability Compatible with 3D Sequential Tier Stacking, Jacopo Franco, Jean-Francois de Marneffe, Anne Vandooren, Yosuke Kimura, Laura Nyns, Zhicheng Wu, Al-Moatasem Bellah El-Sayed**, Markus Jech**, Dominic Waldhoer, Dieter Claes, Hiroaki Arimura, Lars-Åke Ragnarsson, Valeri Afanas'ev*, Andre Stesmans*, Naoto Horiguchi, Dimitri Linten, Tibor Grasser**, Ben Kaczer, imec, *imec/KU Leuven, ** TU Wien

Sequential stacking of CMOS tiers requires low thermal budget processes. In SiO_2 IL's grown at reduced temperatures, we show that unrelaxed interface strain induces excessive formation of hydroxyl-E'defects. We demonstrate atomic hydrogen exposure to passivate these defects at low temperature (100-300°C) and match the reliability of a 900°C oxide.

9:50 a.m.
31.3 Sub-ns Polarization Switching in 25nm FE FinFET toward Post CPU and Spatial-Energetic Mapping of Traps for Enhanced Endurance, Hagyoul Bae, Seung Geol Nam, Taehwan Moon, Yunseong Lee, Sanghyun Jo, Duk-Hyun Choe, Sangwook Kim, Kwang-Hee Lee, Jinseong Heo, Samsung Advanced Institute of Technology

We report sub-ns polarization switching in highly scaled 25nm ferroelectric FinFET with $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric gate stack for high performance CPU application for the first time. Also, low-frequency noise characteristics were newly adopted for resolving spatial and energetic distribution of traps at HZO/SiO_2 interface, SiO_2Si channel interface, and in bulk oxide.

10:00 a.m.

31.4 High-radiation Hardness 4H-SiC Transimpedance Amplifier featuring Stable Offset-voltage for Analog Sensors in Nuclear Power Plants, Masahiro Masunaga, Ryoh Kuwana, Keizo Egawa*, Hiromitsu Hayashi*, Tetsufumi Kawamura, Isao Hara, Digh Hisamoto, Daisuke Ryuzaki, Hitachi, Ltd., *Hitachi High-Tech Solutions Corporation

We developed a 4H-SiC transimpedance amplifier (TIA) with high radiation hardness featuring high offset-voltage stability. Regarding the SiC-TIA operation, the instability of offset-voltage caused by local charge trap was critical, and we demonstrated that by reducing surface electric field, both reliable amplifier performance and high radiation hardness can be achieved.

10:10 a.m.
31.5 Secure 3D CMOS Chip Stacks with Backside Buried Metal Power Delivery Networks for Distributed Decoupling Capacitance, Hiroki Sonoda, Kazuki Monta, Takaaki Okidono*, Yuuki Araga**, Naoya Watanabe**, Haruo Shimamoto**, Katsuya Kikuchi**, Noriyuki Miura***, Takuji Miki, Makoto Nagata, Kobe University, *ECSEC, **National Institute of Advanced Industrial Science and Technology, ***Osaka University

Secure 3D CMOS chip stacks with backside buried metal (BBM) power delivery routing achieve distributed capacitance of 12.8 nF in the full-chip backside area of 71 mm^2 in a 3.9M-gate 0.13-um CMOS cryptographic chip. Four-tier BBM stack demonstrates 59% dynamic IR drop reduction and 8x suppression of statistical information leakage.

10:20 a.m.
31.6 A Novel Complementary Architecture of One-time-programmable Memory and Its Applications as Physical Unclonable Function (PUF) and One-time Password, W. C. Wang, C. C. Chuang, C. W. Chang, E. R. Hsieh*, H.W. Chen**, Steve Chung, National Chiao Tung University, *also with National Central University, **UMC

We proposed a novel 2T complementary architecture of one-time-programmable memory (OTP) made in a foundry logic CMOS chip. It was then used to realize the PUF (Physical unclonable function), and the combination with the AI deep learning algorithm to provide a one-time password capability.

Focus Session 32: Advanced Logic Technology - Future interconnect technology
Thursday, December 17, 11:00 a.m. – 12:10 p.m.
Dechao Guo, IBM Research
Rinus Lee, GlobalFoundries

11:00 a.m.
32.1 The Overview of Current Interconnect Technology Challenges and Future Opportunities (Invited), Ming-Han Lee, Winston Shue, Taiwan Semiconductor Manufacturing Company

This paper examines the challenges facing current copper damascene interconnect and the possible technologies to extend it. In addition, various novel materials are reviewed for their potential application in future interconnect.

11:10 a.m.
32.2 Inflection points in interconnect research and trends for 2nm and beyond in order to solve the RC bottleneck (Invited), Zs. Tőkei, V. Vega, G. Murdoch, M. O'Toole, K. Croes, R. Baert, M. Van der Veen, C. Adelmann, J.P. Soulié, J. Boemmels, C. Wilson, S.H. Park, K. Sankaran, G. Pourtois, J. Sweerts, S. Paolillo, S. Decoster, M. Mao, F. Lazzarino, J. Versluijs, V. Blanco, M. Ercken, E. Kesters,

Q-T. Le, F. Holsteyns, N. Heylen, L. Teugels, K. Devriendt, H. Struyf, P. Morin, N. Jourdan, S. Van Elshocht, I. Ciofi, A. Gupta, H. Zahedmanesh, K. Vanstreels, M.H. Na, imec

Interconnect options will be introduced and reviewed targeting tight pitch metal layers at the local levels. Examples include hybrid metallization, semi-damascene interconnects as well as potential new conductor materials.

11:20 a.m.
32.3 Narrow interconnects: The most conductive metals (Invited), Daniel Gall, Atharv Jog, Tianji Zhou, Rensselaer Polytechnic Institute

In situ transport measurements on epitaxial metal layers (Cu, Co, Ru, Rh, Ir) in combination with first-principles simulations are used to evaluate the resistivity scaling and determine the most conductive metals in the limit of narrow interconnect lines, considering the bulk resistivity, electron mean free path and grain boundary scattering.

11:30 a.m.
32.4 Topological Semimetals for Scaled Back-End-Of-Line Interconnect Beyond Cu (Invited), Ching-Tzu Chen, Utkarsh Bajpai*, Nicholas Lanzillo**, Chuang-Han Hsu***, Hsin Lin***, Gengchiau Liang^, IBM T. J. Watson Research Center, *also with University of Delaware, **IBM Research, ***Academia Sinica, ^National University of Singapore

The resistance bottleneck in metal-interconnect scaling calls for new interconnect materials. This paper explores topological semimetals as a potential solution. After reviewing the desirable properties of topological semimetals for back-end-of-line (BEOL) interconnects, we use CoSi as an example to demonstrate the decreasing resistance-area product with scaling and provide material-search guidelines.

11:40 a.m.
32.5 Staggered Metallization with Air gaps for Independently Tuned Interconnect Resistance and Capacitance (Invited), Kevin L Lin, Mark A Anders, Robert Bristol, Michael Christenson, Giselle Elbaz, Brandon Holybee, Himanshu Kaul, Mauro Kobrinsky, Ram Krishnamurthy, Miriam Reshotko, Hui Jae Yoo, Intel Corporation

A process that improves interconnect resistance and capacitance is presented. Test structures patterned in geometries that lower wiring RC are fabricated, and electrical measurements are compared to simulated values from materials and geometry. Circuit studies with representative examples were performed to quantify the benefit in microprocessor performance and power.

11:50 a.m.
32.6 From Interconnect Materials and Processes to Chip Level Performance: Modeling and Design for Conventional and Exploratory Concepts (Invited), Victor Huang, Da Eun Shim, H. Simka*, Azad Naeemi, Georgia Institute of Technology, *Samsung Semiconductor Inc.

We survey device and interconnect scaling trends in literature. We evaluate copper interconnect and via advancements at the 7nm technology node and compare it with ruthenium interconnects. Despite advancements in copper, we show ruthenium is viable at 7nm, sooner than projections, owing largely to 5X improvement in ruthenium via resistance.

12:00 p.m.
32.7 Silicon compatible optical interconnect and monolithic 3-D integration (Invited), Krishna Saraswat, Stanford University

Device scaling paradigm is threatened by the limits of interconnects. It is imperative to examine alternate interconnect schemes: optical interconnects and 3-D heterogeneous integration and explore possible advantages of lower power dissipation, improved bandwidth, and signal latency. This talk will focus on important integration technologies for integration on Si platform.

Session 33: Optoelectronics, Displays, and Imaging Systems - Emerging Optoelectronic Devices and Systems
Thursday, December 17, 11:00 a.m. – 12:00 p.m.
Chiao Liu, Facebook
Becky Peterson, University of Michigan

11:00 a.m.
33.1 Low power consumption and high resolution 1280X960 Gate Assisted Photonic Demodulator pixel for indirect Time of flight, Y. Ebiko, H. Yamagishi, K. Tatani, H. Iwamoto, Y. Moriyama, Y. Hagiwara, S. Maeda, T. Murase, T. Suwa, H. Arai, Y. Isogai, S. Hida*, S. Kameda*, T. Terada*, K. Koiso*, F. T Brady**, S. Han**, A. Basavalingappa**, T. Michiel***, T. Ueno***, Sony Semiconductor Solutions Corporation, * Sony Semiconductor Manufacturing Corporation, ** Sony Electronics Inc. Image Sensor Design Center, ***Sony Depth Sensing Inc.

A 3.5um square 1.2M pixel indirect time of flight sensor achieves 18,000e- full well capacity and 32% quantum efficiency with diffraction structure. Low power consumption is also achieved, due to low resistance Cu-Cu connection wiring. These device architectures enable high resolution and wide dynamic range 3D depth sensing.

11:10 a.m.
33.2 A 2.8 µm Pixel for Time of Flight CMOS Image Sensor with 20 ke- Full-Well Capacity in a Tap and 36 % Quantum Efficiency at 940 nm Wavelength, YongHun Kwon, Sungyoung Seo, Sunghyuck Cho, Sung-Ho Choi, Taeun Hwang, Youngchan Kim, Young-Gu Jin, Youngsun Oh, Min-Sun Keel, Daeyun Kim, Myunghan Bae, Yeomyung Kim, Seung-Chul Shin, SunJu Hong, Seok-HaLee, Ho Woo Park, Yitae Kim, Kyoungmin Koh, JungChak Ahn, Samsung Electronics

A 2.8µm 4-tap global shutter pixel has been realized for a compact and high-resolution time of flight (ToF) CMOS image sensor. 20,000 e- of full-well capacity (FWC) per a tap is obtained by employing a MOS capacitor. 36% of quantum efficiency (QE) 86 % of demodulation contrast (DC) are achieved.

11:20 a.m.
33.3 Fundamental Challenges in Augmented Reality Display Technology (Invited), Matt Colburn, Facebook Reality Labs, Facebook Inc

Many consider augmented reality to be the next leap in the information revolution. Fundamentally, it will transform all aspects of our lives enabled by new interface modalities. The first step to bringing augmented reality to life is creating a great display.

11:30 a.m.
33.4 Enhanced light outcoupling from OLEDs by suppressing guided modes formation using an ultrathin flexible transparent conductor, ChangYeong Jeong, Yong-bum Park, Jay Guo, University of Michigan

We introduce ultrathin copper-seeded silver film to completely eliminate waveguide modes and enhance outcoupling efficiency of OLEDs. The structure was designed to below the cutoff thickness of waveguide

modes, leading to theoretical maximum EQE of 76.1% that is higher than any other theoretical values reported previously without increasing fabrication steps.

11:40 a.m.
33.5 Low Voltage, High Brightness CMOS LEDs, Jin Xue, Jaehwan Kim, Alexandra Mestre, Kian Ming Tan*, Daniel Chong*, Sandipta Roy*, Hao Nong*, Khee Yong Lim*, Dodd Gray, Kramnik Daniel, Amir Atabaki, Elgin Quek*, Rajeev Ram, Massachusetts Institute of Technology, *Globalfoundries Singapore Pte., Ltd.

A high-brightness infrared LED with emission intensity over 40 mW/cm^2 at 1020 nm is demonstrated at below 2.5 Volt of forward-bias operation for a vertical silicon p-n junction realized in an open-foundry CMOS process. We also demonstrate a complete chip-to-chip optical interconnect utilizing only silicon CMOS devices.

11:50 a.m.
33.6 Gigahertz Large-Area-Electronics RF Switch and its Application to Reconfigurable Antennas, Can Wu, Yue Ma, Suresh Venkatesh, Yoni Mehlman, Sigurd Wagner, James Sturm, Naveen Verma, Princeton University

Large-Area-Electronics (LAE) are extending to broader applications, especially requiring large and conformal form factors. A critical limitation is the TFT low performance, restricting to applications in megahertz range. This work presents ZnO-TFT-based gigahertz RF switches, and their use in reconfigurable antennas, where LAE enables radiative apertures of unprecedented size.

Focus Session 34: Microwave, Millimeter Wave, and Analog Technology - Technologies enabling 5G and beyond
Thursday, December 17, 11:00 a.m. – 12:00 p.m.
Miguel Urteaga, Teledyne
Frédéric Gianesello, ST-Microelectronics

11:00 a.m.
34.1 Millimeter-wave Multi-antenna/MIMO Techniques for 5G NR Base-stations (Invited), Rui Hou, Bo Göransson, Ericsson AB

The architecture and technology choices for millimeter-wave multi-antenna 5G NR base stations are discussed from a communication system perspective.

11:10 a.m.
34.2 A Deep Learning Enabled Universal DPD System (Invited), Chih-Lin I, Yingchao Lin, Guizhen Wang, China Mobile Research Institute

Facing the severe power consumption and energy efficiency challenges in 5G, a novel DPD solution enabled by deep learning and big data is proposed. The architecture, mechanism and deployment strategy along with its advantages are presented. This is a flexible system suitable for various wireless network architectures and application scenarios.

11:20 a.m.
34.3 Millimeter-Wave CMOS Phased-Array Transceiver for 5G and Beyond (Invited), Kenichi Okada, Tokyo Institute of Technology

In this presentation, a 28-GHz phased-array transceiver and 300-GHz transceiver realized by 65nm CMOS will be introduced, which are designed for 5G and beyond. The talk concludes with a discussion on future directions of millimeter-wave wireless communication, based on Shannon and Friis equations.

11:30 a.m.
34.4 PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G communications (Invited), Pascal Chevalier, Frederic Gianesello, Andrea Pallotta, Joao Azevedo Goncalves, Guillaume Bertrand, Julien Borrel, Laurence Boissonnet, Edoardo Brezza, Michel Buczko, Elodie Canderle, Didier Celi, Sebastien Cremer, Nicolas Derrier, Cheikh Diouf, CedricDurand, Franck Foussadier, Patrice Garcia, Nicolas Guitard, Alain Fleury, Alexis Gauthier, Olivier Kermarrec, Jerome Lajoinie, Charles-Alex Legrand, Victor Milon, Frederic Monsieur, Yannick Mourier, Dorothee Muller, STMicroelectronics

While 5G wireless networks are currently deployed around the world, preliminary research activities have begun to look beyond 5G and conceptualize 6G standard. In this paper, we review the development of PD-SOI CMOS and SiGe BiCMOS technologies addressing 5G RF Integrated Circuits (RFICs) and their evolutions for 6G.

11:40 a.m.
34.5 Heterogeneous Integration for High Frequency RF Applications (Invited), Augusto Gutierrez-Aitken, Northrop Grumman Space Systems

Heterogeneous integration (HI) for RF has become an important task for many applications. Several factors need to be considered to select a suitable approach, including active semiconductor technologies, performance, materials for interposers, the HI method and interface, cost, yield, and last but not least the overall reliability of the integration

11:50 a.m.
34.6 Innovative Smart Cut™ Piezo On Insulator (POI) Substrates for 5G acoustic filters (Invited), Eric Butaud, Sylvain Ballandras*, Marie Bousquet**, Alexis Drouin, Brice Tavel, Isabelle Huyet, Alexandre Clairet, Isabelle Bertrand, Aymen Ghorbel, Alexandre Reinhardt**, Soitec, *TEMIS Innovation, **Univ. Grenobles Alpes, CEA-Léti

5G standards implementation drive significant challenges at acoustic filter level and requires innovative solutions. Promising approach relies in Surface Acoustic Waves technology combined with a thin LiTaO3 piezoelectric crystal layer bonded on Silicon substrate so called POI-substrate but suffers from volume manufacturing solution.

Session 35: Sensors, MEMS, and Bioelectronics - Chemical and Biochemical Sensors
Thursday, December 17, 11:00 a.m. - 11:50 a.m.
Steve Kim, Air Force Research Labs, USAF
Gaëlle Lissorgues, University Gustave Eiffel, ESYCOM Lab, ESIEE

11:00 a.m.
35.1 Chemical Sensing in Aqueous Media by Organic TFTs (Invited), Tsuyoshi Minami, Institute of Industrial Science, The University of Tokyo

We have focused on organic thin-film transistors (OTFTs) as platforms for chemical sensor devices. The extended gate-type OTFTs functionalized with natural or artificial molecular recognition materials were fabricated to achieve the detection of targets in complete aqueous media. The OTFTs have enabled to detect environmentally and/or biologically important

11:10 a.m.

35.2 Extended-Gate FET cortisol sensor for stress disorders based on aptamers-decorated graphene electrode: Fabrication, Experiments and Unified Analog Predictive Modeling, Luca Capua, Shokoofeh Sheibani, Sadegh Kamaei Kahmaei, Junrui Zhang*, Adrian Ionescu, EPFL, *Xsensio SA

We report a novel cortisol biosensor, with a unified predictive calibrated model. The sensor shows linearity over a wide concentration range, high voltage (14.7mV/dec.) and current (80%) sensitivity, small drift, low LOD of 0.2nM, and great selectivity.We propose the first unified compact analog predictive calibrated model for cortisol FET sensors.

11:20 a.m.

35.3 Efficient Improvement of Sensing Performance Using Charge Storage Engineering in Low Noise FET-type Gas Sensors, Wonjun Shin, Seongbin Hong, Yujeong Jeong, Gyuweon Jung, Jinwoo Park, Dongseok Kwon, Dongkyu Jang, Donghee Kim, Byung-Gook Park, Jong-Ho Lee, Seoul National University

A novel charge storage engineering (CSE) using program/erase (P/E) operation for improving the sensing performance of FET-type gas sensors with floating-gate is proposed for the first time.

11:30 a.m.

35.4 50 nm Gate Length FinFET Biosensor & the Outlook for Single-Molecule Detection, Sybren Santermans, David Barge, Geert Hellings, Carlos Bergfeld Mori***, Konrad Joseph Migacz*, Jens Rip, Valentina Spampinato, Rita Vos, Bert Du Bois, Ashesh Ray Chaudhuri, Joao Martino, Marc Heyns, Simone Severi, WillemVan Roy, Koen Martens, imec, *KULeuven, *also with University of São Paulo,

We report on the smallest silicon FinFETs functioning as biosensors with 13 nm wide fins and 50 nm gate lengths. These electrolytically gated finFETs exhibit a near-ideal subthreshold swing (~65 mV/dec) and a median voltage referred 1/f noise of only ~470 □V2□m2/Hz (at 1Hz, at threshold). Binding biomolecules to the chemically modified gate dielectric surface changes the threshold voltage VT. DNA-PNA hybridization shows a statistically significant signal across all device geometries (50 nm – 10 µm gate length) with a median VT shift of 36 mV for a hybridized 15 base DNA surface density of ~8×1012 cm-2. We obtain a clear signal of 17 mV for a 20 base DNA surface density of ~8×1011 cm-2, which amounts to tens of molecules for a 13 nm wide and 90 nm long device. This is a major improvement compared to our previously reported 250 nm long FETs which picked up ~800 molecules and a significant step forward towards the realization of single molecule sensing with fully integrated silicon FETs. Finally, based on experiment and simulation, we predict single-molecule detection with SNR > 5 to be possible with sub-70 nm finFETs.

11:40 a.m.

35.5 Large-area manufacturable active matrix digital microfluidics platform for high-throughput bio-sample handling, Hanbin Ma, Subao Shi, Kai Jin, Dongping Wang, Siyi Hu, Yang Su*, Yan Zhang*, Jun Li**, Zhe Liu**, Chen Jiang^, Linrun Feng**, Xiaojun Guo^, Arokia Nathan*, Suzhou Institute of Biomedical Engineering and Technology, Chinese Academy of Sciences, *ACXEL Tech Ltd, **Hangzhou Linkzill Technoloy, ***University of Cambridge, ^Shanghai Jiao Tong University

We present an active-matrix digital microfluidics platform for bio-sample handling, which demonstrates extension of the ubiquitous and highly-scalable flat-panel technology from displays to bio-applications. The fabricated chip contains 32 × 32 pixels in an active area of 10 cm², which can be individually or simultaneously addressed.

Career Session

Friday - 8:00 a.m. - 9:00 a.m., Career Session

Tsu-Jae King Liu, Dean and Roy W. Carlson Professor of Engineering, University of California, Berkeley

Heike Riel, IBM Fellow, Head Science & Technology, Lead IBM Research Quantum Europe, IBM Research

Session 36: Memory Technology - Memory devices for in-memory AI computation
Friday, December 18, 9:30 a.m. - 10:30 a.m.
Sangbum Kim, Seoul National University
Qiangfei Xia, University of Massachusetts Amherst

9:30 a.m.
36.1 In-Memory-Searching Architecture Based on 3D-NAND Technology with Ultra-high Parallelism, Po-Hao Tseng, Feng-Ming Lee, Yu-Hsuan Lin, Liang-Yu Chen, Yung-Chun Li, Han-Wen Hu, Yun-Yuan Wang, Chih-Chang Hsieh, Ming-Hsiu Lee, Hsiang-Lan Lung, Kuang-Yeu Hsieh, Keh-Chung Wang, and Chih-Yuan Lu, Macronix International Co., Ltd.

A high speed, low power, low cost in-memory-searching (IMS) architecture based on 3D-NAND technology is demonstrated. Reliability concerns and improvement solutions are discussed. The flexible encoding algorithm and circuit implementations could further improve functionality. ML/NN applications are discussed with successful demonstration. It provides a powerful solution for memory-centric computing systems.

9:40 a.m.
36.2 Unassisted True Analog Neural Network Training Chip, Yasuteru Kohda, Yulong Li, Kohji Hosokawa, Seyoung Kim, Riduan Khaddam-Aljameh*, Zhibin Ren, Paul Solomon, Tayfun Gokmen, Sankeerth Rajalingam, Chris Baks, Wilfried Haensch, Effendi Leobandung, IBM Research, *IBM Research Zurich

We report first RPU analog neural network training chip with analog capacitor weights, where ALL Multiple and Accumulate functions are performed in analog cross-point arrays, and all weights are updated in parallel, without digital emulation assistance. We show MNIST training accuracy of 92.7%, with real run time faster than digital.

9:50 a.m.
36.3 Accelerated Local Training of CNNs by Optimized Direct Feedback Alignment Based on Stochasticity of 4 Mb C-doped $Ge_2Sb_2Te_5$ PCM Chip in 40 nm Node, Yingming Lu, Xi Li*, Longhao Yan, Teng Zhang, Yuchao Yang, Zhitang Song*, Ru Huang, Peking University, *Shanghai Institute of Micro-System and Information Technology, Chinese Academy of Sciences

We demonstrate efficient CNN training by optimized direct feedback alignment replacing layer-by-layer back propagation, where the stochasticity in PCM is exploited to build merged random feedback matrix with reduced hardware cost. Training time/energy consumptions of VGG-16 are reduced by 3×/3.3× compared with hardware-accelerated BP training, with 90% accuracy on CIFAR-10.

10:00 a.m.
36.4 Monolithic 3D Integration of High Endurance Multi-Bit Ferroelectric FET for Accelerating Compute-In-Memory, Sourav Dutta, Huacheng Ye, Wriddhi Chakraborty, Yuan-Chun Luo, Matthew San Jose, Benjamin Grisafe, Abhishek Khanna, Ian Lightcap, Subhash Shinde, Shimeng Yu, Suman Datta, University of Notre Dame, Georgia Institute of Technology

We demonstrate monolithic 3D integration of BEOL IWO-HZO FeFET with FEOL HKMG Si-NMOS using low thermal budget (<400⁰C) processing. We report MW=0.45V in Lg=20nm IWO FeFET with 100ns write speed and >10⁸endurance cycle. We demonstrate 2bit/cell synaptic weight cell that that provides energy-efficiency and density advantage for CIM accelerators.

10:10 a.m.
36.5 High-Density 3D Monolithically Integrated Multiple 1T1R Multi-Level-Cell for Neural Networks, Eduardo Esmanhotto, Laurent Brunet, Niccolo Castellani, Djohan Bonnet, Thomas Dalgaty, Laurent Grenouillet, Denys R B Ly, Carlo Cagli, Christian Vizioz, Nacima Allouti, Fabien Laulagnet, Olivier Gully, Nathalie Bernard-Henriques, Marc Bocquet*, Gabriel Molas, Pascal Vivet, Damien Querlioz**, Jean-Michel Portal*, Subhasish Mitra, François Andrieu, Claire Fenouillet-Beranger, Etienne Nowak, Elisa Vianello, CEA LETI, *CNRS, **Stanford University

We demonstrate, for the first time, a 3D monolithically integrated multiple 1T1R structure storing up to 3.17 bits per RRAM. We study, using a 4 kb 1T1R array, the conductance relaxation after Multi-Level-Cell programming. We show that conductance relaxation is negligible for Neural Networks inference accuracy.

10:20 a.m.
36.6 Analog error correcting codes for defect tolerant matrix multiplication in crossbars, Can Li,*, Ronny Roth**, Cat Graves, Xia Sheng, John Paul Strachan, Hewlett Packard Labs also with *The University of Hong Kong, **also with Technion

We experimentally demonstrate an analog error correction code for in-memory computing. With low hardware overhead, we show the ability to detect and correct both hard and transient errors. As one example, we experimentally recover the MNIST handwritten digit classification accuracy from 73.12% to 97.36% when current noise is injected.

Focus Session 37: Sensors, MEMS, and Bioelectronics - Energy harvesting and wireless power transmission
Friday, December 18, 9:30 a.m. - 10:40 a.m.
Guangyu Xu, University of Massachusetts, Amherst
Stewart Smith, The University of Edinburgh

9:30 a.m.
37.1 High Power Graphene Micro-supercapacitors (Invited), Richard Kaner, Chenxiang Wang, Maher El-Kady, Volker Strauss*, Arie Borenstein**, Mit Muni, Helen Huang, Xueying Chang, Sheng Qu, Kimberly Sung, University of California, Los Angeles, *Max-Planck-Institute of Colloids and Interfaces, **Ariel University

Only a few materials in Micro-supercapacitors(MSCs) are capable of operating at the high frequencies with high power and sufficient stability for long-term operation. By using graphene and its derivatives as electrodes, we demonstrate that MSCs with ultrahigh power density will push further the monolithic integration and smart multifunctional autonomous system-on-a-chip.

9:40 a.m.
37.2 MEMS Vibrational Energy Harvester for IoT Wireless Sensors (Invited), Hiroshi Toshiyoshi, The Univerisity of Tokyo

A MEMS vibrational energy harvester of electrostatic induction type is developed by using a built-in potential produced by the permanent electrical charge or so-called “electrets.” Maximum power of more than 1.2 mW is produced from the environmental vibrations of 0.65 G (1 G = 9.8 m/s²) at 158 Hz.

9:50 a.m.
37.3 High-voltage micro-plasma switch for efficient power management of triboelectric kinetic energy harvesters (Invited), Philippe Basset, Hemin Zhang*, Ahmad Delbani, Naida Hodzic, Armine Karami, Dimitri Galayko**, ESYCOM, University Gutave Eiffel, *ESYCOM, University of Cambridge, **Sorbonne Université

In this abstract, we compare the three main unstable charge-pumps for triboelectric energy generators (TENGs) and we propose to use an autonomous MEMS micro-plasma switch in a Buck DC-DC converter in order to maximized the voltage across the TENG while obtaining a low voltage rectified output without any external control.

10:00 a.m.
37.4 Radiative Wireless Power Transmission: From Indoor to In-Body Applications (Invited), Hubregt Visser, imec netherlands

In this overview paper we will discuss the feasibility of radiative Wireless Power Transfer (WPT). We will look at the power levels available and the consequences for practical use. Miniaturized WPT receivers will find employment in low-power, duty-cycled IoT sensor applications and are candidates for future biomedical implants.

10:10 a.m.
37.5 Wireless Power Transfer for Internet of Things (Invited), Yoshihiro Kawahara, Takuya Sasatani, The University of Tokyo

Cross-disciplinary collaboration can provide insights into the use of new devices and enable new improvements to devices and hardware. This paper presents a case study of a cross-disciplinary design of a wireless power transfer technology system.

10:20 a.m.
37.6 mm-Wave Backscatter frond-end for 5G-IoT/WPT Applications (Invited), Diogo Matos, Ricardo Correia, Nuno Borges Carvalho, Universidade de Aveiro, Sinuta S.A., Instituto Politecnico de Viseau

This paper presents a mm-Wave backscatter front-end for IoT and WPT applications. The proposed circuit is capable of performing low-order modulations with low static and dynamic power consumption, 60fW and 72µW respectively. Also shows a good EVM performance for different the different data rates and input powers tested.

Session 38: Emerging Device and Compute Technology - Beyond Classical Computing - Advancements in Quantum Technology and Stochastic Computing
Friday, December 18, 9:30 a.m. – 10:30 a.m.
Aida Todri-Sanial, LIRMM, University of Montpellier, CNRS
Susanna Reggiani, University of Bologna

9:30 a.m.

38.1 The Wonderful World of Designer Ge Quantum Dots (Invited), I-Hsiang Wang, Po-Yu Hong, Kang-Ping Peng, Horng-Chih Lin, Thomas George, Pei-Wen Li, National Chiao Tung University

Using a coordinated combination of lithographic patterning and self-assembly, size-tunable spherical Ge QDs were controllably placed at designated spatial locations within Si-containing layers. This significant accomplishment has opened up the possibility of creating diverse quantum, photonic, electronic, and sensing devices for practical applications.

9:40 a.m.
38.2 Coupler characterization of superconducting transmons qubits for cross-resonance gate (Invited), Hanhee Paik, Srikanth Srinivasan, Sami Rosenblatt, Jose Chavez-Garcia, Daniela Bogorin, Oblesh Jinka, George Keefe, Dongbing Shao, Jeng-Bang Yau, Markus Brink, Jerry Chow, IBM T. J. Watson Research Center

We characterize two-qubit cross-resonance gates and unintended residual coupling on various coupled qubit arrangements. Capacitive coupling versus resonator coupling are studied on the basis of cross-resonance gate rate and fall-off of non-nearest neighbor coupling. We experimentally extract coupling rates using Hamiltonian tomography methods, and compare with microwave simulations

9:50 a.m.
38.3 A flexible 300 mm integrated Si MOS platform for electron- and hole-spin qubits exploration, Ruoyu Li, Nard Dumoulin-Stuyck, Stefan Kubicek, Julien Jussot, BT Chan, Fahd Mohiyaddin, Asser Elsayed, Mohamed Shehata, George Simion, Clement Godfrin, Yann Canvel, Tsvetan Ivanov, Ludovic Goux, Bogdan Govoreanu, Iuliana Radu, imec and KU Leuven

We report a 300mm process flow for silicon spin qubit integration that produces high volume and uniform devices while allowing on-the-fly design modifications. Fabricated qubits are characterized at cryogenic temperatures, demonstrating well-defined quantum dots, tunable tunnel coupling, and coherent spin operations, which are essential requirements for a large-scale quantum processor.

10:00 a.m.
38.4 Dispersive vs charge-sensing readout for linear quantum registers, Agostino Apra, Alessandro Crippa, Marco Tagliaferri, Jing Li, Rami Ezzouch, Benoit Bertrand, Louis Hutin, Nils Rambal, Edoardo Catapano, Heimanu Niebojewski, Thomas Bedecarrats, Maud Vinet, Matias Urdampilleta*, Tristan Meunier*, Yann-Michel Niquet, Etienne Dumur, Marc Sanquer, Xavier Jehl, Romain Maurand, Silvano De Franceschi, CEA-IRIG, CEA-Léti, *CNRS Institut Néel, University of Grenoble Alpes

We present recent progress in the implementation of scalable schemes for spin qubit readout. Two schemes based on rf gate reflectometry are compared. We demonstrate single-shot charge sensing with a fidelity of 97% in 5 μs. Finally, we propose a scalable architecture for linear qubit registers relying on charge-sensing readout.

10:10 a.m.
38.5 Cryogenic Benchmarks of Embedded Memory Technologies for Recurrent Neural Network based Quantum Error Correction, Panni Wang, Xiaochen Peng, Wriddhi Chakraborty*, Asif Khan, Suman Datta*, Shimeng Yu, Georgia Institute of Technology, *University of Notre Dame

We propose implementing the quantum error correction circuitry with compute-in-memory (CIM) based recurrent neural network accelerator at 4K. We develop a device-to-system modeling framework that calibrate the transistor parameters and interconnect with experimental data at cryogenic temperature. Then we benchmark the QEC circuitry with SRAM technologies and optimize its energy-delay-product.

10:20 a.m.
38.6 A High-performance and Calibration-free True Random Number Generator Based on the Resistance Perturbation in RRAM Array, Bohan Lin, Bin Gao, Yachuan Pang, Wenqiang Zhang, Jianshi Tang, He Qian, Huaqiang Wu, Tsinghua University

A RRAM TRNG utilizing the resistance perturbation is demonstrated, achieving 230 Mbps throughput. An unique calibration-free feature is derived from the switching asymmetry and nonlinearity of RRAM, contributing to high randomness. Excellent reliability is validated under various testing conditions. Finally, this TRNG is successfully applied to a stochastic computing system.

Session 39: Reliability of Systems and Devices - Aging and Reliability of Memory-based circuits and devices
Friday, December 18, 9:30 a.m. - 10:30 a.m.
Paolo Pavan, Università di Modena e Reggio Emilia
Georgios Konstadinidis, Google

9:30 a.m.
39.1 Machine Learning for Circuit Aging Simulation (Invited), Elyse Rosenbaum, Jie Xiong, Alan Yang, Maxim Raginsky, Zaichen Chen, University of Illinois at Urbana Champaign

High-quality open source software for behavioral model optimization facilitates a behavioral approach to the modeling of aged circuits. A continuous-time formulation of a recurrent neural network (RNN) is compatible with transient circuit simulation. For any reasonable input, the model should produce an output response that is physically plausible.

9:40 a.m.
39.2 A Novel PUF Using Stochastic Short-Term Memory Time of Oxide-Based RRAM for Embedded Applications, Jianguo Yang, Deyang Chen*, Qingting Ding*, Jinbei Fang*, Xiaoyong Xue, Hangbing Lv*, Xiaoyang Zeng*, Ming Liu*, Zhejiang Lab, *Institute of Microelectronics of the Chinese Academy of Sciences, **Fudan University

We demonstrated a PUF utilizing the stochastic short-term memory time of RRAM. The RRAM PUF is capable of regenerating >10²⁰ times after 10 years@115^oC and the BER remains <0.08% at the temperature of up to 115^oC for the read voltage of 0.1-0.7V. The energy efficiency is 0.19 pJ/bit.

9:50 a.m.
39.3 Novel Concept of Hardware Security in Using Gate-switching FinFET Nonvolatile Memory to Implement True-Random-Number Generator, W. Y. Yang, B. Y. Chen, C. C. Chuang, E. R. Hsieh*, K. S. Li**, Steve Chung, National Chiao Tung University, *National Central University, **TSRI

We use a gate-switching resistance memory to implement the TRNG (True random number generator). First, a resistance memory, RG-FinFET, was built . Then, a TRNG was developed from drain current variation of RG-FinFET. It passed all NIST tests, even at high temperature, and demonstrated high throughput as high as 62.5Mbps.

10:00 a.m.
39.4 Hydrogen Absorption Method Using HfOx in Crystalline In-Ga-Zn Oxide FETs for NVM Applications, Toshikazu Ono, Yuichi Yanagisawa, Yoshihiro Komatsu, Takeshi Aoki, Yasuhiro Jimbo,

Shunich Ito, Yasumasa Yamane, Naoki Okuno, Hitoshi Kunitake, Hiroki Komagata, Shinya Sasagawa, Shunpei Yamazaki, Semiconductor Energy Laboratory Co., Ltd

In order to stabilize the electrical characteristics of an In–Ga–Zn oxide FET (OSFET), control of hydrogen inside the OSFET is essential. We have found that the modified HfOx film absorbs hydrogen, and confirmed that the OSFET using the HfOx can dramatically suppress the variation of the threshold voltage.

10:10 a.m.
39.5 Interplay of Switching Characteristics, Cycling Endurance and Multilevel Retention of Ferroelectric Capacitor, Jae Hur, Panni Wang, Zheng Wang, Gihun Choe, Nujhat Tasneem, Asif Khan, Shimeng Yu, Georgia Institute of Technology

Herein, we experimentally characterized 10 nm-thick plasma-enhanced-atomic-layer-deposited HZO capacitors at the pristine, woken-up and fatigued states. The interplay of polarization switching speed, pulse cycling and multilevel retention is explored under variables such as device size and electric field. Woken-up state is found to be the most vulnerable to retention degradation.

10:20 a.m.
39.6 Deep Insights into the Failure Mechanisms in Field-cycled Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Film: TDDB Characterizations and First-Principles Calculations, Wei Wei, Weiqiang Zhang, Fei Wang, Xiaolei Ma, Qianwen Wang, Pengpeng Sang, Xuepeng Zhan, Yuan Li, Lu Tai, Qing Luo, Hangbing Lv*, Jiezhi Chen, Shandong University, Institute of Microelectronics, *Chinese Academy of Sciences

This work aims at studying the failure mechanisms of $Hf_{0.5}Zr_{0.5}O_2$ based ferroelectric memory. By using TDDB measurement and first-principles calculations, the defects profile and the possible formation sites of breakdown paths in the HZO film are addressed. Our research provides guidelines for improving the film quality during the deposition process.

Session 40: Advanced Logic Technology - Advanced Materials and Integration
Friday, December 18, 11:00 a.m. – 12:00 p.m.
Oleg Golonzka, Intel Corporation
Zhao Wang, Facebook

11:00 a.m.
40.1 A Selectively Colorful yet Chilly Perspective on the ^{Highs} and $_{Lows}$ of Dielectric Materials for CMOS Nanoelectronics, Sean King, John Plombon, Jeff Bielefeld, James Blackwell, Shashi Vyas, Ramanan Chebiam, Carl Naylor, David Michalak, Mauro Kobrinsky, Florian Gstrein, Matthew Metz, James Clarke, Rupak Thapa*, Michelle Paquette*, VamseedharaVemuri**, Nick Strandwitz**, Ye Fan***, Marius Orlowski***, Intel corporation, *University of Missouri - Kansas City, **Lehigh University, ***Virginia Tech

The remarkable advancement of CMOS electronics over the past two decades has been greatly aided by dielectric scaling across the permittivity spectrum. This paper describes how new innovations beyond permittivity scaling will allow both the extension of Moore's law and usher in an array of new devices and computational paradigms.

11:10 a.m.
40.2 Wafer-scale integration of double gated WS_2-transistors in 300mm Si CMOS fab, Asselberghs Inge, Quentin Smets, Tom Schram, Benjamin Groven, Devin Verreck, Aryan Afzalian, Goutham

Arutchelvan, Abhinav Gaur, Daire Cott, Thibaut Maurice, Steven Brems, Koen Kennes, Alain Phommahaxay, Emmanuel Dupuy, Dunja Radisic, Jean-Francois de Marneffe, Arame Thiam, Waikin Li, Katia Devriendt, Cedric Huyghebaert, Dennis Lin, Matty Caymax, Pierre Morin, Iuliana Radu, imec

Double gated WS₂-transistors with gate length down to 18 nm are fabricated in a 300mm Si CMOS fab. We built an integration vehicle where impact of each process step can be understood and developed to enhance device performance. The work paves the way towards industrial adoption of 2D materials.

11:20 a.m.
40.3 Switchable NAND and NOR Logic Computing in Single Triple-Gate Monolayer MoS_2 n-FET, Yunyan Chung, Chao-Ching Cheng*, Bo-Kai Kang, Wei-Chen Chueh, Shih-Yun Wang, Chen-Han Chou, Terry Hung, Shin-Yuan Wang, Wen-Hao Chang, Lain-Jong Li*, Chao-Hsin Chien, National Chiao Tung University, *TSMC

Single novel triple-gated monolayer MoS₂ transistor realizes the switchable NAND and NOR computing through top-gate bias (V_{LOW} / V_{HIGH}= 0.75V / 2V). This work demonstrated good logic-gate operation and large ON-OFF ratio modulation, which provide a new perspective in device design for logic and in-memory computing applications.

11:30 a.m.
40.4 First Demonstration of Ultrafast Laser Annealed Monolithic 3D Gate-All-Around CMOS Logic and FeFET Memory with Near-Memory-Computing Macro, F.-K. Hsueh, Je-Min Hung*, Sheng-Po Huang*, Yen-Hsiang Huang*, Cheng-Xin Xue*, Chang-Hong Shen, Jia Min Shieh, Wen-Cheng Chiu, Chao-Cheng Lin, Bo-Yuan Chen, Szu-Ching Liu, Shih-Wei Chen, Deng-Yan Niou, Wen-Hsien Huang, Kai-ShinLi, K.-L. Lin, Da-Chiang Chang, Kun-Ming Chen, Guo-Wei Huang, Ci-Ling Pan*, Meng-Fan Chang, Chenming Hu**/***, Wen Kuan Yeh, Taiwan Semiconductor Research Institute, *National Tsing Hua University, **National Chiao Tung University, ***University of California, Berkeley

For the first time, ultrafast laser annealed BEOL gate-all-around transistor and FeFET memory were demonstrated with monolithic 3D near-memory-computing circuit. The GAA MOSFETs employing picosecond laser dopant activation exhibit record-high Ion (nFETs=407 uA/um, pFETs=345 uA/um). The BEOL FeFETs memory exhibits large memory window ΔV_{th} = 1.2V and >10⁶ cycle endurance.

11:40 a.m.
40.5 10-nm Channel Length Indium-Tin-Oxide transistors with I_{on} = 1860 μA/μm, G_m = 1050 μS/μm at V_{ds} = 1 V with BEOL Compatibility, Shengman Li, Chengru Gu, Xuefei Li, Ru Huang, Yanqing Wu, Peking University, Huazhong University of Science and Technology

BEOL compatible 10-nm Channel Length Indium-Tin-Oxide transistors exhibit record-high I_{on} = 1860 μA/μm, G_m = 1050 μS/μm at V_{ds} = 1 V The on/off ratio exceeds 10^{10} with ultra-low leakage current of 40 fA/μm. Record high f_T 20 GHz and f_{max} of 13 GHz have also been demonstrated.

11:50 a.m.
40.6 Crystal-Orientation-Tolerant Voltage Regulator using Monolithic 3D BEOL FinFETs in Single-Crystal Islands for On-Chip Power Delivery Network, Po-Tsang Huang*, Yu-Wei Liu,Kuan-Fu Lai, Yun-Ping Lan, Tzung-Han Tsai, Bo-Jheng Shih, Ping-Yi Hsieh*,Chih-Chao Yang*, Chang-Hong Shen*, Jia-Min Shieh*, Da-Chiang Chang*, Kuan-Neng Chen, Wen-Kuan Yeh*, and Chenming Hu**

National Chiao Tung University, *Taiwan Semiconductor Research Institute, **University of California, Berkeley

A single-crystal-island technique is demonstrated for Monolithic 3D BEOL-FinFET circuits. BEOL-FinFETs fabricated in the designed single-crystal-Si-islands exhibit excellent electrical performance and low intra-island variability. Crystal-orientation-tolerant voltage regulator is further proposed by allocating PG-cells among multiple-Si-islands, and 42% power noise suppression can be achieved.

Focus Session 41: Memory Technology DTCO of advanced logic and memory
Friday, December 18, 11:00 a.m. – 12:10 p.m.
Nuo Xu, TSMC
Keiji Ikeda, KIOXIA

11:00 a.m.
41.1 DTCO Launches Moore's Law Over the Feature Scaling Wall (Invited), Victor Moroz, Xi-Wei Lin, Plamen Asenov, Deepak Sherlekar, Munkang Choi, Luca Sponton, Larry Melvin, Jaehyun Lee, Binjie Cheng, Alessandro Nannipieri, Joanne Huang, Scott Jones*, Synopsys, Inc., *IC Knowledge LLC

Pitch scaling began slowing after 10nm node and is expected to practically cease by 1nm node. Despite that, transistor density is expected to continue increasing at a similar pace of 45% density increase per node (or 20% per year) through 1nm node, fueled by increasingly sophisticated DTCO and EDA advances.

11:10 a.m.
41.2 Advanced Node DTCO in the EUV Era (Invited), Andy Wei, Charles Wallace, Mark Phillips, Jonathan Knudsen, Sourav Chakravarty, Manjunath Shamanna, Ruth Brain, Intel corporation

EUV lithography has finally made it into high-volume manufacturing and this has reset the approach to leading-edge DTCO. EUV lithography restores the balance between design optimization for PPA, along with technology optimization for yield and cost. Further rapid improvement in EUV lithography capability is highly anticipated.

11:20 a.m.
41.3 Next-Generation Design and Technology Co-optimization (DTCO) of System on Integrated Chip (SoIC) for Mobile and HPC Applications (Invited), Yi-Kan Cheng, Frank Lee, Ming-Fa Chen, Jonathan Yuan, Tze-Chiang Huang, Kuo-Ji Chen, Chuei-Tang Wang, Chih-Lin Chen, Chung-Hao Tsai, Douglas Yu, TSMC

This paper demonstrates the DTCO of system on integrated chip (SoIC) for mobile and HPC applications. The new DTCO includes overall die partitioning, die integration, and interconnect. In this paper, two prototypes of stacking CPU and memory dies are demonstrated with 15% performance gain and 30% average point-to-point distance reduction.

11:30 a.m.
41.4 DTCO including Sustainability: Power-Performance-Area-Cost-Environmental score (PPACE) Analysis for Logic Technologies (Invited), Marie Garcia Bardon, Pieter Wuytens, Lars-Åke Ragnarsson, Gioele Mirabelli, Doyoung Jang, Geert Willems, Arindam Mallik, Alessio Spessot, Julien Ryckaert, Bertrand Parvais, imec, imec / VUB

Design Technology Co-Optimization methodologies and tools make possible to develop early sustainability assessments of logic technologies together with the PPAC metrics. To demonstrate this, we

evaluate the energy and water consumption and greenhouse gas emissions trends from processing logic nodes from iN28 to iN3 with different scaling scenarios.

11:40 a.m.
41.5 Enabling Efficient Design-Technology Interaction by Spec-Driven Extraction Flow (Invited), Huan-Lin Chang, Yutao Ma*, Zhihong Liu*, ProPlus Design Solutions, Inc., *Primarius Technologies Co., Ltd.

We propose a new methodology by adopting technology spec. window and Spec-Driven Extraction Flow (SDEF) to address the inefficiency of the current design-technology co-optimization (DTCO) flow. For the first time, we show that designers could use SDEF to sign off the technology development without the reliance of foundry SPICE models.

11:50 a.m.
41.6 MRAM DTCO and Compact Models (Invited), Jeehwan Song, Jian-Ping Wang, Chris Kim, University of Minnesota

Design-Technology Co-Optimization (DTCO) has become an important design methodology for making early decisions on technology, circuit, and system design parameters. This paper introduces various aspects of DTCO for MRAM development, ranging from SPICE MTJ device models, STT-MRAM power-performance-area evaluation, scalability and variability studies, and novel read and write circuit techniques.

12:00 p.m.
41.7 Enabling Design Technology Co-Optimization of SRAMs through Open-Source Software (Invited), Matthew Guthaus, Hunter Nichols, Jesse Cirimelli-Low, Joseph Kunzler, Bin Wu, University of California, Santa Cruz

OpenRAM is an open-source memory compiler infrastructure that can enable Design Technology Co-Optimization of SRAMs. SRAM DTCO is often plagued by limited access to robust, featured memory compilers whereas OpenRAM can leverage recurring needs of verification, circuits, and tool compatibility to give insight from technology all the way to design.