Integration Technology – From Package Level to Wafer Level Integration

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As 4th industry revolution becomes realization, more sophisticated mobile sets and servers are demanded that, in turn, necessitates advanced device and package technologies. It is apparent that Moore's law has been slowing down and hence is limited to add more functionalities to meet the performance demand. Over the years Chiplet has become the focus of the semiconductor industry as an alternative or complement solution. Considering Chiplet has been discussed in different context for different purposes, this IEDM 2020 Short Course will start by providing some examples in industry talked by several major manufactures, EDA or solution providing companies. Then four important keywords are extracted and addressed in detail from the industry usage of the Chiplet. As one of important keywords, package technology plays a key role in continuing or overcoming the Moore's law. Chiplet, more appropriately Chiplet integration on advanced packaging plartorm, is precisely defined and introduced. That includes 2.xD Silicon/RDL Interposer, 3D vertical chip stacking, and chip partitioning. Physical integration on package platform is not all for Chiplet integration. Die-to-die (D2D) connectivity between Chiplets and its impact on electrical performance will also be discussed. When the Short Course finished, much of advanced package from package integration and wafer level integration is covered.

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