Advanced 3D System Integration Technologies

KC Yee, TSMC

I am KC Yee from TSMC R&D. It is my privilege to have this opportunity to offer an IEDM short course on "Advanced 3D System Integration Technologies". This course aims to give the audience a comprehensive overview on the mainstream 3D system integration technologies (3DSITs) used across high performance computing, networking, smartphones, and consumer electronics. In recent years, chiplets integration has prevailed in semiconductor industry to complement device scaling to co-advance Moore's Law from a system scaling perspective. 3D system integration technologies are main drivers to propel the advancing of system scaling. The outline of the course contains four main sections.

Section I is Introduction, where I will cover some of the fundamental backgrounds regarding 3DSITs

- What is 3D System Integration
- FOM of 3D System Integration
- Why 3D System Integration
- How to Improve FOM of 3D System Integration

In Section II, I will give an overview on 3DSITs from leading foundry, OSATs, and research institutes

In section III, I will cover 3DSITs applications in HPC AI, networking AI, and edge AI

In section IV, I will talk about 3DSITs trends across HPC AI, memory, and mobile AI

Biography: Dr. KC Yee is currently a R&D Director of TSMC advanced Integrated Interconnect & Packaging. He received his Ph.D. degree from the Department of Mechanical Engineering at the University of Texas at Austin. He has 19+ years of semiconductor experiences in advanced IC packaging including optical MEMS, optoelectronics, advanced flip chip, wireless connectivity module, 3D IC, and wafer level fan-out. He is currently a member of SEMI Taiwan PKG & TEST Committee, ECTC Packaging Technologies Sub-committee and EPS Strategic Planning committee. He received China Society of Engineers Distinguished Engineer Award in 2007 and owned/ co-owned 50+ granted US patents