Enablement of Next Generation High Performance NanoSheet Transistors

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As we published in the past, stacked Gate-All-Around Nanosheet technology will replace FinFET for future CMOS logic nodes, as it enables the best device performance and offers the capability to scale the transistor gate length further in the 5NM nodes and beyond. This Short Course will be focused on the enablement of future generations of High Performance Nanosheet transistors. In a first part, we will discuss the best device design for large Weff/footprint and high performance. We will also compare nFET and pFET transport and mobility going from a FinFET device to a Nanosheet transistor architecture. In the second part of my talk, we will be looking at the opportunities and challenges for strain introduction in the channel and thoroughly review how the strain evolves in the Nanosheet channel at the different stages of the FEOL manufacturing process. We will present a novel technique to enable high mobility Nanosheet pFET channel , based on SiGe channel "last" using SiGe cladding epitaxy. This method enables us to obtain a significant amount of 1GPa compressive strain in SiGe that is preserved downstream. We will show the corresponding device electrical advantages in term of hole mobility, performance, Vt modulation and NBTI improvement. Finally, the rest of the presentation will be dedicated to the review of additional additive performance elements, with a special focus on the full bottom dielectric isolation module, critical for subsheet leakage suppression and Ceff improvement. We will also discuss the challenges for multi-Vt patterning on wide NS structures and present additional MOL elements applicable to Nanosheet. These performance elements will enable multiple generations of Nanosheet transistors as we continue device scaling in leading-edge high-performance Logic.

Biography: Nicolas Loubet- *IEEE Member* - Received the B.S. and M.S degrees in physics from Paul Sabatier University, Toulouse (Fr.), in 2000 and 2001. In 2003, he received a high-level Engineering degree in the field of Physics and Microelectronics from the National Institute of Applied Sciences (INSA) in Toulouse, and the PhD degree in the domain of Materials, Technology and Electronic Devices in 2006. From 2003 to 2008, he joined STMicroelectronics Research and Development group in front-end materials and epitaxy where he was engaged in the development of Advanced Epitaxy of Si and SiGe materials, and vapor-phase etching of SiGe for the fabrication of silicon-on-nothing (SON) , Gate-All-Around (GAA) and dielectric isolation transistors. In 2008, he joined the Silicon Technology Research Alliance at IBM Research in Albany, NY and the following years, his research focused on Junction and Strain module engineering for the 20nm, 14nm, 10nm, and 7nm CMOS device nodes using strained SOI and SGOI, SiGe relaxed buffer and ultra-low resistivity SiGe:B and SiC:P for FDSOI with ultra-thin body and box (UTBB) and FinFET devices on Bulk and SOI substrates. In 2015, he became a Senior Engineer and Technical Leader at IBM Research where his research focused on material, process, and device integration of Gate-All-Around devices for 5nm CMOS technology and beyond. In 2017, he became the "face" of IBM for the Nanosheet technology as first author of the IBM 5nm Technology paper and associated worldwide Press Release. Since 2018, he is manager of the Front-End Of Line (FEOL) Process Development team at IBM Research with a focus on materials research and process development for leading edge CMOS logic devices with a special focus on the GAA Nanosheet technology scaling & performance. He has published more than 100 papers in journals and conference proceedings, and the holder of more than 250 patents in the domain of epitaxy, device and process integration