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IRDS at IEDM
PANEL DISCUSSION

IRDS promotes cooperative approach to overcome the end of the semiconductor industry

December 8
6 pm – 8 pm

Hilton San Francisco Union Square,
333 O'Farrell Street, San Francisco, CA

Franciscan Rooms

The IEEE International Roadmap for Devices and Systems (IRDS) is a broad tops-down and bottoms-up roadmap effort to align individualistic research and development efforts throughout the semiconductor industry ecosystem.

This panel intends to lay down the foundation of a rejuvenated, cooperative planning effort among the players of the new electronics industry aimed at overcoming the end of physical scaling by means of the adoption of novel materials, structures, and devices for innovative monolithic and heterogeneous architectures.

These new approaches can complement continued 2D and 3D scaling to ensure the continuation of the semiconductor industry and enable the system integrator community, from conventional computing to new in-memory computing and eventually cryogenic and quantum-inspired devices that go beyond the physical limitation of single-bit manipulation of data.

PANELISTS

Panelists include IRDS Focus Team representatives for More Moore—*Mustafa Badaroglu*, Beyond CMOS—*Matthew Marinella*, Cryogenic Electronics & Quantum Information Processing—*Scott Holmes and Thomas Vogelsang*, and Systems & Architectures—*Kirk Bresniker*

Dr. Mustafa Badaroglu is the Technical Director at Huawei Technologies working on chipset and technology planning of products in the domains of mobile processors, networking, automotive, and wearables. He had various assignments for the execution and management of chipset design from concept to volume production, process technology pathfinding, and design-technology co-optimization. He received his Ph.D. in Electrical Engineering and holds a Master of Industrial Management, both from the Catholic University of Leuven. He holds more than 50 published patents and he has (co)-authored over 100 publications in scientific journals/proceedings. He is the chair of More Moore section in International Roadmap for Devices and Systems (IRDS). He is a senior member of IEEE.

Dr. Matthew Marinella is a Principal Member of the Technical Staff with Sandia National Labs. He is Principal Investigator for Sandia's Nonvolatile Memory Program and leads research projects on neuromorphic, radiation hard, and energy efficient computing. Dr. Marinella chairs the Emerging Memory Devices Section for the IRDS Roadmap Beyond CMOS Chapter, serves on various technical program committees, and is a Senior Member of the IEEE. He received a PhD in electrical engineering from Arizona State University under Dieter K. Schroder in 2008.

Kirk Bresniker is Chief Architect of Hewlett Packard Labs and a Hewlett Packard Enterprise Fellow and Vice President. He joined Labs in 2014 to drive The Machine Research and Advanced Development program, leading teams across Labs and across HPE business units with the goal of demonstrating and evangelizing the benefits of Memory-Driven Computing. Prior to joining Labs, Kirk was Vice President and Chief Technologist in the HP Servers Global Business Unit representing 25 years of innovation leadership. Kirk current holds 28 US and 10 foreign patents in areas of modular platforms and blade systems, integrated circuits, and power and environmental control. He graduated in 1989 Cum Laude from Santa Clara University Humanities Honors program with a BSEE.

Dr. D. Scott Holmes is a former DARPA MTO program manager in the area of superconductor electronics. Holmes also worked at IARPA on the Cryogenic Computing Complexity (C3) program that developed technologies for energy-efficient superconductor computing. Previously he worked at Lake Shore Cryotronics, AFRL, and a decade as a Learning Strategist. Professionally, Holmes is a member of the IEEE Council on Superconductivity representing the Electron Device Society. As a member of the International Roadmap for Devices and Systems (IRDS), he led the establishment of the International Focus Team (IFT) on Cryogenic Electronics and Quantum Information Processing. Holmes received a BSME from MIT and graduate degrees from the University of Wisconsin–Madison.

Dr. Thomas Vogelsang is a Rambus Fellow and member of Rambus Labs. His current research interest is memory for machine learning systems, low power DRAM and in general opportunities to reduce the power of computer systems with a focus on memory including cryogenic memory systems.
He joined Rambus in 2009, first working on low power and 3D DRAM architectures. From 2011 to 2015 he worked on Imaging topics (Binary Pixel and Lensless Smart Sensors).
Prior to working for Rambus, he had various roles in DRAM R&D between 1994 and 2009 at Siemens, Infineon and Qimonda with his main interest in the interaction between circuit design and technology and in low power DRAMs. Thomas Vogelsang is a Senior Member of the IEEE and a member of the International Focus Team on Cryogenic Electronics and Quantum Information Processing of the IRDS. He is author or co-author of 24 publications, 87 granted US patents and multiple pending patent applications. His 2010 paper on DRAM energy consumption is widely referenced in the computer architecture community, cited by over 200 other publications.
He received his diploma and Ph.D. in physics from the Technical University of Munich, Germany.