Session 7 - Modeling and Simulation - Physics of Ferroelectric and Negative Capacitance Devices
Monday, December 9, 1:30 p.m.
Continental Ballroom 6
Co-Chairs: Y. Singh Chauhan, IIT Kanpur
A. Islam Khan, Georgia Institute of Technology

1:35 PM **7.1** Hysteresis-free Negative Capacitance in the Multi-Domain Scenario for Logic Applications
Jorge Gomez, Sourav Dutta, Kai Ni, Jeffrey Smith, Benjamin Grisafe, Asif Khan, Suman Datta, University of Notre Dame, Georgia Institute of Technology

We report for the first time that hysteresis-free negative capacitance can be achieved in a multi-domain FE-DE structure. The results could pave the way for understanding the design framework of robust, steep negative capacitance FETs (NCFETs) with multi- domain ferroelectrics.

2:00 PM **7.2** Revised Analysis of Negative Capacitance in Ferroelectric-Insulator Capacitors: Analytical and Numerical Results, Physical Insight, Comparison to Experiments.
Tommaso Rollo, Franco Blanchini, Giulia Giordano, Ruben Specogna, David Esseni, University of Udine, Delft University of Technology

We present a revised analysis of Negative Capacitance(NC) in ferroelectric-insulator capacitors, focusing on the difference between MFMIM and MFIM-systems. We develop a model accounting for 3D-electrostatics, reporting analytical and numerical results. We explained the lack of NC operation in MFMIMs, compare well with experiments and enlighten the role of traps.

2:25 PM **7.3** Electrostatic Integrity in Negative-Capacitance FETs – A Subthreshold Modeling Approach (Invited)
Pin Su, Wei-Xiang You, National Chiao Tung University

Using a subthreshold potential model, this paper shows that the negative-capacitance FinFET inherently possesses a superior electrostatic integrity than the baseline FinFET. Considering the spacer-induced distributed-charges in our model, we demonstrate that an adequate spacer design can be utilized to further enhance the negative-capacitance effect and the EI for NC-FinFETs.

2:50 PM *COFFEE BREAK*

3:15 PM **7.4** Equivalent Oxide Thickness (EOT) Scaling With Hafnium Zirconium Oxide High-κ Dielectric Near Morphotropic Phase Boundary
Kai Ni, Atanu Kumar Saha, Wriddhi Chakraborty, Huacheng Ye, Benjamin Grisafe, Jeffrey Smith, G. Bruce Rayner, Sumeet Gupta, Suman Datta, University of Notre Dame, Purdue University, Kurt J. Lesker Co.

We demonstrate a novel strategy to scaling the equivalent oxide thickness of MOSFETs by tuning the composition of $Hf_{1-x}ZrxO_2$ thin-film near morphotropic phase boundary, where orthorhombic ferroelectric phase and tetragonal anti-ferroelectric phase co-exist such that a small external electrical perturbation gets amplified to a large charge response through phase transformation.

3:40 PM **7.5** Surface potential-Based Compact Model for Negative Capacitance FETs Compatible for Logic Circuit: with Time Dependence and Multidomain Interaction
Ying Zhao, Ling Li, Quan Li, Xichen Chuai, Guanhua Yang, Ming Liu, Qiang Li, Yue Peng, Genquan Han, Institute of Microelectronics of Chinese Academy of Sciences

A continuous surface potential based compact model of NCFET is proposed, incorporating the multi-domain interaction term, polarization relaxation, temperature dependence and scattering. For the first time, an analytical solution of surface potential without any empirical fitting parameters is obtained. The model is calibrated by experiment and successfully implemented into Verilog-A.