

Session 5 - Reliability of Systems and Devices - Back End and Advanced Characterization

Monday, December 9, 1:30 p.m.

Continental Ballroom 4

Co-Chairs: K. Weide-Zaage, Leibniz Universität Hannover

G. Reibold, CEA-LETI

1:35 PM 5.1 Reverse Tip Sample Scanning for Precise and High-Throughput Electrical Characterization of Advanced Nodes

Umberto Celano, Thomas Hantschel, Thijs Boehme, Antti Kanninen, Lennaert Wouters, Hugo Bender, Niels Bosman, Chris Drijbooms, Steven Folkersma, Kristof Paredis, Wilfried Vandervorst, Paul van der Heide, imec, KU Leuven, University of Jyväskylä

A new method is proposed to enable high-throughput and high-resolution electrical atomic force microscopy in nanoelectronics. Using a reversed pathway of operation, our technique yields an increased time-to-data ($>10x$), enhanced dataset statistics and nm-precise resolution; as herein demonstrated for two- and three-dimensional carrier profiling in fin structures of advanced nodes.

2:00 PM 5.2 Hot-Spot Thermal Sensor Design in FinFETs

S. L. Liu, J. J. Horng, Amit kundu, B. S. Lien, C. H. Lee, Y. H. Chen, Chester Kuo, Y. C. Peng, and Mark Chen, Taiwan Semiconductor Manufacturing Company

This paper analyzes device-structure-induced and process- dependent temperature inaccuracy sources of thermal sensing applications in FinFETs: Self-heating and Joule-heating interaction, non-uniform FinFET-array temperature distribution, and distance limitation due to gate-area non-uniformity. Thermal behaviors of these inaccuracy sources are comprehensively characterized to mitigate the temperature gap between hot-spots and measurements.

2:25 PM 5.3 Characterizing Electromigration Effects in a 16nm FinFET Process Using a Circuit Based Test Vehicle

Nakul Pande, Chen Zhou, M. H. Lin, Rita Fung, Rick Wong, Shi-Jie Wen, Chris Kim, University of Minnesota, TSMC, Cisco Systems

This work showcases measured data corresponding to direct-current (DC) stress induced electromigration (EM) phenomenon, characterized using on-chip circuits for multiple interconnect test structures fabricated in a 16nm FinFET process.

2:50 PM COFFEE BREAK

3:15 PM 5.4 Humidity Penetration Impact on Integrated Circuit Performance and Reliability, Franco Stellari, Cyril Cabral, Peilin Song, Robert Laibowitz, IBM TJ Watson Research

We study the impact of humidity penetration into ICs. We found that the humidity penetration causes the performance of the circuit to be reduced because of the BEOL capacitance increase, while no detectable impact on the overall circuit lifetime is observed because of FEOL BTI and GOX mechanisms dominance.

3:40 PM 5.5 Non-Planarization Cu-Cu Direct Bonding and Gang Bonding with Low Temperature and Short Duration in Ambient Atmosphere

Tzu-Chieh Chou, Kai-Ming Yang, Jian-Chen Li, Ting-Yang Yu, Ying-Ting Chung, Cheng-Ta Ko, Yu-Hua Chen, Tzyy-Jang Tseng, Kuan-Neng Chen, National Chiao Tung University, Unimicron Technology Corp.

Low temperature (150°C) and short duration Cu-Cu direct bonding, without planarization, and gang bonding approaches are demonstrated. The concept is based on the high stress-led inducing deformation and internal friction to achieve low temperature bonding. The bonding structure has the advantage of high roughness tolerance on surface without CMP requirement.