Session 4 - Power Devices and Systems - Advances in GaN Power Devices and GaN Monolithic Integration
Monday, December 9, 1:30 p.m.
Continental Ballroom 1-3
Co-Chairs: P. Moens, ON Semiconductor
G. Prechtl, Infineon Technologies

1:35 PM  4.1  1200 V Multi-Channel Power Devices with 2.8 Ω·mm ON-Resistance
Jun Ma, Catherine Erine, Minghua Zhu, Nela Luca, Peng Xiang, Kai Cheng, Elison Matioli, EPFL, Enkris Semiconductor Inc.

This work demonstrates novel multi-channel GaN devices with slanted tri-gates, presenting high breakdown voltage of 1200 V on a highly-conductivity epi-structure with 80 Ω/sq and low on-resistance of 2.8 Ω*mm. The excellent figure-of-merit of 3.2 GW/cm² significantly outperforms conventional single-channel devices, providing a promising pathway for future efficient power devices.

2:00 PM  4.2  Impact Ionization Coefficients in GaN Measured by Above- and Sub-\(E_g\) Illuminations for \(p^−/n^+\) Junction
Takuya Maeda, Tetsuo Narita, Shinji Yamada, Tetsu Kachi, Tsunenobu Kimoto, Masahiro Horita, Jun Suda, Nagoya University, Kyoto University, Toyota Central R&D Labs, ULVAC Inc.

We propose a novel method to extract impact ionization coefficients of electrons and holes using above- and sub-bandgap illuminations for a \(p^−/n^+\) junction diode. By analyzing the avalanche multiplication of electron- and hole-injected (Franz-Keldysh-induced) photocurrents, the impact ionization coefficients of electrons and holes in GaN are extracted separately.

2:25 PM  4.3  Investigation of nBTI degradation on GaN-on-Si E-mode MOSc-HEMT
Abygaël Viey, William Vandendaele, Marie-Anne Jaud, Jacques Cluzel, Jean-Paul Barnes, Simon Martin, Alexis Krakovinsky, Romain Gwoziecki, Marc Plissonier, Fred Gaillard, Roberto Modica, Ferdinando Iucolono, Matteo Meneghini, Enrico Zanon, Gaudenzio Meneghesso, Gérard Ghibaudo, CEA-Leti, STMicroelectronics, Grenoble Alpes University, University of Padova

We investigate the negative gate stress influence on \(V_{TH}\) instabilities in GaN devices. NBTI transients and complementary ToF-SIMS analysis reveal two trap populations positions involved on \(V_{TH}\) instabilities. Both of them are related to \(C_n\) acceptor traps. NBTI transients exhibit LG influence, which is consistent with the E-field distribution simulation.

3:15 PM  4.4  GaN-on-SOI: Monolithically Integrated All-GaN ICs for Power Conversion

We report the first comprehensive research about GaN power ICs on GaN-on-SOI. HEMT, MIM capacitor, SBD, 2DEG resistor, and resistor-transistor logic (RTL) are co-integrated. A 48V-to-1V buck converter is realized using 200 V GaN half-bridges with integrated drivers. Further, an all-GaN buck converter is successfully designed using the GaN PDK.

3:40 PM  COFFEE BREAK

4:05 PM  4.5  GaN/AlN Schottky-gate p-channel HFETs with InGaN Contacts and 100mA/mm On-current

4:30 PM
High-performance wide-bandgap p-channel devices are broadly desirable to expand the design topologies available in power/RF electronics. To meet that need, this work advances the GaN-on-AlN platform. Authors fabricate p-channel HFETs with 100mA/mm on-currents at room temperature. Various temperature-dependencies, benchmarking results, and technology perspectives are discussed.

4:30 PM 4.6 First Demonstration of a Self-Aligned GaN p-FET
Nadim Chowdhury, Qingyun Xie, Mengyang Yuan, Nitul Rajput, Peng Xiang, Kai Cheng, Han Wui Then, Tomas Palacios, Massachusetts Institute of Technology, Khalifa University, Enkris Semiconductor Inc., Intel Corporation

A self-aligned p-FET with GaN/Al_{0.2} Ga_{0.8} N (20 nm)/GaN heterostructure grown by MOCVD on Si-substrate is demonstrated. Reported Lg=100 nm E-mode p-FET V_{TH}=-1V, exhibits a record R_{ON}=400 Ω∙mm and I_{ON} >5 mA/mm with I_{ON}/I_{OFF} =6×10^5 among p-FETs based on GaN/AlGaN heterostructure, making it a promising candidate for GaN-based complementary circuit technology.