Session 39 - Modeling and Simulation - Multiscale Modeling of Devices and Circuits
Wednesday, December 11, 1:30 p.m.
Continental Ballrom 6
Co-Chairs: W. Vandenberghe, University of Texas, Dallas
C. Weber, Intel

1:35 PM **39.1** State-of-the-art TCAD: 25 Years Ago and Today (Invited)
M. Stettler, S. Cea, S. Hasan, L. Jiang, A. Kaushik, P. Keys, R. Kotlyar, C. Landon, D. Pantuso, A. Slepko, S. Smith, V. Tiwari, C. Weber, and J. R. Weber, Intel Corporation

This talk contrasts Intel's TCAD environment of 25 years ago with today's, which has shifted steadily from more applications-oriented work towards research, and gives examples of studies which illustrate the evolution.

2:00 PM **39.2** Efficient Variability- and Reliability-aware Device-Circuit Co-Design: From Trap Behaviors to Circuit Performance
Wangyong Chen, Linlin Cai, Gang Du, Xiaoyan Liu, Peking University

An efficient variability- and reliability- aware solution is proposed to achieve the device-circuit co-design. STIM method links the charge distributions to the time-dependent variability and reliability. A variation-aware model based on the database is proposed to predict the time-dependent delay degradation and potential critical paths in the digital circuits.

2:25 PM **39.3** Role of Correlation in Systematic Variation Modeling
Ananda Roy, Sourabh Dongaonkar, Sivakumar Mudanai, Intel Corporation

In this work, we show the important, and so far, unrecognized, role that the fine structure of parameter correlations plays in accurate modeling of random variable based systematic variation. We provide an intuitive statistical model to go beyond simple correlation coefficient and accurately capture distribution of measured electrical quantities.

2:50 PM **39.4** An Empirically Validated Virtual Source FET Model for Deeply Scaled Cool CMOS
Wriddhi Chakraborty, Kai Ni, Jeffrey Smith, Arijit Raychowdhury, Suman Datta, University of Notre Dame, Georgia Institute of Technology

We conclude that while ballistic efficiency of nanoscale MOSFETs degrade in linear region as we approach cryogenic temperature, its ballistic efficiency improves in the saturation region at low temperature. The model is used to project performance of Cool CMOS technology for 15nm channel length FETs at deeply scaled nodes.

3:15 PM **39.5** Multiphysics Simulation & Design of Silicon Quantum Dot Qubit Devices
Fahd Ayyalil Mohiyaddin, George Simion, Nard Dumoulin Stuyck, Roy Li, Florin Ciubotaru, Geert Eneman, Fabian Bufler, Stefan Kubicek, Julien Jussot, BT Chan, Tsvetan Ivanov, Alessio Spessot, Philippe Matagne, James Lee, Bogdan Govoreanu, Iuliana Radu, imec

Silicon qubits are strong contenders for building a large-scale quantum processor. Here, we combine several multiphysics simulation methods to assemble a design methodology for silicon qubit devices. We

summarize key device parameters, dimensions and voltages based on detailed models that consider device electrostatics, stress, micro-magnetics, band-structure and spin dynamics.