Session 38 - Memory Technology - Memory for Neural Network
Wednesday, December 11, 1:30 p.m.
Continental Ballroom 5
Co-Chairs: M. Liu, Chinese Academy of Science
Q. Ren, UNIC Memory Technology Co., Ltd

**1:35 PM** **38.1** Optimal Design Methods to Transform 3D NAND Flash into a High-Density, High-Bandwidth and Low-Power Nonvolatile Computing in Memory (nvCIM) Accelerator for Deep-Learning Neural Networks (DNN)
Hang-Ting Lue, Po-Kai Hsu, Ming-Liang Wei, Teng-Hao Yeh, Pei-Ying Du, Wei-Chen Chen, Keh-Chung Wang, and Chih-Yuan Lu, Macronix

We propose optimal design methods of 3D NAND Flash to achieve high-density, high-bandwidth and low-power nvCIM. The proposed 3D NAND nvCIM can produce TOPS/W ~40 (4I4W), and achieve 74.6 frame/sec for a heavy VGG16 network. It is potential to provide high-density and low-power accelerator for deep-learning neural network.

**2:00 PM** **38.2** Storage Reliability of Multi-bit Flash Oriented to Deep Neural Network
Yachen Xiang, Peng Huang, Haozhang Yang, Kunliang Wang, Runze Han, Wensheng Shen, Yulin Feng, Chen Liu, Xiaoyan Liu, Jinfeng Kang, Peking University

The storage reliability of multi-bit flash is of vital importance for the flash based deep neural network (DNN). In this work, the critical concerns correlated with the storage reliability ($I_d$) distribution and data retention) of multi-bit flash and its impacts on the DNN are investigated for the first time.

**2:25 PM** **38.3** A 3D NAND Flash Ready 8-Bit Convolutional Neural Network Core Demonstrated in a Standard Logic Process
Minsu Kim, Muqing Liu, Luke Everson, Gyusung Park, Younghee Jeon, Sihwan Kim, Sang-Soo Lee, Seung-hwan Song, Chris Kim, University of Minnesota, Anaflash Inc.

A convolutional neural network (CNN) core that can be readily mapped to a 3D NAND flash array was demonstrated in a standard 65nm CMOS process. Logic-compatible embedded flash memory cells were used for storing multi-level synaptic weights while a bit-serial architecture enables 8 bit multiply-and-accumulate operation.

**2:50 PM** **38.4** High-Density and Highly-Reliable Binary Neural Networks Using NAND Flash Memory Cells as Synaptic Devices
Sung-Tae Lee, Hyungsu Kim, Jong-Ho Bae, Honam Yoo, Nag Yong Choi, Dongseok Kwon, Suhwan Lim, Byung-Gook Park, Jong-Ho Lee, Seoul National University

A novel synaptic architecture based on NAND cell strings is proposed as a high-density synapse capable of XNOR operation for binary neural networks (BNNs) for the first time. By changing the threshold voltage of NAND flash cells and input voltages in complementary fashion, the XNOR operation is successfully demonstrated.

**3:15 PM** **38.5** Complementary Memory Cell Based on Field-Programmable Ferroelectric Diode for Ultra-Low Power Current-SA Free BNN Applications

Qing Luo, Bing Chen, Rongrong Cao, Xiaoyong Xue, Keji Zhou, Jianguo Yang, Xu Zheng, Haoran Yu, Jie Yu, Tiancheng Gong, Xiaoxin Xu, Peng Yuan, Xiaoyan Li, Lu Tai, Qi Liu, Hangbing Lv, Ming Liu, Institute of Microelectronics of Chinese Academy of Sciences, Zhejiang University, Fudan University

We proposed a complementary memory cell with 2T4D XNOR structure for computing in memory (CIM) applications. Firstly, a field-programmable diode (FPD) was demonstrated with a W/HZO/W structure. For BNN application, a 2T4D XNOR cell-based CSA-free BNN architecture is proposed with small cell area (16 $F^2$) and superior efficiency (387 TOPS/W).

**3:40 PM** **38.6** A 2TnC Ferroelectric Memory Gain Cell Suitable for Compute-in-memory and Neuromorphic Application
Stefan Slesazeck, Taras Ravsher, Viktor Havel, Evelyn Breyer, Halid Mulaosmanovic, Thomas Mikolajick, NaMLab gGmbH, TU Dresden

A 2TnC ferroelectric memory gain cell is proposed, that can be operated either in FeRAM or FTJ mode. The internal gain of the cell mitigates the need for 3D integration of the FeCAPs, making the concept very attractive for embedded memories, compute-in-memory and neuromorphic applications.

**4:05 PM** **38.7** Memory-Logic Hybrid Gate with 3D-Stackable Complementary Latches for FinFET-based Neural Networks
Chieh Lee, Yue-Der Chih, Jonathan Chang, Chrong Jung Lin, Ya-Chin King, National Tsing Hua University, Taiwan Semiconductor Manufacturing Company

A memory-logic hybrid gate with complementary resistive switching pairs on vias in BEOL FinFET technologies with an area-efficient, 3D-stackable structures is proposed. Stable output logic stages enabled by the complementary states on the RRAM pair have been demonstrated. Through stacked-vias architectures, logic operations based on multiple non-volatile states are achieved.