Session 37 - Emerging Device and Compute Technology - Nano Devices for Low-Power Technologies
Wednesday, December 11, 1:30 p.m.
Continental Ballroom 4
Co-Chairs: H. Fukutome, Samsung
F. Schwierz, Technical University Ilmenau

1:35 PM **37.1** Sub-Thermionic Scalable III-V Tunnel Field-Effect Transistors Integrated on Si (100)
Clarissa Convertino, Cezar Zota, Yannick Baumgartner, Philipp Staudinger, Marilyne Sousa, Svenja Mauthe, Daniele Caimi, Lukas Czornomaz, Adrian Ionescu, Kirsten Moselund, IBM Research - Zurich, EPFL

We present scalable III-V tunnel FETs fabricated using a Si CMOS-compatible FinFET process flow and integrated on Si (100) substrates. The devices exhibit a minimum SS of 47 mV/decade, an I_{ON} of 1.5 μA/μm at I_{OFF} = 1 nA/μm and V_{DD} = 0.3 V, and I_{60} of 10 nA/μm.

2:00 PM **37.2** Co-integrated Subthermionic 2D/2D $WSe_2/SnSe_2$ Vertical Tunnel FET and WSe_2 MOSFET on *same flake*: towards a 2D/2D vdW Dual-Transport Steep Slope FET
Nicolo Oliva, Luca Capua, Matteo Cavalieri, Adrian Ionescu, EPFL

In this work we report the fabrication, co-integration and resulting performance of 2D/2D van der Waals (vdW) Vertical p-type Tunnel FETs and p-MOSFETs in a WSe_2SnSe_2 material system. We report the best ever reported combined performance in terms of subthermionic subthreshold swing for a 2D/2D vertical Tunnel FET.

2:25 PM **37.3** Experimental Demonstration of Integrated Magneto-electric and Spin-orbit Building Blocks Implementing Energy-efficient Logic
Chia-Ching Lin, Tanay Gosavi, Dmitri Nikonov, Yen-Lin Huang, Bhagwati Prasad, WonYoung Choi, Van Tuong Pham, Inge Groen, Jun-Yang Chen, Mahendra DC, Huichu Liu, Kaan Oguz, Emily Walker, John Plombon, Benjamin Buford, Carl Naylor, Jian-Ping Wang, Felix Casanova, Ramamoorthy Ramesh, Ian Young, University of California, Berkeley, Intel Corporation, CIC nanoGUNE, University of Minnesota

600 mV magneto-electric switching in 30 nm La-doped $BiFeO_3$ multiferroic oxide and a proof of concept 7 μV spin-orbit signal output in Pt / CoFe local spin injection device with 100 μA supply current were experimentally demonstrated at room temperature for the 1st time. Also demonstrated was a path towards 70 mV spin orbit output using Bi_2Se_3 in a local spin injection device. These are key accomplishments for WRITE and READ building blocks, respectively, toward realization of a magneto-electric spin-orbit (MESO) energy efficient logic device. Moreover, the 1st generation of a MESO logic device with a functional READ unit is demonstrated.

2:50 PM **37.4** Self-organized Pairs of Ge Double Quantum Dots with Tunable Sizes and Spacings Enable Room-Temperature Operation of Qubit and Single-Electron Devices
Kang-Ping Peng, Ching Lun Chen, Ying-Tsan Tang, David M. T. Kuo, Thomas George, Horng-Chih Lin, Pei-Wen Li, National Chiao Tung University, Taiwan Semiconductor Research Institute, National Central University

We report paired Ge double QDs using spacer technology in combination with oxidation of $Si_{0.85}Ge_{0.15}$ in a self-organization approach. Process-controlled tunability of Ge QD diameters (5–20nm) and spacings

(12nm) were achieved. We demonstrated room-temperature operation of Ge qubit devices, within which one QD encodes charges with a proximal QD-SET reads-out.

3:15 PM **37.5** A Probabilistic Approach to Quantum Inspired Algorithms (Invited)
Shuvro Chowdhury, Supriyo Datta, Kerem Yunus Camsari, Purdue University

We describe Probabilistic Computing, based on probabilistic or p-bits that fluctuate between 0 and 1, that are in between digital and quantum mechanical bits. Compact, energy efficient hardware p-bits realized from present-day spintronic building blocks can be interconnected into p-circuits to implement a host of quantum computing inspired algorithms.

3:40 PM **37.6** High-speed Low-energy Heat Signal Processing via Digital-compatible Binary Switch with Metal-insulator Transitions
Takeaki Yajima, Takahisa Tanaka, Yusuke Samata, Ken Uchida, Akira Toriumi, The University of Tokyo, JST-PRESTO

The binary thermistor using the VO_2 metal-insulator transition enables the direct conversion of heat signal to the digital bits with high speed (sub-ns) and low energy (sub-pJ), promising for microscopic heat management. The binary thermistor also enables the high-speed and low-energy heat-mediated data transfer as a basis for non-charge-based functionalities.

4:05 PM **37.7** Gate Reflectometry for Probing Charge and Spin States in Linear Si MOS Split-gate Arrays
Louis Hutin, Benoit Bertrand, Emmanuel Chanrion, Heorhii Bohuslavskyi, Fabio Ansaloni, Tsung-Yeh Yang, John Michniewicz, David Niegemann, Cameron Spence, Theodor Lundberg, Anasua Chatterjee, Alessandro Crippa, Jing Li, Romain Maurand, Xavier Jehl, Marc Sanquer, Fernando Gonzalez-Zalba, Ferdinand Kuemmeth, Yann-Michel Niquet, Silvano De Franceschi, Matias Urdampilleta, Tristan Meunier, Maud Vinet, CEA Leti, CNRS Institut Néel, University of Copenhagen, University of Cambridge, CEA IRIG, Hitachi Cambridge Laboratory

We fabricated a 2×N array of individually controllable Si quantum dots (QDs) with nearest neighbor coupling. We implemented two different gate reflectometry-based readout schemes to either probe spin-dependent charge movements by a coupled electrometer with single-shot precision, or directly sense a spin-dependent quantum capacitance.

4:30 PM **37.8** Experimental Demonstration of Phase Transition Nano-Oscillator Based Ising Machine
Sourav Dutta, Abhishek Khanna, Jorge Gomez, Kai Ni, Zoltan Toroczkai, Suman Datta, University of Notre Dame

Finding the ground state of Ising model maps to various combinatorial optimization problems. Here, we experimentally demonstrate an Ising machine using coupled phase transition metal-to-insulator nano-oscillators (IMT-NO). Compared to other implementations, our hardware provides advantage from the standpoint of room-temperature operation, programmable coupling scheme, compactness and ease of scalability.