Session 36 - Advanced Logic Technology - CMOS Platform Technologies
Wednesday, December 11, 1:30 p.m.
Grand Ballroom B
Co-Chairs: C. Chu, Applied Materials
Y. Li, Lam Research

1:35 PM **36.1** Design-Technology Co-Optimization of Anti-Fuse Memory on Intel 22nm FinFET Technology
Yu-Lin Chao, Sarvesh H. Kulkarni, Soonwoo Cha, Leif R. Paulson, Salil M. Rajarshi, Jason Bloomstrom, Guannan Liu, Mark Armstrong, Jiabo Li, Chen-Yi Su, Stephen M. Ramey, Uddalak Bhattacharya, Bernhard Sell and Ying Zhang, Intel Corporation

An in-depth study of Intel's first FinFET anti-fuse memory is reported. Improvement on gate oxide integrity, source/drain resistance optimization, careful layout design on both bitcell and array, and smart selection of synthesis in combination can offer an array yield exceeding 99.9% without redundancy scheme and at no added process cost.

2:00 PM **36.2** Variability Sources in Nanoscale Bulk FinFETs and TiTaN- a Promising Low Variability WFM for 7/5nm CMOS Nodes
Mandar S. Bhoir, Thomas Chiarella, Lars-Ake Ragnarsson, Jerome Mitard, Naoto Horiguchi, Nihar Ranjan Mohapatra, IIT Gandhinagar, imec

An experimental methodology to segregate variability sources in FinFETs (W_{fin} <10nm) is proposed. The V_t variation, from gate work-function metal (WFM) and oxide charge variations, is the major contributor to in-wafer variability. The FER, GER, RDF contribution to V_t variability is negligible. TiTaN, low variability WFM, for future gate-stack, is introduced.

2:25 PM **36.3** Key Technology Enablers of Innovations in the AI and 5G Era (Invited)
Shien-Yang Wu, Taiwan Semiconductor Manufacturing Company

The proliferation of AI and the deployment of 5G networks accelerate the transformation of our society into a highly connected world. Semiconductors are the indispensable elements in realizing all the product innovations. The progress and challenges of the state of art CMOS technology and advanced packaging will be reviewed.

2:50 PM **36.4** Ultra-scaled Conformal Scavenging Electrode with Superior Tunability for Short-channel RMG FinFET Workfunction and all-ALD 3D-compatible ReRAM
John Rozen, Yohei Ogawa, Takashi Ando, Ruqiang Bao, Eduard Cartier, Kazuhiro Honda, Keon-Chang Lee, John Bruley, Hiroyuki Miyazoe, Koukou Suu, Masanobu Hatanaka, Vijay Narayanan, ULVAC Inc., IBM Research

A baseline TiAl-containing ALD workfunction electrode is established. Furthermore, a novel ALD metal-compound material, MX, yields at least 10Å further scaling of the electrode stack in RMG FinFETs due to its superior scavenging power. For the first time, using MX, we demonstrate an all-ALD ReRAM compatible with 3D architectures.

3:15 PM **36.5** Novel Forksheet Device Architecture as Ultimate Logic Scaling Device Towards 2nm

Pieter Weckx, Julien Ryckaert, Eugenio Litta, Dmitry Yakimets, Philippe Matagne, Pieter Schuddinck, Doyoung Jang, Bilal Chehab, Rogier Baert, Mohit Gupta, Yusuke Oniki, Lars-Ake Ragnarsson, Naoto Horiguchi, Alessio Spessot, Diederik Verkest, imec

Due to CPP scaling slowdown below 42nm, several scaling boosters are needed to reduce the logic standard cell height. Limited scaling can be achieved using FinFET and nanosheets due integration limits for PN separation. A novel forksheet device is proposed achieving extremely scaled PN space using limited additional processing complexity.

3:40 PM **36.6** Machine Learning-enhanced Multi-dimensional Co-Optimization of Sub-10nm Technology Node Options
Ahmet Ceyhan, Jonathan Quijas, Saurabh Jain, Hung-Yi Liu, William E. Gifford, Sourav Chakravarty, Intel Corporation

This paper introduces a machine-learning-enhanced multi-objective, multi-domain co-optimization framework. It presents a holistic approach to define a technology node by co-optimizing its options from the transistor to system level and demonstrates 10X improvement in turn-around time with better quality of results compared to human-optimized CPU implementations in Intel's 10nm technology.

4:05 PM **36.7** 5nm CMOS Production Technology Platform featuring full-fledged EUV, and High Mobility Channel FinFETs with Densest 0.021 μm^2 SRAM Cells for Mobile SoC and High Performance Computing Applications (Late News)
Geoffrey Yeap, S.S. Lin, Y.M. Chen, H.L. Shang, P.W. Wang, H.C. Lin, Y.C. Peng, J.Y. Sheu, M. Wang, X. Chen, B.R. Yang, C.P. Lin, F.C. Yang, Y.K. Leung, D.W. Lin, C.P. Chen, K.F. Yu, D.H. Chen, C.Y. Chang, H.K. Chen, P. Hung, C.S. Hou, Y.K. Cheng, J. Chang, L. Yuan, C.K. Lin, C.C. Chen, Y.C. Yeo, M.H. Tsai, H.T. Lin, C.O. Chui, K.B. Huang, W. Chang, H.J. Lin, K.W. Chen, R. Chen, S.H. Sun, Q. Fu, H.T. Yang, H.T. Chiang, C.C. Yeh, T.L. Lee, C.H. Wang, S.L. Shue, C.W. Wu, R. Lu, W.R. Lin, J. Wu, F. Lai, Y.H. Wu, B.Z. Tien, Y.C. Huang, L.C. Lu, Jun He, Y. Ku, J. Lin, M. Cao, T.S. Chang, S.M. Jang, Taiwan Semiconductor Manufacturing Company

Industry-leading 5nm CMOS technology features, for the first time, full-fledged EUV, and high mobility channel finFETs, offering ~1.84x logic density, 15% speed gain or 30% power reduction over 7nm. This true 5nm technology successfully passed qualification with high yield, and targets for mass production in 1H 2020.