Session 35 - Memory Technology - Selectors and RRAM: Technology and Computing
Wednesday, December 11, 1:30 p.m.
Grand Ballroom A
Co-Chairs: H-Y Cheng, Macronix International Co., Ltd.
S. Spiga, CNR-IMM

1:35 PM **35.1** Composition Optimization and Device Understanding of Si-Ge-As-Te Ovonic Threshold Switch Selector with Excellent Endurance
Daniele Garbin, Wouter Devulder, Robin Degraeve, Gabriele Luca Donadio, Sergiu Clima, Karl Opsomer, Andrea Fantini, Daniel Cellier, Wan Gee Kim, Mahendra Pakala, Andrew Cockburn, Christophe Detavernier, Romain Delhougne, Ludovic Goux, Gouri Sankar Kar, imec, Applied Materials, Inc., Ghent University

We explore the composition space of the Si-Ge-As-Te based ovonic threshold switch selector device. We optimize the composition to increase the crystallization temperature T_x >450°C and achieve stable endurance of more than 10^{11} cycles. We propose a switching model that predicts the distribution of the threshold voltage, drift and time-dependent instabilities.

2:00 PM **35.2** Endurance Improvement of More than Five Orders in Ge_xSe_{1-x} OTS Selectors by using a Novel Refreshing Program Scheme
Firas Hatem, Zheng Chai, Weidong Zhang, Andrea Fantini, Robin Degraeve, Sergiu Clima, Daniele Garbin, John Robertson, Yuzheng Guo, Jian Fu Zhang, John Marsland, Pedro Freitas, Ludovic Goux, Gouri Sankar Kar, imec, Liverpool John Moores University, University of Cambridge, Wuhan University

OTS degradation and the endurance can be therefore improved by more than five orders without adding additional material elements or process steps, based on understanding of the recoverable (slow delocalized defects) and non-recoverable (Ge-Se segregation/crystallization) degradation mechanisms.

2:25 PM **35.3** Reliability and Variability of 1S1R OxRAM-OTS for High Density Crossbar Integration
Diego Alfaro Robayo, Gilbert Sassine, Joel Minguet Lopez, Laurent Grenouillet, Anthonin Verdy, Gabriele Navarro, Mathieu Bernard, Eduardo Esmanhotto, Cathy Carabasse, Damien Deleruyelle, Elisa Vianello, Niccolo Castellani, Lorenzo Ciampolini, Bastien Giraud, Carlo Cagli, Gérard Ghibaudo, Etienne Nowak, Gabriel Molas, CEA Leti, IMEP-LAHC, INL CNRS

HfO_2-OxRAM was co-integrated with optimized OTS selector in 1S1R arrays. Up to 3 decades of current window margin and 5 decades of selectivity were achieved. More than 10^6 programming, and 10^9 read-disturb cycles were demonstrated. 1Gb bank size is envisaged. Semi-analytical model of OTS was developed to analyze stochastic switching.

2:50 PM **35.4** Learning with Resistive Switching Neural Networks (Invited)
Mingyi Rao, Zhongrui Wang, Can Li, Hao Jiang, Rivu Midya, Peng Lin, Daniel Belkin, Wenhao Song, Shiva Asapu, Qiangfei Xia, Joshua Yang, University of Massachusetts, Amherst

Processing-in-memory with RRAMs or memristors is a potential solution to accelerate machine learning in hardware neural networks, which may drastically improve the energy-area efficiency. Here, we discuss three major types of learning, namely the supervised, reinforcement, and unsupervised learning implemented with various 1T1R based neural networks.

3:15 PM **35.5** Novel 1T2R1T RRAM-based Ternary Content Addressable Memory for Large Scale Pattern Recognition
Denys R. B. Ly, Jean-Philippe Noel, Bastien Giraud, Pablo Royer, Eduardo Esmanhotto, Niccolo Castellani, Thomas Dalgaty, Jean-Francois Nodin, Claire Fenouillet-Beranger, Etienne Nowak, Elisa Vianello, CEA-Leti

Resistive-Memories (RRAMs) enable implementations of area-and-energy-efficient Ternary-Content-Addressable-Memories (TCAMs). However, the low RRAM resistance ratio limits the word length of RRAM-based TCAMs hindering the parallel search of large volumes of data for data-intensive applications. Here, we propose a new 1-transistor-2-RRAMs-1-transistor TCAM insensitive to RRAM resistance ratio allowing searches of large pattern.

3:40 PM **35.6** High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning
E. R. Hsieh, M. Giordano, B. Hodson, Akash Levy, S. K. Osekowsky, R. M. Radway, Y. C. Shih, W. Wan, T. F. Wu, Xin Zheng, M. Nelson, B. Q. Le, H. -S. Philip Wong, S. Mitra, S. Wong, Stanford University, National Chiao Tung University, National Tsinghua University, San Jose State University, SkyWater Technology Foundry

We present the first demonstration of 1T4R Resistive RAM (RRAM) array storing two bits per RRAM cell. Our HfO_2-based RRAM is built using a logic foundry technology that is fully compatible with the CMOS back-end process.

4:05 PM **35.7** Metal-oxide Based, CMOS-compatible ECRAM for Deep Learning Accelerator
Seyoung Kim, Teodor Todorov, Murat Onen, Tayfun Gokmen, Douglas Bishop, Paul Solomon, Ko-tao Lee, Matt Copel, Damon Farmer, John Ott, Takashi Ando, Hiroyuki Miyazoe, Vijay Narayanan, John Rozen, IBM TJ Watson Research Center

We demonstrate a CMOS-compatible, metal-oxide based Electro-Chemical Random-Access Memory (MO-ECRAM) featuring symmetric and linear conductance update and selector-less parallel array operations while withstanding high temperature treatments necessary for BEOL compatibility. For the first time, we experimentally show a successful stochastic gradient descent algorithm demonstration using an MO-ECRAM array.

4:30 PM **35.8** Co Active Electrode Enhances CBRAM Performance and Scaling Potential
Attilio Belmonte, Janaki Radhakrishnan, Ludovic Goux, Gabriele Luca Donadio, P. Kumbhare, Augusto Redolfi, Romain Delhougne, Laura Nyns, Wouter Devulder, Thomas Witters, Angelo Covello, Alexis Franquet, Valentina Spampinato, Shreya Kundu, Ming Mao, Hubert Hody, Gouri Sankar Kar, Guy Vereecke, imec, KU Leuven, Università della Calabria

We report for the first time the low-current performance enhancement combined with the improvement of the scaling potential in CBRAM devices by adopting Co as active electrode. Co is proven to yield, with respect to Cu, faster/lower voltage switching and more stable conductive filaments.