Session 31 - Emerging Device and Compute Technology - Focus Session: Quantum Computing Infrastructure
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: I. Radu, imec
Z. Chen, Purdue University

9:05 AM **31.1** Manufacturing Low Dissipation Superconducting Quantum Processors (Invited)
Ani Nersisyan, Stefano Poletto, Nasser Alidoust, Riccardo Manenti, Russ Renzas, Cat-Vu Bui, Kim Fu, Tyler Whyland, Yuvraj Mohan, Eyob Sete, Sam Stanwyck, Andrew Bestwick, Matthew Reagor, Rigetti Computing

Near-term quantum computing applications leverage a hybrid architecture, in which classical and quantum computers work together as co-processors. Here, we provide a framework to analyze application runtime performance on such hardware. We then describe two features of Rigetti's Quantum Cloud Services (QCS) mitigate distinct bottlenecks unlocking state-of-the-art hybrid execution speeds.

9:30 AM **31.2** Scalable Quantum Computing Infrastructure Based on Superconducting Electronics (Invited)
O. Mukhanov, A. Kirichenko, C. Howington, J. Walter, M. Hutchings, I. Vernik, D. Yohannes, K. Dodge, A. Ballard, B. L.T. Plourde, A. Opremcak, C.-H. Liu, R. McDermott, SeeQC, Inc., Syracuse University, University of Wisconsin

Superconducting SFQ circuits proximally located to the qubit or sensor arrays can be the technology of choice due to its low power, 10^{-21} Joule to per switching at 20 mK. These circuits can be engineered to produce the minimal back action to qubits.

9:55 AM **31.3** Silicon Hard-Stop Spacers for 3D Integration of Superconducting Qubits (Invited)
Bethany Niedzielski, David Kim, Mollie Schwartz, Danna Rosenberg, Greg Calusine, Rabi Das, Alexander Melville, Jason Plant, Livia Racz, Jonilyn Yoder, Donna Ruth-Yost, William Oliver, Massachusetts Institute of Technology, MIT Lincoln Laboratory

We demonstrate improved planarity of bonded superconducting qubit chips by utilizing hard-stop silicon spacer posts. We demonstrate high-quality factor resonators on the etched surface and measure qubit coherence (T_1, $T_{<sub>2,echo}$ > 40 μs) in the presence of silicon posts as near as 350 μm to the qubit.

10:20 AM **31.4** A Sparse Spin Qubit Array with Integrated Control Electronics (Invited)
Jelmer Boter, Juan Pablo Dehollain, Jeroen van Dijk, Toivo Hensgens, Richard Versluis, James Clarke, Menno Veldhorst, Fabio Sebastiano, Lieven Vandersypen, Delft University of Technology, Netherlands Organisation for Applied Scientific Research (TNO), Intel Corporation, University of Technology Sydney

Current implementations of quantum computers suffer from large numbers of control lines per qubit, becoming unmanageable with system scale up. Here, we discuss a sparse spin-qubit architecture featuring integrated control electronics significantly reducing the off-chip wire count. This quantum classical hardware integration closes the feasibility gap towards a CMOS quantum computer.

10:45 AM **31.5** High Volume Electrical Characterization of Semiconductor Qubits (Invited)
R. Pillarisetty, H.C. George, T.F. Watson, L. Lampert, N. Thomas, S. Bojarski, P. Amin, R. Caudillo, E. Henry, N. Kashani, P. Keys, R. Kotlyar, F. Luthi, D. Michalak, K. Millard, J. Roberts, J. Torres, O. Zietz, T. Krähenmann, A.-M. Zwerver, M. Veldhorst, G. Scappucci, L.M.K. Vandersypen, J.S. Clarke, Intel Corporation, QuTech and Kavli Institute of Nanoscience, TU Delft

Perhaps the greatest challenge facing quantum computing hardware development is the lack of a high throughput electrical characterization infrastructure at the cryogenic temperatures required for qubit measurements. In this article, we discuss our efforts to develop a high volume cryogenic electrical characterization line to guide 300mm spin qubit process development.

11:10 AM **31.6** Qubit read-out in Semiconductor Quantum Processors: Challenges and Perspectives (Invited)
T. Meunier, M. Urdampilleta, D. Niegemann, B. Jadot, E. Charion, P.-A. Mortemousque, C. Spence, B. Bertrand, G. Billiot, M. Cassé, L. Hutin, H. Jacquinot, G. Pillonet, N. Rambal, Y. Thonnart, A. Amisse, A. Apra, L. Bourdet, A. Crippa, R. Ezzouch, X. Jehl, R. Maurand, Y.-M. Niquet2, M. Sanquer, B. Venitucci2, S. De Franceschi2 and M. Vinet, Université Grenoble Alpes, CNRS, Institut Néel, CEA, IRIG, CEA, LETI

We report the efforts dedicated towards building a reliable spin read-out for Si spin qubit systems. We review several strategies that are pursued in the semiconductor quantum circuit community. We discuss their performance and their integration potential. We then address the architecture to read-out spin qubits at large scale.

11:35 AM **31.7** Challenges in Scaling-up the Control Interface of a Quantum Computer (Invited)
David Reilly, The University of Sydney, NSW

Challenges at the quantum-classical interface are examined with the goal of architecting a scaled-up quantum computer comprising many thousands of qubits. We propose an interface that leverages cryo-CMOS in concert with protocols that enable parallel readout of qubits via multiplexing. We discuss these sub-systems and outline their advantages.

12:00 PM **31.8** III-V-on-CMOS Devices and Circuits: Opportunities in Quantum Infrastructure (Invited)
Cezar Zota, Thomas Morf, Peter Mueller, Clarissa Convertino, Stefan Filipp, Walter Riess, L. Czornomaz, IBM Research GmbH Zurich Laboratory

We demonstrate 3D-integrated III-V devices and circuits on Si CMOS that offer compact and energy-efficient systems. We also propose novel cryogenic III-V LNAs using quantum confinement that operate with orders of magnitude reduction of power dissipation. Applications in quantum infrastructure are explored, where form-factors and power dissipation are key constraints.