Session 30 - Reliability of Systems and Devices - Memory Reliability and Applications
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 4
Co-Chairs: K. Cheung, NIST
H. Park, SK Hynix

9:05 AM **30.1** Ultra-Low Power Physical Unclonable Function with Nonlinear Fixed-Resistance Crossbar Circuits
Mohammad Reza Mahmoodi, Hussein Nili, Zahra Fahimi, Shabnam Larimian, Hyungjin Kim, Dmitri Strukov, University of California, Santa Barbara

We present a strong PUF design based on crossbar circuits with fixed nonlinear I-V crosspoint devices. The PUF operation was demonstrated using unformed 64×64 crossbar circuits with passively-integrated ReRAM devices. The results show ~4× better circuit density, ~100x less power consumption, and higher robustness compared to prior-work ReRAM-based PUFs.

9:30 AM **30.2** Formation of High Reliability Hydrogen-free MONOS Cells Using Deuterated Ammonia, Masaki Noguchi, Tatsunori Isogai, Hiroyuki Yamashita, Keiichi Sawa, Ryota Fujitsuka, Takanori Yamanaka, Shunsuke Okada, Tomonori Aoyama, Fumiki Aiso, Junko Abe, Yoshihiro Ogawa, Seiji Nakagawa, Hideshi Miyajima, Kioxia Corporation

For high reliability non-volatile memory cell dielectrics, hydrogen-free deuterated CT-SiN and TNL-SiON films are demonstrated by using deuterated ammonia. An ultra-high D/H ratio has been successfully obtained in both films, and these films showed good endurance for program erase stress and data retention properties in MONOS capacitors.

9:55 AM **30.3** Filamentary Statistical Evolution from Nano-Conducting Path to Switching-Filament for Oxide-RRAM in Memory Applications
Ernest Y. Wu, Takashi Ando, Youngseok Kim, Ramachandran Muralidhar, Eduard Cartier, Paul Jamison, Miaomiao Wang, and Vijay Narayanan, IBM Research Division

In this work, we demonstrate the Gumbel statistics, a maxima-value distribution for RRAM conductance as opposed to Weibull model. In contrast to Poisson distribution, we show the underlying spatial statistics for switching-filament is controlled by a binomial distribution. The conglomeration of interacting individual vacancies eventually leads to area-dependent single-filament formation.

10:20 AM **30.4** Pushing On-chip Memories Beyond Reliability Boundaries in Micropower Machine-learning Applications (Invited)
Alfio Di Mauro, Francesco Conti, Pasquale Schiavone, Davide Rossi, Luca Benini, ETH-Zurich, Universidad di Bologna

In today's Deep-Neural-Network accelerators, memory access dominates inference energy. We analyze voltage over-scaling for on-chip memories, and explore the energy efficiency and reliability trade-off. Experimental results on FDX22 silicon demonstrate opportunities to achieve maximum efficiency at negligible end-to-end classification accuracy degradation, operating and designing on-chip memories at heavily-reduced reliability margins.

10:45 AM **30.5** OXRAM for Embedded Solutions on Advanced Node: Scaling Perspectives Considering Statistical Reliability and Design Constraints (Invited)

Jury Sandrini, Laurent Grenouillet, Valentina Meli, Niccolo Castellani, I. Hammad, Sophie Bernasconi, François Aussenac, Sophie Van Duijin, G. Audoit, Marios Barlas, Jean-Francois Nodin, Olivier Billoint, Gabriel Molas, Richard Fournel, Etienne Nowak, Fred Gaillard, Carlo Cagli, CEA-Leti

To scale OXRAM bitcell, both cell and selector devices must be considered. We studied scaled OXRAM reliability down to 30nm and provide BER reducing strategies. We illustrate how scaled transistors meet OXRAM voltage requirements and demonstrate an OXRAM integration in 28nm-FDSOI. Eventually we present a 32Mb+ECC design solution in 40nm.