Session 3 - Advanced Logic Technology - Monolithic 3D Integration and BEOL Transistors
Monday, December 9, 1:30 p.m.
Grand Ballroom B
Co-Chairs: S. Eccofey, Universite de Sherbrooke
P. Baars, Globalfoundries

1:35 PM **3.1** Monolithic 3D BEOL FinFET Switch Arrays Using Location-Controlled-Grain Technique in Voltage Regulator with Better FOM than 2D Regulators
Ping-Yi Hsieh, Yi-Jui Chang, Pin-Jun Chen, Chun-Liang Chen, Chih-Chao Yang, Po-Tsang Huang, Yi-Jing Chen, Chih-Ming Shen, Yu-Wei Liu, Chien-Chi Huang, Ming-Chi Tai, Wei-Chung Lo, Chang-Hong Shen, Jia-Min Shieh, Da-Chiang Chang, Kuan-Neng Chen, Wen-Kuan Yeh, and Chenming Hu, Taiwan Semiconductor Research Institute, National Chiao Tung University, Industrial Technology Research Institute, University of California, Berkeley

Monolithic 3D BEOL-FinFET switch arrays are demonstrated in large single crystalline Si islands (2.56 μm^2), whose location, size and shape are determined by design. Details of the improved LCG technique is presented. A voltage regulator implemented with the BEOL switch arrays shows better theoretical FOM(0.089ns) than 2D voltage regulators(0.43ns).

2:00 PM **3.2** 3D-Stacked CAAC In-Ga-Zn Oxide FETs with Gate Length of 72 nm
Masashi Oota, Yoshinori Ando, Kazuki Tsuda, Satoru Oshita, Akio Suzuki, Kunihiro Fukushima, Shuhei Nagatsuka, Tatsuya Onuki, Ryota Hodo, Takayuki Ikeda, Shunpei Yamazaki, Semiconductor Energy Laboratory Co., Ltd

We have fabricated two monolithic 3D-stacked c-axis aligned crystalline In-Ga–Zn oxide FETs (CAAC-IGZO FETs) with a gate length of 72 nm using CAAC-IGZO as the channel material. A memory cell using the CAAC-IGZO FETs has long-term data retention, high-speed operation, and high endurance.

2:25 PM **3.3** Monolithic 3D SRAM-CIM Macro Fabricated with Stackable Gate-All-Around MOSFETs
Fu-Kuo Hsueh, Chun-Ying Lee, Cheng-Xin Xue, Chang-Hong Shen, Jia-Min Shieh, Bo-Yuan Chen, Yen-Cheng Chiu, Hsiu-Chih Chen, Ming-Hsuan Kao, Wen-Hsien Huang, Kai-Shin Li, Chien-Ting Wu, Kun-Lin Lin, Kun-Ming Chen, Guo-Wei Huang, Meng-Fan Chang, Chenming Hu, Wen-Kuan Yeh, Taiwan Semiconductor Research Institute, National Tsing Hua University, National Chiao Tung University, University of California Berkeley

For the first time, below 400ºC-fabricated gate-all-around (GAA) transistor fabrication process was demonstrated with monolithic computing-in-memory circuit. The 3D stackable GAA MOSFETs exhibit record-high $I_{on}I_{off}$ ratio (10^{8}) Moreover, the stackability of the GAA MOSFETs and the differential output of dual-mode 10T SRAM readout enable 2x throughput in the CIM circuitry.

2:50 PM *COFFEE BREAK*

3:40 PM **3.4** Inter-tier Dynamic Coupling and RF Crosstalk in 3D Sequential Integration
Petros Sideris, José Lugo-Alvarez, Perrine Batude, Laurent Brunet, Pablo Acosta-Alba, Sebastien Kerdiles, Claire Fenouillet-Beranger, Gilles Sicard, Olivier Rozeau, François Andrieu, Jean-Pierre Colinge, Gérard Ghibaudo, Christoforos Theodorou, CEA-Leti, IMEP-LAHC

An extensive analysis of the intertier dynamic coupling and RF crosstalk of digital circuits in 3D Sequential Integration concludes on the necessity of a Ground Plane insertion for several applications. A novel

integration scheme of a polysilicon Ground Plane shows more than 20dB of RF crosstalk suppression up to 100GHz.

4:05 PM **3.5** BEOL Compatible 15-nm Channel Length Ultrathin Indium-Tin-Oxide Transistors with I_{on} = 970 μA/μm and On/off Ratio Near 10^{11} at V_{ds} = 0.5 V

Shengman Li, Mengchuan Tian, Chengru Gu, Runsheng Wang, Mengfei Wang, Xiong Xiong, Xuefei Li, Ru Huang, Yanqing Wu, Peking University, Huazhong University of Science and Technology

We fabricate ultrathin-body (3.5 nm) sub-100-nm channel length indium-tin-oxide transistors with ultrahigh on/off ratio near 10^{11} where the 15-nm-long ITO transistor exhibits I_{dmax} of 970 μA/μm at V_{ds} = 0.5 V. We demonstrated a record fast stage delay of 0.49 ns/stage for a 5-stage ring oscillator based on BST inverter.