Session 29 - Advanced Logic Technology - High Mobility Ge-Based Channel Devices
Wednesday, December 11, 9:00 a.m.
Grand Ballroom B
Co-Chairs: Y. Zhao, Zhejiang University
T. Yamaguchi, Renesas Electronic Corp.

**9:05 AM** **29.1** Strain and Surface Orientation Engineering in Extremely-thin Body Ge and SiGe-on-insulator MOSFETs Fabricated by Ge Condensation
Kwang-Won Jo, Cheol-Min Lim, Wu-Kang Kim, Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi, The University of Tokyo

We demonstrate a new strain control technology to change high compressive strain into tensile strain in GOI, resulting in operation of 2.5-nm-thick tensile strain GOI n-MOSFETs with electron mobility of 777 cm2/Vs. Also, (110)-oriented compressive strain $Si_{0.46}Ge_{0.54}$OI p-MOSFETs with hole mobility of 837 cm2/Vs has been realized by Ge condensation.

**9:30 AM** **29.2** Ge Oxide Scavenging and Gate Stack Nitridation for Strained $Si_{0.7}Ge_{0.3}$ pFinFETs Enabling 35% Higher Mobility than Si
Hiroaki Arimura, Kurt Wostyn, Lars-Ake Ragnarsson, Elena Capogreco, Adrian Chasin, Thierry Conard, Stephan Brus, Paola Favia, Jacopo Franco, Jerome Mitard, Steven Demuynck, Naoto Horiguchi, imec

We have demonstrated multiple ways to reduce the $D_{IT}$ of Si-cap-free low-Ge-content (25-30%) SiGe gate stack. The Dit is reduced by Ge oxide scavenging, nitridation and optimized high-pressure anneal. 8-nm-wide strained scaled $Si_{0.7}Ge_{0.3}$ pFinFET with the optimized gate stack demonstrated 35% mobility improvement over Si counterpart.

**9:55 AM** **29.3** First Vertically Stacked Tensily Strained $Ge_{0.98}Si_{0.02}$ nGAAFETs with No Parasitic Channel and $L_G$ = 40 nm Featuring Record $I_{ON}$ = 48 μA at $V_{OV}$=$V_{DS}$=0.5V and Record $G_{m,max}$(μS/um)/$SS_{SAT}$(mV/dec) = 8.3 at $V_{DS}$=0.5V
Chien-Te Tu, Yu-Shiang Huang, Fang-Liang Lu, Hsiao-Hsuan Liu, Chung-Yi Lin, Yi-Chun Liu, Chee Wee Liu, National Taiwan University

Si incorporation as small as 2% into Ge achieves etching selectivity of Ge over $Ge_{0.98}Si_{0.02}$. The infrared response can confirm the removal of the parasitic channel. Record $I_{ON}$ of 48 μA at $V_{OV}$=$V_{DS}$=0.5V and record Q of 8.3 at $V_{DS}$=0.5V with $L_G$ = 40 nm are achieved among Ge nFETs.

**10:20 AM** **29.4** Enabling Sub-5nm CMOS Technology Scaling: Thinner and Taller! (Invited)
Julien Ryckaert, Myung Hee Na, Pieter Weckx, Doyoung Jang, Pieter Schuddinck, Bilal Chehab, Sudhir Patli, Satadru Sarkar, Odysseas Zografos, Rogier Baert, Diederik Verkest, imec

Scaling beyond 5nm will bring us into the post FinFET era where new device architectures optimized for CMOS logic scaling will be required. In this paper, the evolution to vertically stacked Nanosheets, Forksheet, and finally CFET are reviewed in conjunction with buried power rails and wrap around contact.

**10:45 AM** **29.5** First Stacked $Ge_{0.88}Sn_{0.12}$ pGAAFETs with Cap, $L_G$=40nm, Compressive Strain of 3.3%, and High S/D Doping by CVD Epitaxy Featuring Record $I_{ON}$ of 58μA at $V_{OV}$=$V_{DS}$= -0.5V, Record $G_{m,max}$ of 172μS at $V_{DS}$= -0.5V, and Low Noise

Yu-Shiang Huang, Chung-En Tsai, Chien-Te Tu, Hung-Yu Ye, Yi-Chun Liu, Fang-Liang Lu, Chee Wee Liu, National Taiwan University

Record [Sn]=12% and record compressive strain of 3.3% among GeSn 3D transistors to enhance the $I_{ON}$ are demonstrated by CVD epitaxy. For the first time, in-situ $Ge_{0.95}Sn_{0.05}$ caps are grown on stacked $Ge_{0.88}Sn_{0.12}$ channels to improve interface quality and separate carriers from the interface to achieve high mobility. LG is scaled down to 40nm to further boost the $I_{ON}$. Low channel doping and high S/D doping ([B]peak~1E21cm-3 ) can suppress the impurity scattering in the channels and reduce the contact resistivity for the S/D, respectively, to reveal the intrinsic merit of the high mobility of GeSn. The stacked 3 $Ge_{0.88}Sn_{0.12}$ nanosheets achieve record ION of 58μA at $V_{OV}$=$V_{DS}$= -0.5V and record Gm,max of 172μS at $V_{DS}$= -0.5V among GeSn pFETs, and the performance is comparable to mature Si FinFETs, stacked Si channels, and stacked Ge channels. The caps as barriers on the $Ge_{0.88}Sn_{0.12}$ channels decrease the low frequency noise by reducing trapping/detrapping between the GeSn channels and the gate dielectrics.

**11:10 AM** **29.6** First Demonstration of Vertical $Ge_{0.92}Sn_{0.08}$/Ge and Ge GAA Nanowire pMOSFETs with Low SS of 66 mV/dec and Small DIBL of 35 mV/V

Mingshan Liu, Stefan Scholz, Konstantin Mertens, JinHee Bae, Jean-Michel Hartmann, Joachim Knoch, Dan Buca, Qing-Tai Zhao, Forschungszentrum Juelich, RWTH Aachen University, CEA-Leti

We demonstrate for the first time, vertical $Ge_{0.92S}Sn_{0.08}$Ge and Ge GAA nanowire pMOSFETs. High performance 20nm diameter NW Ge pFETs exhibit low SS (66 mV/dec), small DIBL (35 mV/V) and high $I_{ON}I_{OFF}$ ($3\times10^6$). Significant improvements were achieved by adopting $Ge_{0.9}$>$Sn_{0.08}$Ge heterostructure showing 32% $I_{ON}$ enhancement compared with Ge device.

**11:35 AM** **29.7** 300mm Heterogeneous 3D Integration of Record Performance Layer Transfer Germanium PMOS with Silicon NMOS for Low Power High Performance Logic Applications (Late News)

Willy Rachmady, Ashish Agrawal, Seung Hoon Sung, Gilbert Dewey, Siddharth Chouksey, Benjamin Chu-Kung, Giselle Elbaz, Paul Fischer, Cheng-Ying Huang, Kimin Jun, Brian Krist, Matthew Metz, Thoe Michaelos, Brennen Mueller, Adedapo Oni, Rajat Paul, Anh Phan, Paul Sears, Tushar Talukdar, Jessica Torres, Bob Turkot, Larry Wong, Hui Jae Yoo, Jack Kavalieros, Intel Corporation

We report a short channel high performance Ge PMOS integrated with Si NMOS in sequential monolithic 3D stacking. A layer transfer Ge PMOS with record ION = 497 uA/um at IOFF = 8nA/um and ION = 630 uA/um at IOFF = 100nA/um and VDS= -0.5V is achieved.