Session 28 - Memory Technology - Charge Based Memory and Emerging Memories
Wednesday, December 11, 9:00 a.m.
Grand Ballroom A
Co-Chairs: P. Kalavade, Intel
Y. Dong, Micron

9:05 AM **28.1** 3D Semicircular Flash Memory Cell: Novel Split-Gate Technology to Boost Bit Density

Makoto Fujiwara, Tetsu Morooka, S. Nagashima, T. Kato, N. Fukuda, N. Kariya, T. Ogura, T. Kurusu, Y. Shimada, T. Ishikawa, Y. Arayashiki, K. Hirayama, Y. Koyama, S. Kashiyama, W. Cai, Y. Goki, K. Sawa, D. Ikeno, M. Nishikawa, Y. Uchiyama, N. Ohtani, F. Arai, and M. Kondo, Kioxia Corporation, Yokkaichi, Mie, Japan, Western Digital Corporation

Three-dimensional semicircular flash memory cells have been developed for the first time. Properly designed semicircular floating-gate cells achieve superior program/erase characteristics at much smaller cell size relative to circular charge-trap cells. The semicircular floating-gate cell is a promising candidate for higher memory density at a lower number of stacking layers.

9:30 AM **28.2** A Novel Double-Density Hemi-Cylindrical (HC) Structure to Produce More than Double Memory Density Enhancement for 3D NAND Flash

Hang-Ting Lue, Teng-Hao Yeh, Pei-Ying Du, Roger Lo, Wei-Chen Chen, Tzu-Hsuan Hsu, Chiatze Huang, Guan-Ru Lee, Chih-Ping Chen, Yu-Wei Jiang, Min-Feng Hung, Yan-Ru Su, Li-Yang Liang, Chih-Wei Hu, Chia-Jung Chiu, Keh-Chung Wang, and Chih-Yuan Lu, Macronix International Co., Ltd

A novel hemi-cylindrical (HC) 3D NAND Flash is demonstrated. HC 3D NAND squeezes the gate-all-around (GAA) hole, followed by a slit cut to split the GAA device to produce ~ 2.6 times of memory density increase. Good 100K PE cycling endurance and post 10K-cycled 150C retention are demonstrated.

9:55 AM **28.3** Metal-Assisted Solid-Phase Crystallization Process for Vertical Monocrystalline Si Channel in 3D Flash Memory

Hidenori Miyagawa, Haruka Kusai, Riichiro Takaishi, Tomoya Kawai, Yuuichi Kamimuta, Toshiya Murakami, Keiko Ariyoshi, Takanori Asano, Masakazu Goto, Makoto Fujiwara, Yuichiro Mitani, Tomoyuki Obu and Hideaki Aochi, Institute of Memory Technology Research & Development, Kioxia Corporation, Western Digital Corporation

In order to improve the channel conductance of 3D flash memory cell, metal induced lateral crystallization (MILC) process has been applied to channel Si in a vertical memory holes and demonstrated superior device characteristics and those uniformities with maintaining memory performance and reliability.

10:20 AM **28.4** A Fully Integrated Low Voltage DRAM with Thermally Stable Gate-first High-k Metal Gate Process (Invited)

Sung Ho Jang, Junhee Lim, Joon Han, Juyeon Jang, Jaehyun Yeo, Chanmin Lee, Sungkweon Baek, Jaehoon Lee, Jong-Ho Lee, Satoru Yamada, Kyupil Lee, Samsung Electronics

A 35nm node 4Gbit LPDDR3 prototype with high-k metal gate (HKMG) peripheral transistors is implemented for the first time using processes that are fully compatible with those of conventional

commercial DRAMs with poly/SiON (PSiON) transistors. This paper describes that the HKMG transistors in the peripheral circuits drastically reduce operating voltage.

10:45 AM **28.5** First Demonstration of Field-free SOT-MRAM with 0.35 ns Write Speed and 70 Thermal Stability under 400°C Thermal Tolerance by Canted SOT Structure and its Advanced Patterning/SOT Channel Technology
Hiroaki Honjo, Anh Nguyen Thi Van, Toshinari Watanabe, Takashi Nasuno, Chaoliang Zhang, Takaho Tanigawa, Sadahiko Miura, Hirofumi Inoue, Masaaki Niwa, Toru Yoshizuka, Yasuo Noguchi, Mitsuo Yasuhira, Akira Tamakoshi, Masanori Natsui, Yitao Ma, Hiroki Koike, Yu Takahashi, Kaito Furuya, Hui Shen, Shunsuke Fukami, Hideo Sato, Shoji Ikeda, Takahiro Hanyu, Hideo Ohno, T. Endo, Tohoku University

For the first time, we demonstrated field-free 55nm-SOT MRAM with developed canted SOT device and its advanced integration process that achieved write speed of 0.35ns, thermal stability factor of 70 enough for non-volatile memory, and high TMR ratio of 167% under 400°C thermal tolerance for 300mm full compatible BEOL process.

11:10 AM **28.6** Field-Free Switching of Perpendicular Magnetization through Voltage-Gated Spin-Orbit Torque
Shouzhong Peng, Jiaqi Lu, Weixiang Li, Lezhi Wang, H. Zhang, Xiang Li, Kang Wang, Weisheng Zhao, Beihang University, University of California, Los Angeles

We experimentally demonstrate the field-free switching of perpendicular magnetization by the combination of spin-orbit torque (SOT), exchange bias (EB) and voltage-controlled magnetic anisotropy (VCMA) in the IrMn/CoFeB/MgO structure. A high-density and ultra-low-power (6.2 fJ/bit) voltage-gated spintronic memory is proposed and successfully verified by both experiments and simulations.

11:35 AM **28.7** A Multilevel FeFET Memory Device based on Laminated HSO and HZO Ferroelectric Layers for High-Density Storage
Tarek Ali, Patrick Polakowski, Kati Kühnel, Malte Czernohorsky, Thomas Kämpfe, Matthias Rudolph, Björn Pätzold, David Lehninger, Franz Müller, Ricardo Olivo, Maximilian Lederer, Raik Hoffmann, Philipp Steinke, Katrin Zimmermann, Uwe Mühle, Konrad Seidel, Johannes Mueller, Fraunhofer IPMS-Center Nanoelectronic Technologies (CNT)

We report 1-3 bit/cell FeFET operation through optimized HSO and HZO ferroelectric laminate layers using alumina interlayers. Memory window up to 3.5V, switching speed of 300ns, 10 years retention, and 10^4 endurance are reported. The gate stack lamination merits are discussed with insight potential of FeFET as an MLC memory.

12:00 PM **28.8** A Novel Ferroelectric Superlattice Based Multi-Level Cell Non-Volatile Memory
Kai Ni, Jeffrey Smith, Huacheng Ye, Benjamin Grisafe, G. Bruce Rayner, Andrew Kummel, Suman Datta, University of Notre Dame, Kurt J. Lesker Co., University of California, San Diego

We demonstrate a novel and scalable approach to implement multi-level cell memory using ferroelectric (FE) superlattice, which outperforms previous multi-state FE memory implemented using partial polarization switching, from the standpoint of device-to-device variation. We experimentally demonstrate

a 2-bit/cell FE superlattice memory and simulate a 3-bit/cell memory with excellent device-to-device variation.