Session 23 - Emerging Device and Compute Technology - Emerging Devices for Extending Moore's Law
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 6
Co-Chairs: Y. Chai, The Hong Kong Polytechnic University
T. Mueller, Vienna University of Technology

2:20 PM **23.1** Importance of Interconnects: A Technology-System-Level Design Perspective (Invited)
Jie Liang, Aida Todri-Sanial, University of Montpellier

For CVD MoS_2 FETs we demonstrate that downscaling the top-contact length to 13nm induces no penalty on the characteristics, experimentally confirming edge injection with I_{on}=250µA/µm for 50nm SiO_2 gate oxide. This is equally valid for thinner 4nm HfO_2 gate oxide, where the switching characteristics improve with SS_{min}=80mV/dec

2:45 PM **23.2** Ultra-scaled MOCVD MoS_2 MOSFETs with 42nm Contact Pitch and 250µA/µm Drain Current
Quentin Smets, Goutham Arutchelvan, Julien Jussot, Devin Verreck, Inge Asselberghs, Ankit Nalin Mehta, Abhinav Gaur, Dennis Lin, Salim El Kazzi, Benjamin Groven, Matty Caymax, Iuliana Radu, imec, KU Leuven

For CVD MoS_2 FETs we demonstrate that downscaling the top-contact length to 13nm induces no penalty on the characteristics, experimentally confirming edge injection with I_{on}=250µA/µm for 50nm SiO_2 gate oxide. This is equally valid for thinner 4nm HfO_2 gate oxide, where the switching characteristics improve with SS_{min}=80mV/dec

3:10 PM **23.3** Highly Area-Efficient Low-Power SRAM Cell with 2 Transistors and 2 Resistors
Jiayi Li, Jingyu Li, Yi Ding, Chunsen Liu, Xiang Hou, Huawei Chen, Yan Xiong, Yang Chai, David Wei Zhang, Peng Zhou, Fudan University, The Hong Kong Polytechnic University

We demonstrate a highly area-efficient 2-transistor/2-resistor static-random-access-memory cell with high read/write stability composed of novel two-surface-channel transistors, using two-dimensional layered MoS_2. The read and write power of the memory devices are 0.035 µW and 0.036 µW, respectively, indicating a promising application in low-power electronics and highly area-efficient chips.

3:35 PM **23.4** Area-Selective-CVD Technology Enabled Top-Gated and Scalable 2D-Heterojunction Transistors with Dynamically Tunable Schottky Barrier
Chao-Hui Yeh, Wei Cao, Arnab Pal, Kamyar Parto, Kaustav Banerjee, University of California, Santa Barbara

In this work, graphene source/drain heterojuction 2D FETs enabled by area-selective-CVD technology are demonstrated, in terms of reducing the contact and series resistances. Record-high ON-current (~273 µA/µm) and ultra-low contact resistance (~670 ohm·µm) are achieved in a monolayer 2D-FET. Scaling analysis confirms the sub-10 nm prospect of this device.

4:00 PM *COFFEE BREAK*

4:25 PM **23.5** Transient Negative Capacitance of Silicon-doped HfO_2 in MFMIS and MFIS Structures: Experimental Insights for Hysteresis-free Steep Slope NC FETs

Carlotta Gastaldi, Ali Saeidi, Matteo Cavallieri, Igor Stolichnov, Paul Muralt, Adrian Ionescu, EPFL

We experimentally explore the transient negative capacitance effect in ferroelectric high-k gate stacks using multi-ferroelectric domain Si:HFO2 with and without metal plane. We demonstrate that despite the smaller gain, the MFIS structure provides hysteresis-free stable performance boosting in all the regimes of operation of a 14nm UTB SOI MOSFET.

4:50 PM **23.6** Bi-directional Sub-60mV/dec, Hysteresis-Free, Reducing Onset Voltage and High Speed Response of Ferroelectric-AntiFerroelectric $Hf_{0.25}Zr_{0.75}O_2$ Negative Capacitance FETs
Min-Hung Lee, Kuan-Ting Chen, Chun-Yu Liao, Guo-Yu Siang, Chieh Lo, Hong-Yu Chen, Yi-Ju Tseng, Chung-Yu Chueh, Ching Chang, Yen-Yun Lin, Yu-Jun Yang, F-C Hsieh, Shu-Tong Chang, Ming-Han Liao, Kai-Shin Li, Chee Wee Liu, National Taiwan Normal University, National Taiwan University, National Chung Hsing University, Taiwan Semiconductor Research Institute

First demonstration of quasi-antiferroelertic $Hf_{0.25}Zr_{0.75}O_2$ (QAFE-HZO) NC-FET with non-hysteretic bi-directional sub-60mV/dec (SS_{for}=51mV/dec, SS_{rev}53mV/dec, ΔV_T1mV) for low onset voltage, N-DIBL, NDR, and high speed response. An operation window for non-hysteretic steep SS of QAFE-HZO as compared with accompanying a non-negligible hysteresis of FE-HZO(Zr=50%). NC time is improved 48-77% from transient response.

5:15 PM **23.7** Direct Observation of Interface Charge Behaviors in FeFET by Quasi-Static Split C-V and Hall Techniques: Revealing FeFET Operation
Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi, The University of Tokyo

Quasi-static split C-V is proposed as a novel method to monitor polarization and charge distribution in FeFETs. Our method, extracting Q-V_g loops directly from FeFET structures, is a powerful tool to understand the real operation and device physics of FeFETs including the memory window and the NC effect.