Session 21 - Reliability of Systems and Devices - Emerging Transistor Reliability and Pertinent Strategies
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 4
Co-Chairs: F. Schanovsky, Global TCAD Solutions BmbH
B. Weir, Broadcom

2:20 PM **21.1** Addressing Reliability Challenges in Advance Nodes for Commercial and Automotive Application (Invited)
Tanya Nigam, Peter Paliwoda, Xinggong Wan, Andreas Kerber, GLOBALFOUNDRIES

Building in reliability is critical during technology development, as we continue scaling or incorporating additional functionality. In this paper Front End Of Line methodologies for DC, Equivalent AC and correlation to RO/SRAM/Logic degradation and failure are presented. Additionally, Self-Heating and Variability characterization for commercial and automotive applications are discussed.

2:45 PM **21.2** A Physics-aware Compact Modeling Framework for Transistor Aging in the Entire Bias Space
Zhicheng Wu, Jacopo Franco, Philippe Roussel, Stanislav Tyaginov, Brecht Truijen, Michiel Vandemaele, Geert Hellings, Nadine Collaert, Guido Groeseneken, Dimitri Linten, Ben Kaczer, imec, KU Leuven

A unified compact modeling framework of device aging is proposed and verified on FinFET technology

3:10 PM **21.3** Understanding and Physical Modeling Superior Hot-Carrier Reliability of Ge pNWFETs
Stanislav Tyaginov, Al-Moatasem El-Sayed, Alexander Makarov, Adrian Chasin, Hiroaki Arimura, Michiel Vandemaele, Markus Jech, Elena Capogreco, Liesbeth Witters, Alexander Grill, An De Keersgieter, Geert Eneman, Dimitri Linten, Ben Kaczer, imec, Nanolayers, TU Vienna

We accurately model degradation and the time-to-failure measured during hot-carrier stress in Ge and Si pNWFETs. The superior time-to-failure in Ge devices has been explained by a much higher energy (5.5eV) needed to break Ge-O bonds (precursors) and form O-vacancies (defects) compared to the Si-H bond rupture energy (2.6eV).

3:35 PM *COFFEE BREAK*

4:00 PM **21.4** New Insight into MOS Gate Stack Formations on Ge and SiGe from Thermodynamics, Reaction Kinetics and Nanoscale Engineering
Akira Toriumi, Tomonori Nishimura, The University of Tokyo

Oxidation and thermal robustness of gate stacks in Ge and SiGe are intensively investigated. The key points of new understanding are twofold. One is that GeO_2Ge interface reaction occurs inhomogeneously, and the other is that Si in SiGe is oxidized by GeO_2 and Ge agglomeration also occurs on SiGe surface.

4:25 PM **21.5** Novel Concept of the Transistor Variation Directed Toward the Circuit Implementation of Physical Unclonable Function (PUF) and True-random-number Generator (TRNG)
Y. Xiao, E. R. Hsieh, Steve Chung, T. P. Chen, S. A. Huang, T. J. Chen, Osbert Cheng, National Chiao Tung University, UMC

We use a unique feature of S/D variations of 14nm FinFET to realize PUF and TRNG. The S/D variation was used to design PUF. The defect generated traps was observed from a new Ib-RTN which was used to design TRNG. Reliability tests of array and circuits are presented.

4:50 PM **21.6** Physical Insights on Steep Slope FEFETs including Nucleation-Propagation and Charge Trapping

Yang Xiang, Marie Garcia Bardon, Md Nur Kutubul Alam, Mischa Thesberg, Ben Kaczer, Philippe Roussel, Mihaela Ioana Popovici, Lars-Ake Ragnarsson, Brecht Truijen, Anne S. Verhulst, Bertrand Parvais, Naoto Horiguchi, Guido Groeseneken, J. van Houdt, imec, KU Leuven, Vrije Universteit Brussel, TU Wien

We present an analysis of steep slope FEFETs including statistical multidomain nucleation-propagation and high-K hafnia-oxide charge trapping, based on a compact model validated on transistor I-V measurement. The proposed field-independent propagation proves key to explaining the steep slope. Trapping is shown to assist polarization-switching and enlarge the detrimental I-V hysteresis