Session 2 - Memory Technology - STT-MRAM
Monday, December 9, 1:30 p.m.
Grand Ballroom A
Co-Chairs: G. Hu, IBM TJ Watson Research Center
S. Kang, Qualcomm

1:35 PM **2.1** Demonstration of a Reliable 1 Gb Standalone Spin-Transfer Torque MRAM For Industrial Applications
Sanjeev Aggarwal, Hamid Almasi, Mark DeHerrera, Brian Hughes, Sumio Ikegawa, Jason Janesky, Han Kyu Lee, Hui Lu, Frederick Mancoff, Kerry Nagel, Goei Shimon, Jijun Sun, Tom Andre, Syed Alam, Everspin Technologies Inc.

We demonstrate reliable operation of our 1 Gb standalone STT-MRAM product over a temperature range of -40C to 110C. Well-behaved read and write distributions over 4 sigma enable an endurance lifetime of 2e11 cycles and data retention of 10 years at 85C.

2:00 PM **2.2** 1Gbit High Density Embedded STT-MRAM in 28nm FDSOI Technology
K. Lee, J. H. Bak, Y. J. Kim, C. K. Kim, A. Antonyan, D. H. Chang, S. H. Hwang, G. W. Lee, N. Y. Ji, W. J. Kim, J. H. Lee, B. J. Bae, J. H. Park, I. H. Kim, B. Y. Seo, S. H. Han, Y. Ji, H. T. Jung, S. O. Park, O. I. Kwon, J. W. Kye, Y. D. Kim, S. W. Pae, Y. J. Song, G. T. Jeong, K. H. Hwang, G. H. Koh, H. K. Kang, and E. S. Jung, Samsung Electronics Co.

High density 1Gb embedded STT-MRAM in 28nm FDSOI technology was successfully demonstrated. Based on the highly reliable and manufacturable eMRAM technology, high yield over 90% was achieved with satisfying read, write function and 10 years retention. Improved endurance up to 1E10 cycles was achieved to broaden eMRAM applications.

2:25 PM **2.3** Manufacturable 22nm FD-SOI Embedded MRAM Technology for Industrial-grade MCU and IOT Applications
Vinayak Bharat Naik, Kangho Lee, Kazutaka Yamane, Robin Chao, Jae-Hyun Kwon, Naganivetha Thiyagarajah, Nyuk Leong Chung, Suk Hee Jang, Behtash Behin-Aein, Jia Hao Lim, Tae Young Lee, Wah Peng Neo, Hemant Dixit, Sivabalan K, Lian Choo Goh, Timothy Ling, Jay Hwang, Dinggui Zeng, Jia Wen Ting, Eng Huat Toh, Lei Zhang, Rachel Low, Nivetha Balasankaran, Li Ying Zhang, K. W. Gan, L. Y. Hau, J. Mueller, B. Pfefferling, O. Kallensee, S. L. Tan, C. S. Seet, Y. S. You, S. T. Woo, E. Quek, S. Y. Siah, J. Pellerin, GLOBALFOUNDRIES

We demonstrate the manufacturable 22nm FD-SOI embedded-MRAM by achieving product functionality and reliability in package level at -40~125 °C. The product reliability is confirmed by passing LTOL, HTOL, 1M endurance and 5x-solder reflows tests. In addition, we demonstrate the macro capability to cover magnetic immunity of >500 Oe.

2:50 PM *COFFEE BREAK*

3:15 PM **2.4** 2 MB Array-Level Demonstration of STT-MRAM Process and Performance Towards L4 Cache Applications
Juan G. Alzate, Umut Arslan, Peng Bai, Justin Brockman, Yu-Jin Chen, Nilanjan Das, Kevin Fischer, Tahir Ghani, Philip Heil, Patrick Hentges, Rawshan Jahan, Aaron Littlejohn, Mohammad Mainuddin, Daniel Ouellette, James Pellegren, Tanmoy Pramanik, Conor Puls, Pedro Quintero, Tofizur Rahman, Meenakshi Sekhar, Bernhard Sell, Mansi Seth, Andrew Smith, Angeline Smith, Liqiong Wei, Chris Wiegand, Oleg Golonzka, Fatih Hamzaoglu, Intel Corporation

We demonstrate 2 MB arrays of scaled-size MTJ devices capable of meeting L4 Cache specifications across all proposed temperatures of operation. The technology achieves ECC-correctable bit fail rates for a 20 ns write time, a 4 ns read time, endurance of 10^{12} cycles, and retention of 1 second at 110C.

3:40 PM **2.5** A Novel Integration of STT-MRAM for On-chip Hybrid Memory by Utilizing Non-Volatility Modulation

Jeong-Heon Park, Joonmyoung Lee, Junho Jeong, UngHwan Pi, Whan Kyun Kim, SungChul Lee, Eunsun Noh, Kwangseok Kim, Woochang Lim, Shin Kwon, Byoung-Jae Bae, InHo Kim, NaYoung Ji, Kilho Lee, HyunChul Shin, Shin Hee Han, Sohee Hwang, Daeeun Jeong, Junghyuk Lee, S. Nam, H. Kang, E. Jung, Samsung Electronics Company Ltd.

We demonstrate a novel way of integrating STT-MRAM for on-chip hybrid memory which exhibits either features of high-retention or high-speed implemented in separate zones in a single chip. For satisfying high-temperature retention requirement, tailored MTJs are shown to support > 10 year retention at 220℃.

4:05 PM **2.6** Spin-transfer Torque MRAM with Reliable 2ns Writing for Last Level Cache Applications

Guohan Hu, Janusz Nowak, Matthias Gottwald, Stephen Brown, Bruce Doris, Christopher D'Emic, Pouya Hashemi, Dimitri Houssameddine, Qing He, Daeshik Kim, Juhyun Kim, Raman Kothandaraman, Gen Lauer, H. K. Lee, Nathan Marchack, Mark Reuter, Ray Robertazzi, Jonathan Sun, Thitima Suwannasiri, Philip Trouilloud, Seonghoon Woo, Daniel Worledge, IBM TJ Watson Research Center

Reliable 2ns switching of STT-MRAM devices was achieved for the first time by demonstrating 100% write-error-rate yield at 1e-6 write-error floor of 254 devices. A single device with less than 1e-11 write-error rate was demonstrated with 2ns write pulses. Reliable 3ns switching was demonstrated with a completely different stack design.

4:30 PM **2.7** 22nm STT-MRAM for Reflow and Automotive Uses with High Yield, Reliability, and Magnetic Immunity and with Performance and Shielding Options (Late News)

William Gallagher, Eric Chien, Tien-Wei Chiang, Jian-Cheng Huang, Meng-Chun Shih, C.Y. Wang, Chih-Hui Weng, Sean Chen, Christine Bair, George Lee, Yi-Chun Shih, Chia-Fu Lee, Po-Hao Lee, Roger Wang, Kuei-Hung Shen, J.J. Wu, Wayne Wang, Harry Chuang, TSMC

We demonstrate high yielding solder-reflow-capable STT-MRAM embedded in 22nm CMOS. The technology supports -40 to 150°C operation and has ten-year native magnetic field immunity >1100 Oe at 25°C at 1ppm bit upset level, with a shield-in-package demonstrating even higher immunity. Trading off retention, higher performance and endurance are also demonstrated.