Sesion 19- Advanced Logic Technology - BEOL and 3D Packaging Innovation
Tuesday, December 10, 2:15 p.m.
Grand Ballroom A
Co-Chairs: H. Shang, TSMC
C. Liu, National Taiwan University

2:20 PM **19.1** Buried Power Rails and Back-side Power Grids: Arm® CPU Power Delivery Network Design Beyond 5nm
Divya Prasad, S. S. Teja Nibhanapudi, Shidhartha Das, Odysseas Zografos, Bilal Chehab, Satadru Sarkar, Rogier Baert, Alex Robinson, Anshul Gupta, Alessio Spessot, Peter Debacker, Diederik Verkest, Jaydeep Kulkarni, Brian Cline, Saurabh Sinha, Arm Reserarch, The University of Texas at Austin, imec

An Arm CPU is designed with buried-power rails (BPR) and back-side power delivery at 3nm node. It is found that careful power-delivery-network design alleviates IR drop but deteriorates the energy with front side power delivery. However, back-side power delivery with BPR eliminates this trade-off demonstrating ~7X improvement in IR drop.

2:45 PM **19.2** Monolithic Heterogeneous Integration of BEOL Power Gating Transistors of Carbon Nanotube Networks with FEOL Si Ring Oscillator Circuits
Chao-Ching Cheng, Chun-Chieh Lu, Tsu-Ang Chao, Ang-Sheng Chou, Tianqi Gao, Jianwen Zhao, Zheng Cui, Hung-Li Chiang, Tzu-Chiang Chen, Lain-Jong Li, H.-S. Philip Wong, Taiwan Semiconductor Manufacturing Company, University of Science and Technology of China, Chinese Academy of Science

High-performance carbon-nanotube (CNT) network transistors are successfully integrated as BEOL power-gating devices onto Si CMOS wafers manufactured using 28-nm process technology. FEOL Si ring-oscillators with BEOL CNT header transistors achieve a similar quiescent current (IDDQ) and comparable active power consumption as compared to the operation without the CNT header transistors.

3:10 PM **19.3** Three-Layer BEOL Process Integration with Supervia and Self-Aligned-Block Options for the 3 nm Node
Victor-Hugo Vega-Gonzalez, Christopher Wilson, Basoene Briggs, Stefan Decoster, J. J. Versluijs, Alicja Lesniewska, Sara Paolillo, Rogier Baert, Harinarayanan Puliyalil, Joost Bekaert, Els Kesters, Quoc Toan Le, Christophe Lorant, Olalla Varela Pedreira, Lieve Teugels, Nancy Heylen, Zaid El-Mekki, Marleen van der Veen, Tomas Webers, Hemant Vats, Luc Rijnders, Miroslav Cupak, Jae Uk Lee, Youssef Drissi, L. Halipre, A.-L. Charley, P. Verdonck, T. Witters, S. V. Gompel, Y. Kimura, N. Jourdan, I. Ciofi, A. Gupta, A. Contino, G. Boccardi, S. Lariviere, L. Dupas, B. De-Wachter, E. Vancoille, F. Lazzarino, M Ercken, P. Debacker, R. Kim, D. Trivkovic, K. Croes, P. Leray, L. Dillemans, Y.-F. Chen, Z. Tokei imec

The integration of a three-layer BEOL process with an intermediate 21 nm pitch level, relevant for the 3 nm node, is demonstrated using full barrier-less Ruthenium dual-damascene metallization. Variations of minimum island, via extension and tip-to-tip were electrically evaluated. Scaling boosters supervia and self-aligned block were investigated. Reliability study included.

3:35 PM *COFFEE BREAK*

4:00 PM **19.4** Heterogeneous Integration Using Omni-Directional Interconnect Packaging
Adel Elsherbini, Shawna Liff, Johanna Swan, Intel Corporation

We present a new packaging building block for 3D integrated circuits; Omni Directional Interconnect (ODI). It enables combining the high bandwidth benefit of 3D stacking with the minimal die area and direct

power delivery of 2D packaging. ODI performance and cost benefits are summarized and the fabrication results are presented.

4:25 PM **19.5** Integrated Deep Trench Capacitor in Si Interposer for CoWoS Heterogeneous Integration

S.Y. Hou, Harry Hsia, C.H. Tsai, K.C. Ting, T.H. Yu, Y.W. Lee, F.C. Chen, W.C. Chiou, C.T. Wang, C.H. Wu, Douglas C.H. Yu, TSMC

High-K based deep trench capacitors have been integrated the first time in the silicon interposer with TSV and fine-pitch interconnects for chip-on-wafer-on-substrate (CoWoS) integration. A specific capacitance density of 340 nF/mm2 is achieved over a large capacitor array, providing a total capacitance of 68 uF per interposer die.

4:50 PM **19.6** Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices (Invited)

D. B. Ingerly, S. Amin, L. Aryasomayajula, A. Balankutty, D. Borst, A. Chandra, K. Cheemalapati, C.S. Cook, R. Criss, K. Enamul, W. Gomes, D. Jones, K.C. Kolluru, A. Kandas, G.-S. Kim, H. Ma, D. Pantuso, C.F. Petersburg, M. Phen-givoni, A.M. Pillai, A. Sairam P. Shekhar, P. Sinha, P. Stover, A. Telang, Z. Zell, Intel Corporation

Presents the key silicon features of Intel's 3D stacking technology, Foveros, as it is used to enable logic-on-logic die stacking. A robust face-to-face die connection is enabled with a high yielding, robust microbump connection. Additionally, we describe the TSVs used for connection to the package along with their electrical properties.