Session 11 - Advanced Logic Technology - Gate-All-Around Device Technologies
Tuesday, December 10, 9:00 a.m.
Grand Ballroom A
Co-Chairs: S. Maitrejean, CEA
K.H. Cho, Samsung

9:05 AM **11.1** Vertical Nanowire and Nanosheet FETs: Device Features, Novel Schemes for Improved Process Control and Enhanced Mobility, Potential for Faster & More Energy-Efficient Circuits
Anabela Veloso, Geert Eneman, Trong Huynh-Bao, Adrian Chasin, Eddy Simoen, Emma Vecchio, Katia Devriendt, Stephan Brus, Erik Rosseel, Andriy Hikavyy, Roger Loo, Vasile Paraschiv, BT Chan, Dunja Radisic, Waikin Li, J. J. Versluijs, Lieve Teugels, Farid Sebaai, Paola Favia, Hugo Bender, Eric Vancoille, Jeroen E. Scheerder, Claudia Fleischmann, Naoto Horiguchi, P. Matagne, imec

We report on p&n vertical gate-all-around nanowire and nanosheet FETs, evaluating the impact of doping and key dimensions on: performance, variability, noise, reliability (junctionless vs. inversion-mode) using RMG, which enables a new scheme for enhanced mobility by stress. Gate (mis)alignment control and their potential as MRAM selector are also discussed.

9:30 AM **11.2** Multiple-Vt Solutions in Nanosheet Technology for High Performance and Low Power Applications
Ruqiang Bao, Koji Watanabe, Jingyun Zhang, Jing Guo, Huimei Zhou, Andrew Gaul, Muthumanickam Sankarapandian, Juntao Li, Alex Hubbard, Reinaldo Vega, Shanti Pancharatnam, Paul Jamison, Miaomiao Wang, Nicolas Loubet, Veeraraghavan Basker, Daniel Dechene, Dechao Guo, Bala Haran, Huiming Bu, Mukesh Khare, IBM Semiconductor Technology Research

We reported an innovative integration scheme to enable volumeless multi-Vt and metal multi-Vt to provide the multi-Vt solutions in NS technology for high performance computing and low power applications. Meanwhile, metal gate boundary control was also developed to enable variable NS widths on the same wafer to satisfy both applications.

9:55 AM **11.3** 3D-carrier Profiling and Parasitic Resistance Analysis in Vertically Stacked Gate-All-Around Si Nanowire CMOS Transistors
Pierre Eyben, Romain Ritzenthaler, An De Keersgieter, Umberto Celano, Thomas Chiarella, Anabela Veloso, Hans Mertens, Vanessa Pena, Gaetano Santoro, Jerome Machillot, Myungsun Kim, Toshihiko Miyashita, Naomi Yoshida, Hugo Bender, Olivier Richard, Kristof Paredis, Lennaert Wouters, Jerome Mitard, Naoto Horiguchi, imec, Applied Materials

We have utilized s-SSRM in order to extract for the first time 3D carrier distributions into multi-channel h-GAA Si NW-CMOSFETs. Good correlation with DIBL characteristics could be established. Thanks to these results and to TCAD simulations we could give a first explanation of the ON-current performance increase of GAA pMOSFETs.

10:20 AM **11.4** A Novel Dry Selective Etch of SiGe for the Enablement of High Performance Logic Stacked Gate-All-Around NanoSheet Devices
Nicolas Loubet, Subhadeep Kal, Cheryl Alix, Shanti Pancharatnam, Huimei Zhou, Curtis Durfee, Michael Belyansky, Nathaniel Haller, Koji Watanabe, Thamarai Devarajan, Jingyun Zhang, Xin Miao, Muthumanickam Sankarapandian, Mary Breton, Robin Chao, Andrew M Greene, L. Yu, J. Frougier, Daniel Chanemougame, Kandabara Tapily, Jeffrey Smith, Veeraraghavan Basker, Aelan Mosden, Peter Biolsi, Trace Hurd, Rama Divakaruni, B. Haran, H. Bu, TEL Technology Center, IBM Research

In this paper, we demonstrate a first of a kind SiGe dry etch technique for the formation of inner spacers and for channel release, enabling stacked NanoSheet (NS) gate-all-around device architectures with a wide range of NS device widths on the same wafer, critical for power/performance optimization of this technology.

10:45 AM COFFEE BREAK

11:10 AM 11.5 Imaging, Modeling and Engineering of Strain in Gate-All-Around Nanosheet Transistors
Shay Reboh, Remi Coquand, Nicolas Loubet, Nicolas Bernier, Emmanuel Augendre, Robin Chao, Juntao Li, Victor Boureau, Jingyun Zhang, Raja Muthinti, Olivier Faynot, Tenko Yamashita, CEA-Leti, IBM Research

3D modelling of strains in GAANS is calibrated on hardware using TEM strain-mapping. Compression of channels due to stress from the encapsulation of source/drain is reversed to tensile after gate stack/contact modules. Si-channel cladded with SiGe illustrates the co-integration of compressive SiGe channels with limited change of the integration flow.

11:35 AM 11.6 Full Bottom Dielectric Isolation to Enable Stacked Nanosheet Transistor for Low Power and High Performance Applications
Jingyun Zhang, J. Frougier, Andrew M Greene, Xin Miao, Lan Yu, Reinaldo Vega, Pietro Montanini, Curtis Durfee, Andrew Gaul, Shanti Pancharatnam, Charlotte D Adams, Heng Wu, Huimei Zhou, Tian Shen, Ruilong Xie, Muthumanickam Sankarapandian, Junli Wang, Koji Watanabe, Ruqiang Bao, Xuefeng Liu, Chanro Park, Hosadurga K Shobha, Praveen Joseph, Dexin Kong, Abraham Arceo De La Pena, J. Li, R. Conti, D. Dechene, N. Loubet, R. Chao, T. Yamashita, R. Robison, V. Basker, K. Zhao, D. Guo, B. Haran, R. Divakaruni, H. Bu, IBM Research

In this paper, full ─BDI ─ is first demonstrated on horizontally stacked Nanosheet device structures with ─ Lmetal 12 nm. The comparison of full ─ BDI scheme ─ vs ─ PTS scheme has been systematically studied. ─BDI scheme can potentially provide: 1) good immunity of sub-channel leakage due to process variation; 2) power-performance co-optimization.

12:00 PM 11.7 First Demonstration of CMOS Inverter and 6T-SRAM Based on GAA CFETs Structure for 3D-IC Applications
S.-W. Chang, P.-J. Sung, T-Y. Chu, D. D. Lu, C. -J. Wang, N.-C. Lin, C.-J. Su, S.-H. Lo, H.-F. Huang, J.-H. Li, M.-K. Huang, Y.-C. Huang, S.-T. Huang, H.-C. Wang, Y.-J. Huang, J.-Y. Wang, L.-W Yu, Y.-F. Huang, F.-K. Hsueh, C.-T. Wu, W. C.-Y. Ma, K.-H. Kao, Y.-J. Lee, C.-L. Lin, R.W. Chuang, K.-P. Huang, S. Samukawa, Y. Li, W.-H. Lee, T.-S. Chao, G.-W. Huang, W.-F. Wu, J.-Y. Li, J.-M. Shieh, W. -K. Yeh, Y.-H. Wang, Taiwan Semiconductor Research Institute, National Cheng Kung University, National Chiao Tung University, National Sun Yat-sen University, Feng Chia University, Industrial Technology Research Institute, Tohoku University, National Taiwan University, National Applied Research Laboratories

CMOS inverters and 6T-SRAM cells based on vertically stacked GAA CFET are experimentally demonstrated, which is promising for 3D-ICs applications. Manufacturing difficulties of vertically stacked source/drain electrodes of the CFET device is overcome by using junctionless transistors. TCAD modeling shows CFET inverter has lower input capacitance than standard CMOS.