Tutorial 4: Cryogenic MOSFET Modeling

Christian Enz, EPFL

There is currently a large effort to try to miniaturize quantum computers taking advantage of solid-state technologies enabling a potentially large number of qubits operating in regimes that allow superposition and entanglement. CMOS is the preferred technology for building the qubit array and mixing it with the control and readout electronics taking advantage of the cryogenic temperature to operate the electronics at lower power and/or faster. The design and optimization of these CMOS analog and digital circuits need a compact transistor model that is valid down to cryogenic temperatures. Unfortunately, the current MOSFET compact models do not scale properly with temperature down to such low temperature. This tutorial will address this limitation. It starts with an assessment of the analog performance at cryogenic temperatures using the simplified EKV MOSFET model. The main effects occurring at cryogenic temperature are then described and a physics-based MOSFET model that scales down to ultra-low temperatures is then presented.