Tutorial 6: 3D Sequential Integration

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3D sequential integration allows vertically stacking several layers of devices with a unique connecting via density above 10^8 via/mm^2. However, the thermal stability of the lower tier(s) constrains the thermal budget of the sequentially processed upper tier(s).

The first aim of this tutorial will be to present the main prospective application sectors, namely (i)Pursuing Moore's law without resorting to MOSFETs scaling ii) Enabling alternative computing paradigms through close proximity between logic and memory units iii) offering new heterogeneous co-integrations schemes for smart sensor arrays iv) adding low cost functionalities above ICs.

Moreover, major 3D sequential integration demonstrations examples will be reviewed revealing the rich diversity of stacked low temperature devices currently under study ranging from traditional low temperature Si MOSFETs, poly-Si TFTs, junction-less devices, carbon nanotubes, oxide semiconductors, etc.

This tutorial will give a synoptic view of all the key enabling process steps required to build high performance Si CMOS with thermal budget preserving the integrity of active devices and interconnects (top channel formation, gate stack reliability, junction's activation, low resistivity gate realization, selective epitaxy, spacer's formation) and will sketch a status on current low temperature device performance with respect to their high temperature counterparts.