3D NAND: Challenges and Potentials, *Jian Chen, Western Digital*

Jian Chen is Senior Vice President of Technology for Western Digital, responsible for the company's overall 3D NAND technology development. Prior to his current role, he was Vice President of Memory System Engineering, led the exploring of novel storage system architecture and eco-system for emerging memories, and managed the memory system group, responsible for the architecture design of USB, CF, SD/µSD, and SSD products from 2007 to 2013. From 1999 to 2007, he started as device manager for the first Toshiba-SanDisk joint project 0.16um 1G MLC NAND development, and involved in all subsequent generations of 2D NAND development in various roles, including 3 years starting the first 300mm joint fab in Yokkaichi Japan. From 1996 to 1999, he worked on the original SanDisk triple-poly NOR technology as device, foundry and FA engineer. Prior to SanDisk, he worked on 3 generations of NOR flash memory at AMD. Holder of over 140 granted US patents, he is co-author of a book chapter on Flash Memory Reliability and JEDEC flash memory reliability standard. He is the author of several key patents that have been used in NAND for over 15 years, such as binary cache, coupling canceling technique, fast programming method and cell airgap. He published the papers that first discovered and coined the term GIDL. He received his MS and Ph.D. in EECS from UC Berkeley, and B.S. in Solid State Device Physics from University of Electronic Science and Technology, Chengdu, China.

Abstract: In our modern data abundant and dominant world, memory and storage are becoming ever more important in the memory and computing hierarch. As an industry, we are gifted with secular and insatiable demand with no end in sight. In the past 30 years, we have successfully met that challenge, scaled the NAND flash cost by more than one million times with 17 generations of 2D and 3D NAND technologies, increased density, performance and functionality, and played critical role in transforming modern mobile world. As successor to the floating gate 2D NAND, charge-trap 3D NAND technology has successfully been developed and entered the 100+ layer era, with various architectures choices that focus on optimization of different parameters. The industry is facing huge challenges in further scaling and cost reduction, with abundant opportunities for Capital tool vendors, for new process and material and architecture innovations. 3D NAND is also quite veritable, with proper design trade-offs, within the same technology generation, it can offer chips with write performance from 10MB/s to 1GB/s, read access time from 100us to 1us, endurance from 1 thousand to 1 million, and cost difference of 10X. There is opportunity for the industry to utilize the full spectrum of capabilities and values of the ever-scaling 3D NAND technology.