Emerging Technologies for Memory-Centric and Low Power Architectures,
Edith Beigne, Facebook

Edith Beigné joined Facebook Inc. in Menlo Park in November 2018 to lead the AR/VR Silicon Research team. Before that, she was with CEA-LETI, Grenoble, France, from 1998 to 2018 where she was the Research Director of Integrated Circuits and System Division. Since 2009, she has been a senior scientist in the digital and mixed-signal design lab where she focused on low power and adaptive circuit techniques, exploiting asynchronous design and advanced technology nodes like FDSOI 28nm and 14nm for many different applications from high performance MPSoC to ultra-low power IoT applications. Her main research interests today are low power digital and mixed-signal circuits and design with emerging technologies. She is part of ISSCC TPC since 2014 and part of VLSI Symposium TPC since 2015. Distinguished Lecturer for the SSCS in 2016/2017, Women-in-Circuits Committee chair and JSSC Associate Editor since 2018. She visited Stanford University in 2018.

Abstract: Many of today's edge computing applications are suffering from high energy and lack of on-chip memory capacity. Memories are the most power-hungry components in many of these applications. Significant improvement can be traded off by using new emerging technologies like 3D integration and Non-volatile memories. This course will first discuss power and integration challenges for edge computing applications and give an overview of alternate technologies to be used in conjunction with CMOS technologies. State-of-the-art solutions for design and architecture leveraging non-volatile memories and 3D integration will be presented. We will conclude on Augmented Reality applications challenges.