Memory Devices and Selectors for High-Density Memory Technologies,
Alessandro Calderoni, Micron Technology

Alessandro Calderoni received the Laurea degree in Electrical Engineering (cum laude) from Politecnico di Milano, Italy, in 2006. He joined the Research and Development department of STMicroelectronics (then Numonyx) in 2006 and the Emerging Memory department of Micron Technology in 2010. He has been working on Emerging Memory for more than 10 years in different roles and with different responsibilities. His research interests include: CMOS modeling; NAND characterization and modeling; Phase Change Memory (PCM) array characterization and reliability, transport mechanisms and low-frequency noise characterization and modeling; Read margin improvement tool development; different RRAM and CBRAM systems with particular focus on reliability aspects; Cross-point architectures evaluation and selector device characterization; path-finding evaluation of DRAM-like architectures. He is currently a Senior Manager of Device Technology in the Emerging Memory Research and Development Team at Micron Technology.

Abstract: Over the last decade, the Memory Sub-System has become a fundamental bottle-neck for all Computing Systems from mobile devices to servers. The exponential increase of generated data and the growing demand for faster processing and analytics on big data has sparked the interest for in-memory computing. In-memory computing demands a significant increase of main memory (DRAM) density as well as high performance memories. DRAM scaling requires an aggressive and cost-effective lithography roadmap and it faces several materials and process integration challenges. New Emerging Memories may enable scaling beyond the limits of existing technologies as well as offer alternative ways to design a system architecture that enables a memory-centric computing (as opposed to a long history of processor-centric computing). In this course, we will be discussing scaling challenges of traditional memories (DRAM and NAND) as well as focus on Emerging Memory requirements for high-density applications.