Design Technology Co-Optimization for 3nm and Beyond, *Lars Liebmann, TEL*

Lars Liebemann spend over 25 years enabling semiconductor scaling first at an IDM and then a foundry, Lars Liebmann recently joined Tokyo Electron at their TEL Technology Center America, Albany, NY. Having received BS and MS degrees in Nuclear Engineering and a PhD in Engineering Physics from Rensselaer Polytechnic Institute, Troy, NY, Dr. Liebmann started working on semiconductor scaling in 1991 when critical dimensions were approaching a quarter micron. As his work on resolution enhancement techniques became increasingly complex and layout invasive, he found himself interacting with the design community earlier and more fundamentally in every technology node. These engagements on restrictive design rules, lithography friendly design, and multiple exposure enhanced design flows laid the foundation for what is now known as design-technology co-optimization (DTCO). After spending a decade advancing DTCO as a means of developing robust technology definitions in the early stages of leading-edge technology nodes. Dr. Liebmann joined TEL where he is focusing primarily on 3D integration as a means of maintaining semiconductor scaling. He holds over 95 patents, has published over 70 technical papers, is a fellow of SPIE, and summarized his early tenure work in a book: 'Design Technology Co-Optimization in the Era of Sub-resolution IC Scaling'.

Abstract: The semiconductor industry is on the verge of hitting what appears to be the most decisive scaling barrier yet. While the end of VLSI logic scaling has been prophesized and proven wrong many times in the last five decades, the imminent end to any possibility of further reduction in critical dimensions is cause for concern. As with the many scaling barriers that have come before, we will engineer our way through this to prosper for many more technology nodes. Though unlike the barriers of the past, this one will require unprecedented interdisciplinary collaboration to maintain meaningful value-add at a time when the three main pillars that have supported this industry: Moore, Dennard, and von Neumann are all crumbling. 3D integration for logic scaling, unlike memory, is not merely an exercise in integrating transistor density in volume rather than area; it is an exercise in deriving value from highly-complex system-level benefits. Just as pitch-based scaling with a focus on resolution enhancement techniques (RET) gave way to design-technology co-optimization (DTCO) with a focus on scaling boosters such as self-aligned gate contacts (SAGC) and buried power-rails (BPR), we are now transitioning to the era of system-technology co-optimization (STCO) to exploit value from solutions such as complementary FET (CFET) and 3D integrated logic. When once it was seen as revolutionary those etch engineers and lithography engineers collaborated, we are now challenged to synergistically innovate across the entire spectrum of the design-to-silicon infrastructure. After briefly reviewing the contributions DTCO has made to semiconductor scaling thus far, this short course will show examples of how engineers with skillsets in diametrically opposed specialties within our broad technical endeavor have to join forces to seek out opportunities for incremental value gain. Through examples focused on different potential 3nm node scenarios, attendees will be introduced to DTCO's latest 'tools of the trade', including process emulation and technology prototyping to quantify achievable power-performance-area-cost (PPAC) gains.