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Abstract: Interconnects are no longer simply the wiring for devices, rather becoming enablers of new concepts and architectures for advanced nodes. In this short course a toolbox of options will be reviewed to keep pace and drive PPA scaling for 3nm technology and beyond. Scaling boosters to help with pattering, yield and area scaling will be reviewed. These include: Fully-Self-Aligned-Via (FSAV) and Self-Aligned-Block (SAB) techniques to reduce variability and enhance edge placement error (EPE) tolerance; multi-level high aspect ratio Super-Vias (SV) mitigate minimum area and via extension restrictions; and Buried Power Rails (BPR) to enable track height scaling. The extendibility of traditional Cu-Low-k and entry points for the integration of alternative metals will be discussed. Finally, disruptive metal etching integration schemes to maintain aggressive RC scaling will be motivated.