

Session 18: Circuit and Device Interaction - Embedded Memory at Advanced CMOS Nodes

Tuesday, December 4, 2:15 PM

Grand Ballroom A

Co- Chairs: R. Waser, RWTH Aachen

A. Mocuta, imec

2:20 PM - 2:45 PM

18.1 MRAM as Embedded Non-Volatile Memory Solution for 22FFL FinFET Technology, O. Golonzka, J.-G. Alzate, U. Arslan, M. Bohr, P. Bai, J. Brockman, B. Buford, C. Connor, N. Das, B. Doyle, T. Ghani, F. Hamzaoglu, P. Heil, P. Hentges, R. Jahan, D. Kencke, B. Lin, M. Lu, M. Mainuddin, M. Meterelliyoz, P. Nguyen, D. Nikonov, K. O'Brien, J. O'Donnell, K. Oguz, D. Ouellette, J. Park, J. Pellegrin, C. Puls, P. Quintero, T. Rahman, A. Romang, M. Sekhar, A. Selarka, M. Seth, A. J. Smith, A. K. Smith, L. Wei, C. Wiegand, Z. Zhang and K. Fischer, Intel Corporation

This paper presents key features of MRAM-based non-volatile memory embedded into Intel 22FFL technology. 22FFL is a high performance, ultra low power FinFET technology for mobile and RF applications with extensive high voltage and analog support, and a high level of design flexibility at low cost. Embedded NVM technology presented here achieves 200°C 10-year retention capability combined with >1E6 cycle endurance and high die yield. Technology data retention, endurance and yield capabilities are demonstrated on 7.2Mbit arrays. We describe device-level MTJ characteristics, key integration features, cell characteristics, array operation specifics, as well as key yield milestones.

2:45 PM - 3:10 PM

18.2 Demonstration of Highly Manufacturable STT-MRAM Embedded in 28nm Logic, Y. J. Song, J. H. Lee, S. H. Han, H. C. Shin, K. H. Lee, K. Suh, D. E. Jeong, G. H. Koh, S. C. Oh, J. H. Park, S. O. Park, B. J. Bae, O. I. Kwon, K. H. Hwang, B.Y. Seo, Y.K. Lee, S. H. Hwang, D. S. Lee, Y. Ji, K.C. Park, G. T. Jeong, H. S. Hong, K. P. Lee, H. K. Kang, and E. S. Jung, Samsung Electronics

We successfully demonstrated the manufacturability of 8Mb STT-MRAM embedded in 28nm FDSOI logic platform by achieving stable functionality and robust package level reliability. Read margin were greatly improved by increasing TMR value and also reducing distribution of cell resistance using advanced MTJ stack and patterning technology. Write margin was also increased by improving the efficiency using novel integration process. Its product reliability was confirmed in package level with passing HTOL 1000 hours tests, 10⁶ endurance test, and retention test. For a wider application, we also demonstrated the feasibility of high density 128Mb STT-MRAM. Based on these results, we clearly verified the product manufacturability of embedded STT-MRAM.

3:10 PM - 3:35 PM

18.3 Enablement of STT-MRAM as last level cache for the high performance computing domain at the 5nm node, S. Sakhare*, M. Perumkunnil, T. Huynh Bao, S. Rao, W. Kim, D. Crotti, F. Yasin, S. Couet, J. Swerts, S. Kundu, D., Yakimets, R. Baert, HR. Oh, A. Spessot, A. Mocuta, G. Sankar Kar, A. Furnemont, imec

The increased complexity of CMOS transistor processing has led to limited scaling of high density SRAM cell at advanced technology nodes. STT-MRAM appears to be a promising candidate for replacing last level caches (LLC). This paper addresses design technology co-optimization (DTCO) of STT-MRAM technology and analyzes its viability as a LLC (compared to SRAM) for the high performance computing (HPC) domain (while maintaining a constraint of occupying merely 43.3% of SRAM macro area at identical capacities). This is the first study that breaks down a power, performance and area (PPA) comparison between SRAM and STT-MRAM based LLCs at the 5nm node. The STT-MRAM design and analysis is based on a silicon verified compact model and can be realized using 193i single patterning at the 5nm node.

Our STT-MRAM design manages to achieve a nominal access latency <2.5ns and <7.1ns for read and write operations respectively. We also observe a clear and significant trend of increasing energy gains with respect to SRAM for increasing LLC sizes with the crossover points for STT-MRAM read and write operations at 0.4MB and 5MB respectively.

3:35 PM *Coffee Break*

4:00 PM - 4:25 PM

18.4 Truly Innovative 28nm FDSOI Technology for Automotive Micro-Controller Applications embedding 16MB Phase Change Memory, *F. Arnaud, P. Zuliani, M.P. Reynard, A. Gandolfo, F. Diesgni, P. Mattavelli, E. Gomiero, G. Samanni, C. Jahan, R. Berthelon, O. Bewer, E. Richard, V. Barral, A. Villaret, S. Kohler, J.C. Grenier, R. Ranica, C. Gallon, A. Souhaite, D. Ristoiu, L. Favennec, V. Caubet, S. Delmedico, N. Cherault, R. Beneyton, S. Chouteau, P.O. Sassoulas, A. Vernhet, Y. Le Fric, F. Domengie, L. Scotti, D. Pacelli, J. L. Ogier, F. Boucard, S. Lagrasta, D. Benoit, L. Clement, P. Boivin, P. Ferreira, R. Annunziata, P. Cappelletti, STMicroelectronics*

For the first time we propose a 28nm FDSOI e-NVM solution for automotive micro-controller applications using a Phase Change Memory (PCM) based on chalcogenide ternary material. A complete array organization is described exploiting body biasing capability of Fully Depleted Silicon On Insulator (FDSOI) transistors. Leveraging triple gate oxide integration with high-k metal gate (HKMG) stack, a true 5V transistor with high analog performance has been demonstrated. Reliable PCM 0,036um² analytical cell with 2 decades programming window after 1 Million of cycles has been demonstrated. Finally, current distributions based on a fully integrated 16MB macro-cell is presented achieving Bit Error Rate (BER) < 10⁻⁸ after multiple bakes at 150°C and 10k cycling of code storage memory.

4:25 PM - 4:50 PM

18.5 A cost-efficient 28nm split-gate eFLASH memory featuring a HKMG hybrid bit cell and HV device, *R. Richter, M. Trentzsch, S. Dünkel, J. Müller, P. Moll, B. Bayha, K. Mothes, A. Henke, M. Mazur, J. Paul, P. Krottenthaler, J. Poth, S. Jansen, R. Hüseltz, H. Kim, A. Zaka, T. Herrmann, E.M. Bazizi, S. Beyer, P. Ghazavi*, H. Om'mani*, S. Lemke*, Y. Tkachev*, F. Zhou*, J. Kim*, X. Liu*, V. Tiwari*, and N. Do*, GLOBALFOUNDRIES, *Silicon Storage Technology, Inc.*

We demonstrate for the first time the integration of the proven SuperFlash® bit cell into 28 nm High-K Metal Gate (HKMG) technology, incorporating logic HKMG into the flash cell. Flash cell and high-voltage (HV) devices are implemented into a cost-optimized process flow saving seven masks compared to other 28nm eFLASH technologies. Comparable program/erase (P/E) endurance of up to one million cycles at 125°C is shown and program disturb characteristics meets array operation requirements. The Wordline transistor exhibits no degradation in sub-threshold slope of the post 100k P/E cycling, demonstrating robust reliability despite the introduction of HKMG into the flash cell. Additionally, the HKMG based HV devices demonstrate performance similar to platforms without HKMG material.

4:50 PM - 5:15 PM

18.6 A Bi-stable 1- /2-Transistor SRAM in 14 nm FinFET Technology for High Density / High Performance Embedded Applications, *Y. Widjaja, J. Wilson, T. Nguyen, J-W Han, C. Norwood, D. Maheshwari, S. Lai, P. Vorenkamp, Z. Or-Bach, Y. Nishi*, Zeno Semiconductor Inc., *Stanford University*

1-transistor and 2-transistor (1T/2T) SRAM are fabricated using 14 nm baseline foundry process without any process modifications. A bi-stable self-latch mechanism is established in a single transistor where its p-type body becomes electrically floating by reverse biased, buried depletion regions from adjacent n-wells. The bit cell operation and the disturb immunity are verified. A unit cell size of 0.039 μm² is achieved, offering >2x area reduction over 6T-SRAM and providing comparable power and performance.

