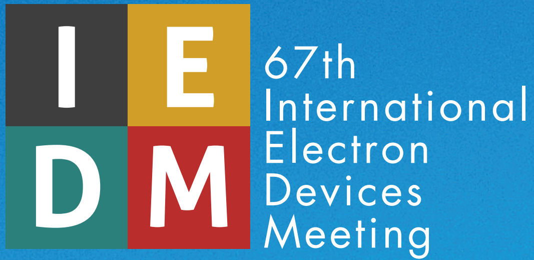

2021 IEDM Conference Proceedings

Innovative Devices for a Better Future

For More Information
IEDM Online: ieee-iedm.org

Social Networks:
ieee-iedm.org/social-media

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Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

Digital & Social Media

- LinkedIn: https://www.linkedin.com/groups/7475096/
- Twitter: https://twitter.com/ieee_iedm
- Facebook: https://www.facebook.com/IEEE.IEDM
- YouTube: https://www.youtube.com/channel/UC9X-8YPHtsy3SMQwU0yZdTg
- Wikipedia: https://en.wikipedia.org/wiki/International_Electron_Devices_Meeting

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Topics of Interest

ADVANCED LOGIC TECHNOLOGY (ALT)

Papers are solicited in the areas of CMOS platform technologies and applications (e.g., HPC, LOP, mobile, automotive, low-temperature CMOS, etc.), logic devices and circuits, process integration schemes for advanced nodes, innovations in material, process and metrology techniques, and design technology co-optimization (DTCO) and system technology co-optimization (STCO). Platform technologies include state-of-the-art Si and beyond-Si channel devices, gate-all-around devices, stacked devices with different polarity transistors, advanced interconnect, novel power distribution integration schemes, heterogenous 2.5D/3D integration schemes, and BEOL compatible transistors. Device architecture, device design and analysis, process integration, module advancements in process and patterning, metrology, physical layout effects, techniques for reduced variability, yield, methodologies and solutions for DTCO/STCO in the solicited areas are of high interest.

EMERGING DEVICE and COMPUTE TECHNOLOGY (EDT)

Papers are solicited on emerging nanoelectronic devices and physics. This includes devices based on novel transport and control mechanisms such as tunnel FET, negative capacitance FET, topological materials and devices, phase transitions, ferroelectrics and quantum effects. Devices based on low-dimensional systems including 2D materials, CNTs, nanowires, and quantum dots are welcomed. Devices with novel device functions and/or novel materials for neuromorphic compute, approximate and analog compute, and non-charge-based logic such as spintronics are key topics. Furthermore, emerging state machines and time dynamical compute systems are also of interest. Qubit devices as well as devices and systems designed to enable quantum computing, quantum simulation and quantum annealing are of high interest. Papers in EDT focus primarily on device physics, innovative transistor structures, and novel concepts; more mature “platform candidate” papers, such as based on established two-terminal resistive memories, should be submitted to ALT and MT. Reliability assessment of emerging devices are also solicited here, while assessments for more mature devices should be submitted to RSD.

MEMORY TECHNOLOGY (MT)

Papers are solicited in the areas related to embedded and standalone memory technology. This includes advances in both conventional memories including SRAM, DRAM and Flash, and emerging memories including ReRAM, MRAM, PCRAM, ferroelectric memory, crosspoint memory and selectors, organic memory and NEMS-based memory, as well as their applications in the areas of compute-in-memory, and machine learning. Topics span from demonstration of novel device concepts to fully integrated memory arrays, and from product prototyping to manufacturing related challenges and solutions. Demonstrations of manufacturing maturity of emerging memories are of high interest. Submission of papers on novel device concepts and demonstrations, novel integration schemes, novel circuit design schemes, and novel memory architectures that enhance memory performance or improve system level performance in compute-in-memory and AI applications is strongly encouraged.

MICROWAVE, MILLIMETER WAVE and ANALOG TECHNOLOGY (MAT)

Papers are solicited in the areas of high frequency device technology, device physics as well as high frequency circuit applications in the micro, mm-wave and THz frequency spectrum. Device physics and technology include based on Si, SiGe, wide bandgap compound semiconductors like III-Vs, III-nitrides, gallium oxide and silicon carbide. Circuit aspects covers analog front ends, filters, beam formers, switches, LNAs, PAs, tunable passives, antenna arrays, SAW/BAW and RF devices for mixed signal, energy harvesting circuit and IoTs, circuit and device interaction for higher system integrity, readout IC targeting quantum computing in the micro and mm-wave domain.

MODELING and SIMULATION (MS)

Papers are solicited on theoretical approaches to electronic devices, including logic devices, memory devices, optical devices, interconnects and (bio)sensors. Theoretical approaches include analytical, numerical and statistical approaches applied to structures with dimensions ranging from atomistic over device dimensions to full-chip dimensions, including physics-based compact modeling. Key to submissions is, that the device innovation is central, either through predictive insight in the potential of novel device concepts, predictive analysis revealing significant improvement to devices, breakthroughs in the theoretical understanding of the device operation, breakthroughs in the understanding of device processing enabling improved device performance, novel insights in variability, reliability and yield issues, breakthrough in device optimization based on DTCO. Topics also include neuromorphic computing, quantum computing, spintronics, low-dimensional devices, ferroelectrics, thermal modeling, 3D/heterogeneous integration, electro-chemical/mechanical devices. Comparison with experimental data, model calibration and multi-scale simulation chains are highly encouraged.

OPTOELECTRONICS, DISPLAYS, and IMAGING SYSTEMS (ODI)

Papers are solicited on optoelectronics, displays, and imaging systems. This includes novel devices, structures, and integration for image sensors, displays, light sources, photonic devices, and high-speed photodetectors and modulators. New technologies on heterogeneous integration of optoelectronics as well as on photonic-electronic integration for optical interconnects, on-chip networks and sensing are welcomed. Papers on quantum photonics and plasmonics for neuromorphic and quantum computation, sensing and encryption are also of interest. Furthermore, ODI includes CMOS imagers, high-speed and high-time resolution imagers, CCDs, stacked image sensors, and displays of all types. In addition, papers on displays for augmented or virtual reality, holography, TFTs for photonics applications, flexible, stretchable, and/or printed electronics, in-display sensors are encouraged. Papers on displays or light emitting devices with novel materials such as perovskites or quantum dots are also of interest. We particularly welcome submissions concerning optoelectronic or photonic devices or systems based on topological concepts.

POWER DEVICES and SYSTEMS (PDS)

Papers are solicited on discrete and integrated power devices, modules and systems using Si, compound semiconductors, and diamond. Papers exploring the system-level impact of power devices are also of interest. Topics of interest include power devices (diodes, BJTs, FETs, super-junction devices, heterostructures, IGBTs, HEMTs, light-triggered structures, bi-directional switches etc.), and materials (Si, SiC, GaAs, GaN, AlN, Ga2O3, etc.), power systems on a chip, high performance passives (magnetics), novel circuit topologies enabled by wide band-gap semiconductors, manufacturing processes, device design, modeling (TCAD and compact models), devices physics, and reliability. Devices targeting the full range of power and power conversion applications, including automotive, power supplies for computers and data centers, integrated voltage regulators, power conditioners for photovoltaic solar, wind applications, motor drives, electric aviation, and smart grid (solid-state transformers, MVDC distribution, HVDC transmission), and wireless power transfer, are of interest besides fundamental studies on doping, deep-level traps, interface state densities and device reliability for power switching devices.

RELIABILITY OF SYSTEMS and DEVICES (RSD)

Papers are solicited in all areas of electrical and physical characterization, reliability evaluation and yield analysis of transistors, interconnects, circuits and systems mainly (but not limited) to Si-based technologies. Specific reliability topics include, for FEOL: transistor degradation due to hot carriers and bias temperature instabilities; dielectric wear-out and breakdown; self-heating effects; process charging damage; latch-up and ESD; soft error mechanisms in logic and memories. For MEOL/BEOL topics include: electromigration failure of contacts and interconnects; breakdown of BEOL dielectrics and MEOL spacers; thermal management; For system and circuit reliability topics include design for reliability and variability-aware design, robustness and security of electronic circuits and systems. Of particular interest are investigations of degradation mechanisms for devices, circuits and systems in the following area: conventional and emerging memories; more-than-Moore applications; biomedical devices and systems; automotive and aerospace.

SENSORS, MEMS, and BIOELECTRONICS (SMB)

Papers are solicited in the areas of sensors, micro/nano electromechanical systems (MEMS and NEMS), microfluidics/lab-on-chip, and BioMEMS, with particular emphasis on new device concepts, integrated implementations, CMOS-on-MEMS, embedded intelligence, organic-inorganic hybrid microfabrication, flexible devices, and multi-sensors on a chip for applications in health, medicine, communication, mobility, and energy. Sensors include chemical, molecular and biological detection based on acoustic, electrical, electrochemical, magnetic, mechanical and optical principles. Topics of interest in the MEMS area include actuators, physical sensors, resonators, integrated inertial measurement units, TFTs, RF MEMS, micro-optical and optomechanical devices, micro-power generators, and devices for energy harvesting as well as on-chip energy storage. BioMEMS area covers organic-inorganic hybrid devices, point-of-care biomedical devices, bio-electronic interface, integrated biomedical sensing and implantable neural interfaces.

Program

See the Appendix for all abstracts and speaker bios.

Tutorials

The tutorials are in their twelfth year and are stand alone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields, and facilitate understanding of the technical sessions. In contrast, the traditional short courses are focused on a single technical topic.

All Tutorials will be held on Saturday, December 11th, 2021.

Saturday, December 11, 2:45 p.m. - 4:15 p.m.

- Beyond FINFET era: Challenges and opportunities for CMOS technology, Kai Zhao, IBM
- TCAD based DTCO and STCO, Asen Asenov, University of Glasgow
- 6G Technology Challenges from devices to wireless systems, Aarno Pärssinen, Oulu University

Saturday, December 11, 4:30 p.m. - 6:00 p.m.

- Selective and Atomic Scale Processes for Advanced Semiconductor Manufacturing, Robert Clark, TEL
- Machine Learning for Semiconductor Device and Circuit Modeling, Elyse Rosenbaum, Univ. of Illinois at Urbana-Champaign
- GaN Power Device Technology and Reliability, Dong Seup Lee, Texas Instruments

Short Courses

Sunday, December 12, 2021, 9:00 a.m. – 5:30 p.m.

IEEE IEDM will offer two short courses with in-depth coverage of highly relevant topics from world experts.

Advance registration is recommended. All short courses will be held on Sunday, December 12th.

Short Course 1: Future scaling and integration technology

Course Organizer: Dechao Guo, IBM Research

- Processes and Materials Engineering Innovations for Advanced Logic Transistor Scaling, Benjamin Colombeau, Applied Materials
- Interconnect Resistivity: New Materials, Daniel Gall, Rensselaer Polytechnic Institute
- Metrology and Material Characterization for the Era of 3D Logic and Memory, Roy Koret, Nova Ltd.
- Beyond FinFET Devices: GAA, CFET, 2D Material FET, Chung-Hsun Lin, Intel
- Heterogenous Integration Using Chiplets & Advanced Packaging, Madhavan Swaminathan, Georgia Tech
- Design-Technology Co-Optimization / System-Technology Co-Optimization, Victor Moroz, Synopsys

Short Course 2: Emerging Technologies for Low Power Edge Computing

Course Organizers: Huaqiang Wu, Tsinghua University and John Paul Strachan, Forschungszentrum Jülich

- Mobile NPUs for Intelligent Human Computer Interaction, Hoi-Jun Yoo, KAIST
- Brain-inspired strategies for optimizing the design of neuromorphic sensory-processing systems, Giacomo Indiveri, University of Zurich
- Memory based AI & Data Analytics solutions, Euicheol Lim, SK hynix
- Material strategies for memristor-based AI hardware and their heterointegration, Jeehwan Kim, MIT
- RRAM devices for data storage and in-memory computing, Wei Lu, University of Michigan
- Practical implementation of wireless power transfer, Hubregt Visser, IMEC

Plenary Session

December 13, 2021

Welcome and Awards

General Chair: Tibor Grasser, TU Wien

Plenary Papers

Technical Program Chair: Barbara De Salva, Facebook

1.1 "The Smallest Engine Transforming Humanity: The Past, Present, and Future"

Kinam Kim, Chairman, Samsung Electronics, Samsung

1.2 "Creating the Future: Augmented Reality, the Next Human-Machine Interface"

Michael Abrash, Chief Scientist at Facebook Reality Labs, Facebook

1.3 "Quantum Computing Technology"

Heike Riel, IBM Fellow and the Head of the Science & Technology Department at IBM Research, IBM Zurich

Focus Sessions

As every year, IEEE IEDM 2021 will offer Special Focus Sessions on emerging topics with invited talks from world experts to highlight the latest developments.

Monday, December 13, 1:35 PM

- Session 3 – Advanced Logic Technology – Focus Session - Stacking of devices, circuits, chips: design, fabrication, metrology - challenges and opportunities

Tuesday, December 14, 9:05 AM

- Session 14 - Emerging Device and Compute Technology - Focus Session - Device Technology for Quantum Computing

Wednesday, December 15, 9:05 AM

- Session 25 - Memory Technology/Advanced Logic Technology - Focus Session - STCO for memory-centric computing and 3D integration

Wednesday, December 15, 1:35 PM

- Session 35 - Sensors, MEMS, and Bioelectronics/Optoelectronics, Displays, and Imaging Systems - Focus Session - Technologies for VR and Intelligence Sensors
- Session 38 - Emerging Device and Compute Technology/Optoelectronics, Displays, and Imaging Systems - Focus Session - Topological Materials, Devices, and Systems

Career Session

Tuesday, December 14, 12:20pm to 2:00 pm

Speakers: Sophie Vandebroek, Strategic Vision Ventures LLC

Deji Akinwande, University of Texas

Technical Program

See the Appendix for all abstracts and speaker bios.

IEDM committee announces that IEDM will be an in-person conference December 11-15 at the Hilton San Francisco Union Square. Starting December 17, the full conference will be on-demand

Monday, December 13, 1:35 PM

- Session 2 - Memory Technology - STT-MRAM technology and exploratory devices
- Session 3 - Advanced Logic Technology - Focus Session - Stacking of devices, circuits, chips: design, fabrication, metrology - challenges and opportunities

- Session 4 - Microwave, Millimeter Wave and Analog - Innovative RF technologies for low power and RF/mmW applications
- Session 5 - Power Devices and Systems - GaN power devices, technologies, and circuits
- Session 6 - Reliability of Systems and Devices - Reliability studies on advanced memories: Ferroelectric, ReRAM, DRAM
- Session 7 - Emerging Device and Compute Technology - 2D Channel Transistors Session 8 - Modeling and Simulation - Memory Technology
- Session 9 - Optoelectronics, Displays, and Imaging Systems - Emerging Detectors and Displays Technologies

Tuesday, December 14, 9:05 AM

- Session 10 - Memory Technology - Charge-based Memories
- Session 11 - Microwave, Millimeter Wave and Analog - III-V technologies and their Applications to THz/6G
- Session 12 - Memory Technology - NOR Flash and RRAM for In-Memory Computing Session 13 - Advanced Logic Technology - Platform Technologies and Advanced Gate Stack
- Session 14 - Emerging Device and Compute Technology - Focus Session - Device Technology for Quantum Computing
- Session 15 - Modeling and Simulation – Ferroelectric Materials, Devices and Applications Session 16 - Sensors, MEMS, and Bioelectronics - Biomedical Devices

Tuesday, December 14, 2:20 PM

- Session 17 - Memory Technology - Emerging Non-Volatile Memories
- Session 18 - Modeling and Simulation - Advanced simulation and modeling of FETs
- Session 19 - Emerging Device and Compute Technology - Ferroelectric based FET: From Fundamentals to Applications
- Session 20 - Optoelectronics, Displays, and Imaging Systems - SPADs and LiDAR
- Session 21 - Emerging Device and Compute Technology - Compute-in-memory (CiM) with emerging devices and integration technology
- Session 22 - Advanced Logic Technology - Front- and back-side advanced interconnects Session 23 - Sensors, MEMS, and Bioelectronics - Novel Sensor Technologies
- Session 24: Panel Discussion, 8:00 PM – 10:00 PM - Is HW/SW co-design a necessary evil or a symbiotic partner? Moderator: Myung-hee Na, SK Hynix

Wednesday, December 15, 9:05 AM

- Session 25 - Memory Technology/Advanced Logic Technology - Focus Session - STCO for memory- centric computing and 3D integration
- Session 26 - Advanced Logic Technology - Advances in Nanosheet FET devices Session 27 - Modeling and Simulation - Low-dimensional and spin-based devices Session 28 - Memory Technology - Emerging memory (PCRAM/OTS)
- Session 29 - Optoelectronics, Displays, and Imaging Systems - Integrated Photonics Session 30 - Optoelectronics, Displays, and Imaging Systems - Image Sensors Session 31 - Reliability of Systems and Devices - Advanced Logic Device Reliability
- Session 32 - Emerging Device and Compute Technology - CMOS+X Devices: New Materials and Spintronics

Wednesday, December 15, 1:35 PM

- Session 33 - Memory Technology - Ferroelectric Memory
- Session 34 - Advanced Logic Technology - Future Technologies: 3D Integration and 2D Channel Materials
- Session 35 - Sensors, MEMS, and Bioelectronics/Optoelectronics, Displays, and Imaging Systems - Focus Session - Technologies for VR and Intelligence Sensors
- Session 36 - Power Devices and Systems - Recent Advancements in Power Semiconductor Devices Session 37 - Emerging Device and Compute Technology - Two-Dimensional and Oxide Semiconductors: Optimization and

Applications

- Session 38 - Emerging Device and Compute Technology/Optoelectronics, Displays, and Imaging Systems - Focus Session - Topological Materials, Devices, and Systems
- Session 39 - Reliability of Systems and Devices - Reliability in RF/Power/Security Applications Session 40 - Emerging Device and Compute Technology - Cryogenic, Exploratory and Quantum Computing Devices

Panel Discussion

Tuesday, December 14, 8:00 pm - 10:00 pm

Is HW/SW co-design a necessary evil or a symbiotic partner?

Moderator: Myung-hee Na, SK Hynix

We all know that technology itself is not sufficient to meet all demands of emerging workloads in data-centric era. Everyone says that HW/SW co-design and optimization is becoming more critical for most applications. Yet, it is not quite clear what HW/SW co-design really means in technology research and development.

We would like to open discussion to help IEDM communities bring software close to technology HW for impactful innovation.

Panelists:

- Sriram Balasubramanian, Samsung
- Kirk Bresniker, HPE
- Kailash Gopalakrishnan, IBM
- Hsien-Hsin Sean Lee, Facebook
- Poonacha Kongetira, SambaNova Systems
- Subhasish Mitra, Stanford
- Kathleen Philips, imec
- Elisa Vianello, CEA-LETI

Magnetics Society events at IEDM 2021

Technically sponsored by the IEEE Magnetics Society

Two IEEE Magnetics Society events at IEDM 2021

With the rising interest of the microelectronics industry in STT-MRAM, it is very important to strengthen the relationship between the microelectronics and magnetism communities since this technology requires expertise from both areas. For that, two special events related to MRAM technology are being organized around IEDM by the IEEE Magnetics Society. These events are co-chaired by B. Dieny, K. Garello, L. Thomas, with the additional help of the program committee formed of D. Worledge, K.J. Lee, S. Fukami, J. Katine, J. Guedj and of P. Mahoney and J.A. Incorvia for the logistics.

1) A special poster session dedicated to MRAM - Hilton Union Square, 15 Dec 2021, Yosemite Room, 9:00 am - 12:00 pm

Various topics will be covered including MRAM materials, phenomena, technology, testing, hybrid CMOS/MTJ technology and circuits, spin-logic. Similar MRAM poster sessions that took place since IEDM 2016 were very successful, with more than 30 posters presented yearly and very active cross-disciplinary discussions. This session is technically organized by the IEEE Magnetics Society. It will appear as a special MRAM poster session embedded in the IEDM conference. This event will be a great opportunity to bring together experts in magnetism and in microelectronics.

We strongly encourage teams involved in MRAM R&D to present posters related to MRAM, spintronic circuits or spin logic during this special poster session. The posters will be selected by an international program committee formed by members of the IEEE Magnetics Society. There will be no publications associated with these posters in the Proceedings of IEDM.

To present a poster during the MRAM poster session at IEDM 2021, send a half page abstract to kevin.garello@cea.fr before 29 October 2021. In the list of authors, underline who will be the presenting author. Only abstracts of posters which will be presented in-person during IEDM can be submitted. The notification of acceptance/rejection will be sent by mid-November. Participants to this poster session will have to register for IEDM as regular attendees.

More information will be posted on the IEEE Magnetics Society website: https://www.ieeemagnetics.org/

2) The 13th MRAM Global Innovation Forum - Hilton Union Square, 16 Dec 2021, 8:45am – 6:00pm

The MRAM Forum series was initiated by Samsung Semiconductor, and this forum marks the 13th edition. This is a one-day event organized the day following IEDM (i.e on 16 December 2021, 8:45am – 6:00pm) in the same hotel as IEDM (Hilton Union Square, 333 O'Farrell St, San Francisco). The Forum will consist of 11 invited talks from leading experts and a panel discussion. Various MRAM related topics will be covered including STT-MRAM technology, memory and processor demonstrations, spin orbit torque MRAM, and the needs, challenges and potential of MRAM.

As for IEDM, the 13th MRAM Global Innovation Forum will be an in-person event. However, all talks as well as the panel discussion will be recorded and made available on-demand to registered attendees starting 18 December for a period of two months after the Forum. There will be no-fees associated to the Forum registration but registration is mandatory.

To register to the Forum, send an email to incorvia@austin.utexas.edu with first name, last name, contact email, affiliation. Indicate whether you intend to attend in-person or only wish on-line access to the Forum presentations after the Forum. A confirmation email will be sent to you. The deadline for registering to the Forum is 20th, November 2021. Note that the number of in-person attendees to the Forum will be limited.

Details on these events will be updated on the IEDM (https://www.ieee-iedm.org/) and IEEE Magnetics Society (https://www.ieeemagnetics.org/) websites.

Bernard DIENY, Luc THOMAS and Kevin GARELLO

Exhibits & Exhibit Events

After the successful Exhibits Events in the last years, IEEE IEDM 2022 will again be open to exhibitors. Take this unique opportunity to exhibit at the IEEE's flagship conference on electron devices.

Booth pricing (includes one regular access to the technical program):

- 10x10 booth: $2,500
- 10x20 booth: $4,500
- Academic booth: $1,000* limited quantity available.

Featured Products

- Advanced memory
- Novel displays
- MEMS devices
- Optoelectronics
- High-speed devices
- Nanometer-scale CMOS transistor technology
- Novel quantum and nano-scale devices and phenomenology
- Process technology and device modeling and simulation
- Devices for power and energy harvesting
- Sensors

Event Highlights

- Conference includes over 38 technical sessions with over 200 speakers
- The conference, including exhibitor participation, is promoted to more than 250 worldwide media outlets
- Limited exhibit availability
  - 22 booths available for 2022

Attendance History & Demographics

Over 600 companies represented including:

- NASA
- Qualcomm
- Samsung
- Sony
- TEL
- TSMC
- AMD
- Apple
- Applied Materials
- Hitachi
- Intel
- Micron

Attendance History by Company Type

Company Type	2020 (Virtual)	2019	2018
Industry	1289	1193	1179
University	683	666	697
Government	58	26	42
TOTAL ATTENDEES	**2030**	**1885**	**1918**
Countries Represented	28	26	28

What is Included with Booth

10 x 10 Booth ($2,500)*

- One full conference registration and one exhibit only registration
- Company name and booth number included in pre-show planner email to all attendees
- One booth package per 10x10 booth
  - 1-6′ draped table
  - 2-side chairs
  - 1-wastebasket
  - 1-7″x44″ company identification sign

*Limited number of booths will be available at a reduced rate for academic exhibitor

*10x20 booths available for $4,500

Appendix - Abstracts, Bios & Technical Program

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Short Course 2: Emerging Technologies for Low Power Edge Computing, 9:00 a.m. – 5:30 p.m.

Monday, December 13
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Session 3 - Advanced Logic Technology - Focus Session - Stacking of devices, circuits, chips: design, fabrication, metrology - challenges and opportunities
Session 4 - Microwave, Millimeter Wave and Analog - Innovative RF technologies for low power and RF/mmW applications
Session 5 - Power Devices and Systems - GaN power devices, technologies, and circuits
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Session 8 - Modeling and Simulation - Memory Technology
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Session 12 - Memory Technology - NOR Flash and RRAM for In-Memory Computing
Session 13 - Advanced Logic Technology - Platform Technologies and Advanced Gate Stack
Session 14 - Emerging Device and Compute Technology - Focus Session - Device Technology for Quantum Computing
Session 15 - Modeling and Simulation – Ferroelectric Materials, Devices and Applications
Session 16 - Sensors, MEMS, and Bioelectronics - Biomedical Devices

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Deji Akinwande, University of Texas

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Session 19 - Emerging Device and Compute Technology - Ferroelectric based FET: From Fundamentals to Applications
Session 20 - Optoelectronics, Displays, and Imaging Systems - SPADs and LiDAR
Session 21 - Emerging Device and Compute Technology - Compute-in-memory (CiM) with emerging devices and integration technology
Session 22 - Advanced Logic Technology - Front- and back-side advanced interconnects
Session 23 - Sensors, MEMS, and Bioelectronics - Novel Sensor Technologies

Session 24: Panel Discussion, 8:00 PM – 10:00 PM
Is HW/SW co-design a necessary evil or a symbiotic partner?
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Wednesday, December 15, 9:05 AM
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Session 26 - Advanced Logic Technology - Advances in Nanosheet FET devices
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Session 28 - Memory Technology - Emerging memory (PCRAM/OTS)
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Session 30 - Optoelectronics, Displays, and Imaging Systems - Image Sensors
Session 31 - Reliability of Systems and Devices - Advanced Logic Device Reliability
Session 32 - Emerging Device and Compute Technology - CMOS+X Devices: New Materials and Spintronics

Wednesday, December 15, 1:35 PM
Session 33 - Memory Technology - Ferroelectric Memory
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Session 35 - Sensors, MEMS, and Bioelectronics/Optoelectronics, Displays, and Imaging Systems - Focus Session - Technologies for VR and Intelligence Sensors
Session 36 - Power Devices and Systems - Recent Advancements in Power Semiconductor Devices
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Session 39 - Reliability of Systems and Devices - Reliability in RF/Power/Security Applications
Session 40 - Emerging Device and Compute Technology - Cryogenic, Exploratory and Quantum Computing Devices

Tutorials 1-3

Saturday, December 11, 2:45 PM – 4:15 PM

Tutorial 1: Continental Ballroom 4/Tutorial 2: Continental Ballroom 5/Tutorial 3: Continental Ballroom 6

Tutorial 1: Beyond FINFET era: Challenges and opportunities for CMOS technology, Kai Zhao, IBM

Invention of FINFET and its introduction to mass production are among the most important breakthroughs in the recent CMOS technology history. With the excellent SCE control capability and process extendibility, FINFET architecture has enabled the industry to push technology scaling advancement in the past decade. Now the industry is at another important juncture where to further the scaling trend, transitioning from FINFET to Nanosheet becomes clear and imminent. In this tutorial, we will walk through some of the recent advancement in nanosheet technology and why it is the best candidate beyond FINFET, we will also review the latest research directions for device architectural options beyond Nanosheet and the corresponding challenges and opportunities. In addition to the FEOL device options, a brief review of the recent DTCO and BEOL advancement will also be included in this tutorial.

Tutorial 2: TCAD based DTCO and STCO, Asen Asenov, Glasgow University

Design-Technology Co-Optimization (DTCO) and System-Technology Co-Optimization (STCO) has become mandatory in advanced technology nodes. It is well understood that tailoring the transistor characteristics by tuning the technology is not sufficient anymore. The interconnects also play important role in this process responsible for approximately half of the circuit performance. The transistor and interconnect characteristics haveto meet the requirement for design and optimization of particular circuits, systems and corresponding products. Modeling and simulation play an increasing important role in the DTCO and STCO process with the benefits of speeding up and reducing the cost of the technology, circuit and system development and hence reducing the time-to-market. The DTCO and STCO also play critical role when making decisions about the next technology generations including the point of transition from FinFET to nanowire and nano-sheet architectures

In this tutorial we will introduce the key concepts of DTCO and STCO and the corresponding DTCO/STCO tools and flows originally developed by Gold Standard Simulations (GSS) and now marketed by Synopsys after the acquisition of GSS in 2016. The concepts will be illustrated with examples including both FinFET and PDSOI technologies. We will also describe how the DTCO and STCO can be used to make critical decisions regarding future technology generations.

Tutorial 3: 6G Technology Challenges from devices to wireless systems, Aarno Pärssinen, Oulu University

Evolution of wireless communications systems has provided ever increasing data rates for wireless communications systems over the years, and Edholm's law predicts data rates exceeding 1Tbps in ten year time. Such a target is also one of the key drivers on the way towards 6G communications and sensing. However, scaling up the performance of future systems to the requested bandwidths is not straightforward and many aspects related to technologies indicate challenges that must be taken seriously. Those include availability and properties of carrier frequencies to achieve the capacity, radio propagation and hardware technologies from antennas to transistors that are needed for such systems. Speed of transistors, interconnects, etc. will limit the capabilities on one side. On the other hand, scaling of antennas towards higher carrier frequencies and their impact to RF transceivers have different constraints on the potential solutions. Future wireless systems should take these aspects carefully into account, and on the other hand, technologies that would pave the way towards improved communications and sensing capabilities with reasonable power consumption will be core elements for 6G.

This tutorial addresses many of the aspects that need to be considered when implementing radio systems for anticipated 6G requirements. Principles of wireless communications systems will be analyzed against link capacity and range and based on those challenges related to RF transceivers with circuit and device aspects will be explored. Wireless communication system are already complex and complexity will even increase once technology boundaries are approached. The tutorial will provide insights on the challenges related to technologies at different hierarchies and considerations on the tradeoffs to be tackled related to the next generation of communications.

Tutorials 4-6

Saturday, December 11, 4:30 PM – 6:00 PM

Tutorial 4: Continental Ballroom 4/Tutorial 5: Continental Ballroom 5/Tutorial 6: Continental Ballroom 6

Tutorial 4: Selective and Atomic Scale Processes for Advanced Semiconductor Manufacturing, Robert D. Clark, Tokyo Electron

Continued device density scaling according to Moore's Law has resulted in the adoption of 3D device geometries and architectures and driven critical dimensions down to atomic scales. This tutorial briefly reviews the trends in device scaling since Dennard-style linear shrinking became untenable and outlines the forces driving 3D integration going forward as well as the impact these changes are having on manufacturing process technologies. The tutorial then introduces multi-patterning and atomic scale process technologies used for 10nm and beyond semiconductor manufacturing including plasma and thermal atomic layer deposition (ALD) and atomic layer etching (ALE) technologies. Selective processing including area selective deposition (ASD) is explained as an emerging technology enabling new device nodes and integration schemes. The scope of the discussion includes examples of how these technologies enable self-aligned and sub-lithographic patterning, and device and interconnect engineering along with EUV lithography to overcome edge placement error effects and realize atomic scale process control for manufacturing. Finally, a view of how integrated circuit manufacturing will continue to evolve through 3D monolithic and heterogeneous integration is presented to frame the future opportunities and challenges for advanced process technologies.

Tutorial 5: Machine Learning for Semiconductor Device and Circuit Modeling, Elyse Rosenbaum, University of Illinois, Urbana-Champaign

Machine learning (ML) algorithms and models are used extensively for image recognition, natural language processing, and recommender systems. EDA is a less mainstream application for ML methods, although that may be changing as evidenced by Google's recent announcement that its engineers developed a chip floor planning tool that utilizes reinforcement learning and which completes the placement task more quickly than human designers [Mirhoseini, Nature, 2021]. This tutorial focuses on one aspect of EDA – modeling

Optimization is a key element of every ML algorithm. Optimization is also used extensively in hardware modeling, e.g. compact modeling. Those observations may lead one to question how ML-enabled modeling differs from the modeling techniques used by device engineers. This tutorial will attempt to define the term machine learning and explore its commonalities with and differences from conventional physics-based modeling techniques.

The tutorial will focus on ML models that are especially suitable for device and circuit modeling. It will review prior works that applied ML to parameter extraction, TCAD, device modeling or circuit modeling. It is assumed that attendees have some familiarity with semiconductor device modeling (e.g. compact

models, reliability models, noise models, etc.) and/or circuit simulation. No prior knowledge of machine learning is required.

Tutorial 6: GaN Power Device Technology and Reliability, Dong Seup Lee, Texas Instruments

Excellent material properties of Gallium Nitride (GaN) have promised superior device performance over conventional silicon technologies in power electronics applications. Combination of large critical electric field and high electron mobility makes it possible to scale down power devices, which provides numerous benefits such as smaller input/output capacitances and low on-resistance. In addition, lack of body diode in GaN devices eliminates reverse recovery delay, allowing high frequency operation and opening possibilities for new circuit topologies. Thanks to these benefits, extensive research has been conducted in both academia and industries over the last few decades. Various process technologies have been developed and numerous studies on diverse reliability issues have been conducted. Based on all these efforts, performance and reliability of GaN power devices have improved tremendously and several manufacturers have announced commercial products in recent years. Market adoption is also growing rapidly in various areas from consumer electronics to industrial applications.

This tutorial introduces a broad overview of GaN power device technology. First of all, basics of GaN, including polarization, device structure, and fabrication process will be covered. Then, various reliability issues will be reviewed, starting from intrinsic device level to real applications. Finally, the tutorial will conclude with a discussion of the recent progress and future of GaN technology.

Short Course 1: Future scaling and integration technology

Sunday, December 12, 2021, 9:00 a.m. – 5:30 p.m.

Course Organizer: John Paul Strachan, Dechao Guo, IBM Research

- Processes and Materials Engineering Innovations for Advanced Logic Transistor Scaling, Benjamin Colombeau, Applied Materials
- Interconnect Resistivity: New Materials, Daniel Gall, Rensselaer Polytechnic Institute
- Metrology and Material Characterization for the Era of 3D Logic and Memory, Roy Koret, Nova Ltd.
- Beyond FinFET Devices: GAA, CFET, 2D Material FET, Chung-Hsun Lin, Intel
- Heterogenous Integration Using Chiplets & Advanced Packaging, Madhavan Swaminathan, Georgia Tech
- Design-Technology Co-Optimization / System-Technology Co-Optimization, Victor Moroz, Synopsys

1. **Processes and Materials Engineering Innovations for Advanced Logic Transistor Scaling,** Benjamin Colombeau, Applied Materials

AI computing workloads require demanding semiconductor solutions at a time when traditional Moore's Law scaling is slowing down. The drive to continue improving semiconductor power, performance, area and cost scaling (PPAC) is enabled by new architectures, new structures for 3D devices, new materials, new ways to shrink, and advanced packaging. In this short course, we will first discuss process technology and materials engineering approaches used to extend FinFET scaling more specifically for critical FEOL modules (channel, junction, gate and contact). As gate length must continue scaling, new architecture Gate All Around Nanosheet is being pursued to alleviate FinFET electrostatics limitation. We will discuss

benefits and challenges of GAA Nanosheet architecture for forthcoming generation of advanced CMOS and highlight how novel co-optimized processes and materials innovations play a critical role to address integration and device performance challenges.

2. **Interconnect Resistivity: New Materials,** Daniel Gall, Rensselaer Polytechnic Institute

   A major challenge for the continued downscaling of integrated circuits is the resistivity increase of Cu interconnect lines with decreasing dimensions, limiting power efficiency and causing the interconnect delay to exceed the gate delay. This resistivity increase is due to electron scattering at Cu surfaces and grain boundaries and leads to, for example, a 10-fold resistance increase for 10-nm-wide Cu lines. Alternative interconnect materials have the potential to outperform Cu. These include metals with a small electron mean free path to render electron scattering at surfaces and grain boundaries negligible, 2D materials as new liner/barrier layers which maximize the conductor cross-sectional area and facilitate specular surface scattering, and topological metals with protected surface states that suppress electron scattering. This talk presents recent research results focusing on these new materials for high-conductivity narrow interconnects.

3. **Metrology and Material Characterization for the Era of 3D Logic and Memory,** Roy Koret, Nova Ltd.

   As technology keeps scaling, devices migrate from 2D into 3D integration. Within this new era, we observe how 3D aspects of geometry and material characterization become even more prominent. Thus, IC manufactures need to evaluate the current metrology capabilities, and examine new metrology and characterization techniques they need to add to their toolbox. The course intension is to provide the audience with the understanding of the existing metrology platforms, that have matured during the 2D integration era, how they were taken to their extreme performance, and which new methods (alternative) need to be combined into the production line, in order to support the 3D revolution. The short course will cover among other topics, the usage of multiple dimensional and material metrology techniques such as Critical Dimension Scanning Electron Microscope (CDSEM), Transmission Electron Microscopy (TEM), X-ray Photoelectron Spectroscopy (XPS), X-ray Fluorescence (XRF), Atomic Force Microscopy (AFM), Optical scatterometry (OCD), and different aspects of hybrid approach and Machine-Learning usage in High Volume Manufacturing. While having these known systems deployed today, we will review new metrology platforms, which are potential to gain high attraction as they shift from Lab to Fab.

4. **Beyond FinFET Devices: GAA, CFET**, **2D Material FET,** Chung-Hsun Lin, Intel Corporation

   With the introduction of FinFET technology on Intel’s 22nm process node in 2011, the three-dimensional channel structure unleashed a new era of design-technology co-optimization for both high performance and low power workloads. In FinFETs, transistor density and performance scaling are driven by Fin geometry optimization, high-mobility channel materials and contact resistance reduction with scaled Contacted Poly Pitch (CPP) and gate length. As FinFET scaling comes to an end, there are several innovative device architectures for next generation technologies: from gate-all-around (GAA) transistor, complementary FET (CFET), to atomic channel FET with 2D materials. The GAA transistor is the most pragmatic architecture in the near term to enable incremental CPP and gate length scaling because of its limited perturbation to a conventional FinFET process integration and design flows. CFET (3D stacking) technology brings additional cell level area scaling benefit as well as heterogeneous integration benefit for high mobility channel enablement. 2D material FET provides the ultimate gate length scaling with high mobility channel capability. In this short course, we will focus on the status of these innovations with the corresponding engineering opportunities and challenges for high volume manufacturing.

5. **Heterogenous Integration Using Chiplets & Advanced Packaging,** Madhavan Swaminathan, Georgia Tech

   The semiconductor industry is moving towards heterogeneous integration for three primary reasons namely, 1) monolithic integration using large dies in advanced nodes is becoming uneconomical, 2) time to market using monolithic integration is becoming long because of design, yield and integration complexity, and 3) systems today are driven by heterogeneity where use of a single transistor process alone is insufficient to meet the requirements. But how does the landscape look like for heterogeneous integration? What are the advanced packaging platforms available for both 2.5D and 3D integration? What are the technologies available today and what are the emerging technologies? How does one compare the various technologies? What is the minimum chiplet size that can be assembled and the largest package size that can be supported? How does heterogeneity affect signal integrity and power delivery? In this presentation these questions will be answered where the various categories of advanced packaging technologies will be described and compared along with details on construction, line dimensions, form factor, bandwidth density, data rate, power delivery metrics, thermal management solutions, and system integration potential. Details on emerging technologies such as glass interposer will also be presented.

6. **Design-Technology Co-Optimization / System-Technology Co-Optimization,** Victor Moroz, Synposys

   Lithographic feature scaling pace started to slow down at 10nm node and is expected to stop scaling after 2nm node. Despite that, we see Moore's law continuing at least for the next 10 years with annualized transistor density increase of ~20% and annualized reduction of cost per transistor of ~15%. This progress is enabled by increasingly sophisticated DTCO (Design-Technology Co-Optimization) and STCO (System-Technology Co-Optimization) methodologies. This work illustrates DTCO and STCO methodologies applied to advanced CMOS logic and SRAM to explore and quantify different innovations in design and technology. One illustration is about operating CMOS at cryogenic temperatures. It requires significant reduction (over 300 mV) of threshold voltage, which is challenging for HKMG process, but can provide dramatic improvements in power consumption (close to 10x) or performance (over 40%). Another illustration is about the role of transistor variability as the driving force behind industry transitions from planar MOSFET to FinFET to GAA technologies. Besides these DTCO examples, we apply STCO analysis to 3D heterogeneous integration, which enables additional boost of transistor density and reduction of cost per function, but requires resolving multiple inter-related electrical, thermal, stress, and power delivery challenges. We share design and technology innovations that address these challenges.

Short Course 2: Emerging Technologies for Low Power Edge Computing
Sunday, December 12, 2021, 9:00 a.m. – 5:30 p.m.

Course Organizer: Huaqiang Wu, Tsinghua University
John Paul Strachan, Forschungszentrum Jülich

- Mobile NPUs for Intelligent Human Computer Interaction, Hoi-Jun Yoo, KAIST
- Brain-inspired strategies for optimizing the design of neuromorphic sensory-processing systems, Giacomo Indiveri, University of Zurich
- Memory based AI & Data Analytics solutions, Euicheol Lim, SK hynix
- Material strategies for memristor-based AI hardware and their heterointegration, Jeehwan Kim, MIT
- RRAM devices for data storage and in-memory computing, Wei Lu, University of Michigan

- Practical implementation of wireless power transfer, Hubregt Visser, IMEC

1. **Mobile NPUs for Intelligent Human Computer Interaction**, Hoi-Jun Yoo, KAIST

   Recently, Deep Neural Networks are widely used for realization of the AI services in cyber and physical world. In this presentation, firstly, the status of AI and DNN SoCs will be reviewed from the viewpoint of the mobile and edge AIs, and the evolution of DNN Accelerators. Especially, mobile, embedded and IoT deep learning hardware, low power NPU and reconfigurable NPU will be introduced. In addition, "Dynamically Reconfigurable Processor" architecture will be explained in detail with the real chip measurement results, such as human emotion recognition for intelligent HCI. Secondly, the On-Chip Training, which will be the next wave over the current AI revolution, will be explained for personalized and privacy protected AI applications. The personalization and autonomous adaptation to the environmental changes are possible with the on-chip supervised and reinforcement learning capability. Low power training processors will be explained with algorithm and hardware co-optimization methods. Real-time training, GAN and DRL examples will be introduced with dedicated training chips which are implemented for the many exciting low-power and high-performance applications such as object recognition and the object tracking applications in Gaming, AR/VR, Intelligent Robotics, Drones, Autonomous Driving, Security, Camera, Health Monitoring and IoT.

2. **Brain-Inspired Strategies for Optimizing the Design of Neuromorphic Sensory-Processing Systems**, Giacomo Indiveri, University of Zurich

   Recently, Artificial Intelligence (AI) neural networks and learning algorithms have emerged as a successful computing paradigm for solving a wide range of complex tasks. However for many practical purposes that involve real-time interactions with the environment these algorithms, and the conventional computing systems they are implemented on, cannot match the performance of biological systems. One of the reasons is that the principles of computation used by nervous systems is radically different from those of today's computers. In this talk I will present neuromorphic electronic circuits that directly emulate the physics of computation used by biological neural processing systems, and brain-inspired signal processing strategies to build beyond von Neumann ultra-low power computing technologies for real-world sensory-processing edge-computing applications.

3. **Memory based AI & Data Analytics Solutions**, Euicheol Lim, SK hynix

   The advent of the AI/Big data era is causing a rapid shift in computer architecture from computing-centric to data-centric. In order to provide a competitive AI-based service, it is necessary to process a huge amount of data quickly in the data center, and it is also needed to process more data at the edge server. However, in the traditional computing architecture where data movement occurs in the order of cache - memory - storage, data movement consumes more energy rather than data operation itself and the performance of the system largely depends on it. Near data processing can be a solution to address the data movement issue by offloading certain tasks near or in memory side, thus improving performance and energy efficiency. This course shows the demand of near data processing from the data pipeline and operation flow of the specific AI/Big data service system, and with a specific solution examples I'd like to explain what type of near data processing architecture is feasible. The analog computing in memory that processes data and processing in analog cell array will be introduced as an extreme example of near data processing. And as a more practical solution, the computational memory card solution will be covered as well. Also, we will discuss which part of the overall AI service system each solution will play a role in. In this course, we mainly focus on the solution and system perspectives rather than the device-level technology.

4. **Material Strategies for Memristor-based AI Hardware and their Heterointegration**, Jeehwan Kim, Massachusetts Institute of Technology

   Conventional memristors typically utilize a defective amorphous solid as a switching medium for defect-mediated formation of conducting filaments. However, the imperfection of the switching medium also causes stochastic filament formation leading to spatial and temporal variation of the devices. In this talk, I will present our material strategy to precisely confine the conducting paths in memristors which allow us to operate 1R-based crossbar arrays with a great programmability. By embedding this crossbar array into the edge of heterogeneously integrated chip, we demonstrate a reconfigurable heterochips with stackability. The reconfigurable chip features (1) memristor crossbar arrays for non-von Neumann computing and (2) optical communication between chips enabled by heterointegrating LEDs and photodiodes. I will discuss about outlook of our recent reconfigurable heterogeneous integration schemes for future electronics.

5. **RRAM Devices for Data Storage and In-Memory Computing**, Wei Lu, University of Michigan

   Neural Networks (NNs) are now widely used in artificial intelligence (AI) applications. However, NNs often come with high computation and energy cost when implemented using existing hardware. In-memory computing (IMC) systems can potentially offer orders of magnitude improvements in energy consumption and throughput. In this talk I will discuss such systems based on an emerging device – resistive-random access memory (RRAM). An RRAM is a two-terminal electronic device with an inherent memory effect, driven by internal ion re-distribution within a solid-state switching medium. As a memory device, RRAM is being commercialized by several fabs for applications such as embedded memory and stand-alone data storage. They are also widely considered as a promising candidate for in-memory computing and neuromorphic computing hardware due to RRAM's ability to simultaneously store weights and process information at the same physical locations. Prototype RRAM-based IMC circuits can already perform tasks such as feature extraction, data clustering and image analysis by utilizing the efficient MAC operations offered by IMC circuits. Direct RRAM/CMOS integration further allows all functions to be implemented in an integrated chip and re-programmable for different tasks. Approaches towards a scalable IMC system will be introduced to address device non-idealities and accommodate practical AI models.

6. **Practical Implementation of Wireless Power Transfer**, Hubregt Visser, IMEC

   Since the invention of radio (Hertz, Marconi) at the end of the 19th century, far-field transfer of energy has been feasible. Although radio has been further developed for the transfer of information, the idea of long-distance Wireless Power Transfer (WPT) was picked up from the beginning by Nikola Tesla and was clearly demonstrated by Harrell Noble from Westinghouse at the Chicago World Fair in 1933-1934, after which interest decreased. The availability of compact, high-power microwave sources regained the interest in WPT and in 1964, William Brown from Raytheon demonstrated a wirelessly powered model helicopter. Again, interest decreased, since radiative WPT cannot, in a practical way, power or charge mobile phones, tablets or laptops over several meters distance. For that, inductive (resonant) WPT over very short distances has been developed. Accepting that 'power through the air' is feasible only for ultra-low power applications, we can concentrate now on IoT devices such as sensors and headphones and remotes. Given the ultra-low power levels, the design of a long-distance WPT receiver is a non-trivial task. In this presentation, the different building blocks of such a receiver, i.e., antenna, rectifier, boost converter and load, will be discussed. This will be done by going through the design steps of a couple of practical, remotely powered applications like an electrical clock, a temperature sensor with display and a wireless temperature and humidity sensor.

   Session 1: Plenary
   Monday, December 13, 9:00 AM
   Grand Ballroom B

Co-Chairs: Tibor Grasser, TU Wien
Barbara De Salvo, Facebook

1.1 The Smallest Engine Transforming Humanity: The Past, Present, and Future, K. Kim, Samsung

1.2 Creating the Future: Augmented Reality, the next Human-Machine Interface, M. Abash, Facebook

1.3 Quantum Computing Technology, H. Riel, IBM Zurich

Session 2: Memory Technology - STT-MRAM technology and exploratory devices
Monday, December 13, 1:30 PM
Grand Ballroom A
Co-Chairs: Etienne Nowak, CEA-Leti
Jung-Hyuk Lee, Samsung Electronics

1:35 PM
2-1 28nm CIS-Compatible Embedded STT-MRAM for Frame Buffer Memory, K. Lee, D. S. Kim, J. H. Bak, S. P. Ko, W. C. Lim, H. C. Shin, J. H. Lee, J. H. Park, J. H. Jeong, J. M. Lee, T. Kai, H. Sato, J. W. Lee, K. H. Ryu, Y. J. Kim, S. H. Han, B. Y. Seo, K. S. Suh, H. H. Kim, H. T. Jung, D. H. Jang, N. Y. Ji, M. J. Eom, I. H. Kim, K. Lee, K. H. Hwang, Y. J. Song and H. S. Kim, Samsung Electronics Co

We demonstrate embedded STT-MRAM fully integrated onto 28nm CIS logic platform, highlighting the world-best macro density of 13.94 Mb/μm^2. MTJ stack has been improved for frame buffer applications, achieving write speed <50ns and endurance >1E10 cycles. Furthermore, we have confirmed scalability of the CIS-compatible MTJ processes beyond 28nm.

2:00 PM
2-2 A 20Mb Embedded STT-MRAM Array Achieving 72% Write Energy Reduction with Self-termination Write Schemes in 16nm FinFET Logic Process, T. Ito, T. Saito, Y. Taito, K. Sonoda, G. Watanabe, K. Matsubara, A. Kanda, T. Shimoi, K. Takeda, T. Kono, Renesas Electronics Corporation

We present the low energy write techniques and measurement results of 20Mb embedded STT-MRAM test chip in 16nm FinFET logic process. Proposed self-termination write schemes with slope write voltage and current pulse and variable parallel bit write sequence achieve 72% write energy reduction and 50% total write pulse time reduction.

2:25 PM
2-3 First Experimental Demonstration of MRAM Data Scrubbing: 80 Mb MRAM with 40 nm junctions for Last Level Cache Applications, H. Wu, V. Katragadda, E. Evarts, E. Edwards, R. Southwick, A. Dutta, G. Lauer, V. Mehta, R. Johnson, O. van der Straten, A. Reznicek, M. Wordeman, M. Rizzolo, R. Patlolla, D. Metzler, C. Yang, D. Edelstein, D. Canaperi, S. Teehan, J.M. Slaughter and D.C. Worledge IBM Research

This work provides the first experimental demonstration of data scrubbing on MRAM for last level cache, using 80Mb arrays with 40nm CD. Chip error rate (CER) is modelled first and then scrubbing is applied with MTJ optimization, delivering 30% energy barrier reduction and 2 orders higher endurance without CER penalty.

2:50 PM Coffee Break

3:15 PM

2-4 Design Challenges and Solutions of Emerging Nonvolatile Memory for Embedded Applications (Invited), Y.-D. Chih, C.-C. Chou, Y.-C. Shih, C.-F. Lee,W.-S. Khwa, C.-Y. Wu, K.-H. Shen, W.-T Chu, M-F Chang, H. Chuang, T.-Y. J. Chang, Taiwan Semiconductor Manufacturing Company (TSMC)

STT-MRAM and RRAM are attractive candidates to replace charge-based embedded flash. The key challenges include small read window, large write current, endurance and data retention. Data retention during reflow , WLCSP and the magnetic field interference to STT-MRAM are the additional challenges. TDCO solutions were proposed to address these challenges.

3:40 PM

2-5 2X reduction of STT-MRAM switching current using double spin-torque magnetic tunnel junction, G. Hu, G. Lauer, J. Z. Sun, P. Hashemi, C. Safranski, S. L. Brown, L. Buzi, E. R. J. Edwards, C. P. D'Emic, E. Galligan, M. G. Gottwald, O. Gunawan, H. Jung, J. Kim, K. Latzko, J. J. Nowak, P. L. Trouilloud, S. Zare, and D. C. Worledge, IBM-Samsung MRAM Alliance, IBM TJ Watson Research Center

We introduce a new device, Double Spin-torque Magnetic Tunnel Junction (DS-MTJ), utilizing spin torque from both free-layer interfaces to reduce I_c by 2x. Unlike double MTJ, the DS-MTJ does not suffer from reduced device MR. Experimental data shows 2x reduction in I_c and write-error-rate = 1e-6 with 2-3 ns write pulses.

4:05 PM

2-6 Fast Switching Down to 3.5 ns in Sub-5-nm Magnetic Tunnel Junctions Achieved by Engineering Relaxation Time, B. Jinnai, J. Igarashi, T. Shinoda, K. Watanabe, S. Fukami, and H. Ohno, Tohoku University

We show fast switching down to 3.5 ns while maintaining high data retention in sub-5-nm ultra-small magnetic tunnel junctions (MTJs) using multilayered ferromagnets (FMs). The MTJ technology can cover a wide variety of applications even at the ultra-small scale needed for advanced-node integrated technology.

Session 3: Advanced Logic Technology Focus Session- Stacking of devices, circuits, chips: design, fabrication, metrology - challenges and opportunities

Monday, December 13, 1:30 PM
Grand Ballroom B
Co-Chairs: Oleg Golonzka, Intel
Yao-Jen Lee, Taiwan Semiconductor Research Institute

1:35 PM

3-1 CFET Design Options, Challenges, and Opportunities for 3D Integration (Invited), L. Liebmann, J. Smith, D. Chanemougame, and P. Gutwin. TEL Technology Center, America, LLC

Design-details of standard-cell-architectures using complementary-field-effect-transistors (CFET) are explored. The primary structural-elements of CFET are reviewed and the layout-impact of several 2nd-order technology-constructs is analyzed. A manufacturability-assessment and cost-analysis of the resulting CFET technology-architecture-definition is presented. Finally, the extendibility of CFET to 3.5-track cell-height as well as higher-order 3D-integration is explored.

2:00 PM

3-2 3D sequential integration: applications and associated Key Enabling Modules (design & technology) (Invited), P. Batude, O. Billoint, S. Thuries, P. Malinge*, C. Fenouillet-Beranger, A. Peizerat, G. Sicard, P. Vivet, S. Reboh, C. Cavalcante, L. Brunet, X. Garros, T. Mota Frutuoso, B. Sklenard, J. Lacord, D. Lattard, C. Theodorou***, V. Lapras, M. Mouhdach, G. Gaudin**, G. Besnard**, I. Radu**, F. Ponthenier, A. Farcy*, T. Matheret, P. Brunet, F. Milesi, L. Le Van-Jodin, A. Sarrazin, B. Perrin, C. Moulin, S. Maitrejean, M. Alepidis***, I. Ionica***, S. Cristoloveanu***, E. Josse*, F. Guyader*, F. Gaillard , M. Vinet F. Andrieu, J. Arcamone, E. Ollier, CEA, Leti, Minatec Campus, and University Grenoble Alpes, *ST Microelectronics, ** SOITEC, ***IMEP-LAHC

3D sequential integration (3DSI) is envisioned for highly miniaturized smart imagers and fine pitch logic and memory imbrication. This paper describes partitioning in 3DSI and design methodologies. A status is also done on low temperature processes and device performance adapted for these applications (i.e. digital ≤1V and analog ≥2.5V devices).

2:25 PM
3-3 Inspection and metrology challenges for 3 nm node devices and beyond (Invited), T. Shohjoh, M. Ikota, M. Isawa, G. F. Lorusso*, N. Horiguchi*, B. Briggs*, H. Mertens*, J. Bogdanowicz*, P. De Bisschop*, A.-L. Charley*, Hitachi High-Tech Corporation, *imec, Leuven, Belgium

We report on non-destructive inspection and metrology potential of high-voltage (HV) critical dimension scanning electron microscopy (CD-SEM) for 3-nm node devices and beyond. We have demonstrated the lateral recess depth of the buried SiGe layer can be measured, and also have observed the buried voids and residue using HV CD-SEM.

2:50:00 PM Coffee Break

3:15 PM
3-4 Heterogeneous Integration Enabled by the State-of-the-Art 3DIC and CMOS Technologies: Design, Cost, and Modeling, (Invited) X.-W. Lin, V. Moroz, X. Xu, Y. Gao, D. Rennie, P. Asenov, S. Smidstrup, D. Sherlekar, Z. Qin, T. Fang, J. Lee, M. Choi, and S. Jones*, Synopsys, Inc., *IC Knowledge LLC

Various aspects of heterogeneous integration are reviewed, including (1) 3DIC interconnect options, (2) die-to-die interface design, (3) cost model for SOC disaggregation, and (4) physical modeling of a novel design with 2nm SOC on RDL interposer for package-die co-optimization, in terms of power integrity and thermal, mechanical, and electrical properties.

3:40 PM
3-5 Design for 3D Stacked Circuits, (Invited) P. Franzon, W. Davis, E. Rotenberg, J. Stevens, S. Lipa, T. Nigussie, H. Pan, L. Baker, J. Schabel, S. Dey, and W. Li, North Carolina State University

2.5D and 3D technologies can give rise to a node equivalent of scaling due to improved connectivity. Aggressive exploitation scenarios include functional partitioning, circuit partitioning, logic on DRAM, design obfuscation and modular chiplets. Design issues that need to be addressed include thermal management, design for test and computer aided design.

4:05 PM
3-6 3D SoC integration, beyond 2.5D chiplets (Invited), E. Beyne, D. Milojevic, G. Van der Plas, G. Beyer, imec

2.5D “Chiplet” integration is mainly limited to latency-tolerant applications. In contrast, the “3D-SoC” design approach, an extension of the 2D System-on-Chip design methodology, reduces latency between block. In 3D-SoC, the system is automatically partitioned into separate chips that are concurrently designed & interconnected in the 3rd dimension with scaled pitches.

4:30 PM
3-7 Foundry Perspectives on 2.5D/3D Integration and Roadmap (Invited), D. C. H. Yu, C-T Wang and H. Hsia Taiwan Semiconductor Manufacturing Company

Advanced foundry 2.5D/3D system integration technology platform (3DFabric™) have been established to help realize chiplets integration to sustain Moore’s law. We show that, by scaling 2.5D system envelop and 3D bond pitch, energy efficient performance (EEP) is enhanced 2x from-node-to-node. We integrate passives, photonics and cooling modules to further this.

Session 4: Microwave, Millimeter Wave and Analog - Innovative RF technologies for low power and RF/mmW applications
Monday, December 13, 1:30 PM
Continental Ballrooms 1-3
Co-Chairs: Rabia Tugce Yazicigil, Massachusetts Institute of Technology
Hongtao Xu, Fudan University

1:35 PM
4-1 Overview of design challenges for automotive radar MMICs (Invited), M. Martinez-Vazquez, Renesas Electronics Europe

This paper presents some of the challenges for the design of multi-channel MMIC (Monolithic microwave integrated circuits) transceivers to be usedin automotive radar systems. The focus will be on the influence of the RF (radio frequency) frontend performance, especially in relation with the maximum achievable range.

2:00 PM
4-2 Monolithically Integrated Self-Biased Circulator for mmWave T/R MMIC Applications, Y. Cui, H. Chen*, S. Chen, D. Linkhart**, H. Tan***, J. Wu*, S. Yoon, M. Geiler**, A. Geiler**, E. Beam, A. Xie, N. Wang*, M. Regan, M. Kruzich, B. Nguyen, D. White, A. Ketterson, C. Lee, D. Willis***, H. Wang*, and Y. Cao, Qorvo, *University of Southern California, Metamagnetics, ***Southern Methodist University

Monolithically on-chip integrated circulator devices are demonstrated for the first time through the direct integration of polycrystalline hexaferrite magnetic material with GaN/SiC wafers. The first full-duplex transmit/receive MMIC integrated on a semiconductor wafer has also been demonstrated, showing over 100 times in size miniaturization as compared to conventional technology.

2:25 PM
4-3 Green Poly-Si TFTs: RF Breakthroughs (fT/fmax = 63.6/30 GHz) by an Ingenious Process Design for IoT Modules on Everything, Y.-J. Ye, P.-H. Yu, C.-K. Lee, P.-W. Li, K.-M. Chen*, G.-W. Huang*, and H.-C. Lin, National Yang Ming Chiao Tung University, *Taiwan Semiconductor Research Institute (TSRI)

We report a low-temperature process platform for fabricating RF poly-Si TFTs with $f_T/f_{max}$of 63.6/30 GHz. The superior RF performance is achieved by an exquisite combination of large-grain poly-Si channel, T-

gate, air-spacers, and silicide electrodes, using green laser crystallization, high etching selectivity, salicide process, and microwave annealing for S/D activation.

2:50 PM Coffee Break

3:15 PM
4-4 Phase-Change Material RF Switches and Monolithic Integration in 180 nm RF-SOI CMOS Processes (Invited), G. Slovin, N. El-Hinnawy, K. Moen, D. Howard. Tower Semiconductor

Improvements to the PCM RF switch have resulted in increased power handling and cycling endurance. Full wafer endurance tests to 100-million cycles show reduced R_{ON}-drift and variability. Devices cycled 1-billion times demonstrate similar results. A new process is presented with the PCM RF switch monolithically integrated into a RF-SOI process.

3:40 PM
4-5 Beyond 8 THz Displacement-field Nano-switches for 5G and 6G Communications, M. Samizadeh Nikoo, T. Wang, P. Sohi, M. Zhu, F. Qaderi, R. A. Khadar, A. Floriduz, A. M. Ionescu, and E. Matioli, École polytechnique fédérale de Lausanne

Here we demonstrate that the fast switching of displacement-fields confined in a few-nanometers-thin crystal between a textured metal and an electron sheet provides cut-off frequencies above 8 THz, with low ON-state resistance of 120 Ω.µm, low parasitic capacitance of 100 aF.μm^{-1}, and below 10-ps switching-time for 5G communications, and beyond.

Session 5: Power Devices and Systems - GaN power devices, technologies, and circuits
Monday, December 13, 1:30 PM
Continental Ballroom 4
Co-Chairs: Rebecca Nikolic, Lawrence Livermore National Laboratories
David Sheridan, Alpha and Omega Semiconductor

1:35 PM
5-1 200 V GaN-on-SOI Smart Power Platform for Monolithic GaN Power ICs, T. Cosnier, O. Syshchyk*, B. De Jaeger, K. Geens, D. Cingu, Elena Fabris, M. Borga, A. Vohra, M. Zhao, B. Bakeroot**, D. Wellekens, A. Magnani, P. Vudumula*, U. Chatterjee, R. Langer and S. Decoutere, Imec, *KU Leuven, Belgium, **Ghent University

This paper demonstrates a 200 V GaN-on-SOI smart power ICs platform developped on 200 mm substrates. Depletion-mode (d-mode) MIS-HEMTs and Gated-Edge-Termination Schottky barrier diodes (GET-SBDs) have been successfully integrated in an enhancement-mode (e-mode) HEMT technology baseline. A variety of low-voltage devices and passive components further supports the GaN ICs platform.

2:00 PM
5-2 A GaN Power Integration Platform Based on Engineered Bulk Si Substrate with Eliminated Crosstalk between High-Side and Low-Side HEMTs, G. Lyu, J. Wei*, W. Song, Z. Zheng, L. Zhang, J. Zhang, Y. Cheng, S. Feng, Y. Hon Ng, T. Chen, K. Zhong, J. Liu**, R. Zeng**, K. J. Chen*, the Hong Kong University of Science and Technology, * Peking University, ** Tsinghua University

GaN on engineered bulk Si (EBUS) substrate is proposed for GaN power IC with PN-junctions and trenches providing isolations. The concept was demonstrated with 200-V p-GaN HEMTs and the crosstalk effects between HS/LS HEMTs are effectively eliminated.

2:25 PM
5-3 SiN/in-situ-GaON Staggered Gate Stack on p-GaN for Enhanced Stability in Buried-Channel GaN p-FETs, L. Zhang, Z. Zheng, Y. Cheng, Y. Hon Ng, S. Feng, W. Song, T. Chen, K. J. Chen, The Hong Kong University of Science and Technology

A delicate SiN_x/in-situ-GaO_xN_{1-x} staggered gate stack is designed for GaN p-FETs for stability enhance-ment. It yields a barely changed VTH within wide bias and temperature ranges, thereby leading to stable GaN complementary logic ICs. The optimized ICs exhibit high stability over long-period operations and at temperatures up to 400 °C.

2:50 PM
5-4 GaN/AlGaN superlattice based E-mode p-channel MES-FinFET with regrown contacts and >50 mA/mm on-current, A. Raj, A. Krishna, N. Hatui, B. Romanczyk, C. Wurm, M. Guidry, R. Hamwey, N. Pakala, S. Keller, and U. K. Mishra, Department of Electrical and Computer Engineering, University of California Santa Barbara

In this work, we report on GaN/AlGaN superlattice based MES-FinFET devices with MOCVD regrown p^+ contacts around the fins. 75 nm wide FinFETs showed a normally-off operation with an on-current of 65 mA/mm, highest ever reported for any GaN based E-mode pFETs. Simultaneously, a large I_{on}/I_{off} $>10^7$ was also achieved.

3:15 PM Coffee Break

3:40 PM
5-5 Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV, M. Xiao, Y. Ma, Z. Du*, V. Pathirana**, K. Cheng***, A. Xie****, E. Beam****, Y. Cao****, F. Udrea**, H. Wang*, Y. Zhang. Virginia Polytechnic Institute and State University, *University of Southern California, **University of Cambridge, United Kingdom. ***Enkris Semiconductor, China. ****Qorvo

We present a new device concept, the Multi-Channel Monolithic-Cascode high-electron-mobility transistor (MC^2-HEMT), and experimentally demonstrated normally-off AlGaN/GaN MC^2HEMTs with breakdown voltage from 3.45 kV up to over 10 kV. This is the first report of 3-kV+ normally-off GaN devices, and our MC^2HEMTs show the highest figure-of-merits in all 6.5-kV+ transistors.

4:05 PM
5-6 Emerging circuit techniques to utilize wide-bandgap semiconductors in compact, lightweight, and efficient power converters (Invited), R.C.N. Pilawa-Podgurski, University of California, Berkeley

Wide-bandgap power devices enable dramatic improvement in switching speed, on-state resistance, and operating temperature. However, to fully utilize the increased figure-of merit (FOM) of these new silicon carbide (SiC) and gallium nitride (GaN) devices, the power electronics designer must also consider new circuit techniques. In particular, the high-speed switch transition can give rise to undesirable ringing, voltage overshoot, and electromagnetic interference (EMI), if not managed properly. Here, we outline some challenges associated with power electronics design with wide-bandgap power semiconductors, and present solutions that help unleash the true potential of these groundbreaking devices.

Session 6: Reliability of Systems and Devices - Reliability studies on advanced memories: Ferroelectric, ReRAM, DRAM
Monday, December 13, 1:30 PM
Continental Balroom 5
Co-Chairs: Paolo Pavan, Università de Modena e Reggio Emilia

Xavier Garros, CEA-Leti

1:35 PM

6-1 Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, N. Tasneem, Z. Wang, Z. Zhao*, N. Upadhyay**, S. Lombardo, H. Chen, J. Hur, D. Triyoso***, S. Consiglio***, K. Tapily***, R, Clark***, G. Leusink***, S. Kurinec*, S. Datta**, S. Yu, Kai Ni*, M. Passlack#, W. Chern, A. Khan, Georgia Tech, *Rochester Institute of Technology **University of Notre Dame School of MSE, Georgia Tech, ***TEL Technology Center, America, LLC, #Taiwan Semiconductor Manufacturing Company

We track carrier capture and emission dynamics during write operations in n-type ferroelectric-field-effect transistors by directly and separately measuring the trap related hole and electron currents through the body terminal and shorted source-drain, respectively. The universality of the suggested mechanisms is confirmed in different FEFETs fabricated in different facilities.

2:00 PM

6-2 Improved Multi-bit Storage Reliablity by Design of Ferroelectric Modulated Anti-ferroelectric Memory, Y. Xu*, Y. Yang, S. Zhao, T. Gong, P. Jiang*, Y. Wang*, P. Yuan*, A. Dang*, Y. Chen*, S. Lv*, Y. Ding*, Y. Wang, J. Bi, Q. Luo, M. Liu, Institute of Microelectronics of Chinese Academy of Sciences, *University of Chinese Academy of Sciences, Beijing, China.

For the first time, we present a new concept of ferroelectric modulated anti-ferroelectric memory. Independent 2-step state switching and large polarization are presented. as a promising option for multi-bit storage in advanced technology nodes. the improved multi-bit storage reliability is verified by kinetic Monte Carlo modeling.

2:25 PM

6-3 Accurate Picture of Cycling Degradation in HfO2-FeFET Based on Charge Trapping Dynamics Revealed by Fast Charge Centroid Analysis, R. Ichihara, Y. Higashi, K. Suzuki, K. Takano, Y. Yoshimura, T. Hamai, K. Takahashi, K. Matsuo, Y. Nakasaki, M. Suzuki, Y. Kamimuta, M. Saitoh, Kioxia Corporation

We establish an accurate picture of cycling degradation in HfO2-FeFET based on the dynamics of various charge-trapping (electron/hole, stable/unstable, program-induced/read-induced) revealed by fast charge centroid analysis. Cycling-induced fixed electron at HfO2/SiO2 interface induces an additional reversible hole-trapping leading to Vth window narrowing.

2:50 PM

6-4 Improving Edge Dead Domain and Endurance in Scaled HfZrOx FeRAM, Y.-D. Lin, P.-C. Yeh, Y.-T. Tang*, J.-W. Su, H.-Y. Yang, Y.-H. Chen**, C.-P. Lin**, P.-S. Yeh, J.-C. Chen, P.-J. Tzeng, M.-H. Lee***, T.-H. Hou,**, S.-S. Sheu, W.-C. Lo, and C.-I Wu#, Industrial Technology Research Institute, *National Central University, Taiwan. **National Yang Ming Chiao Tung University, ***National Taiwan Normal University, Taiwan, #National Taiwan University, Taiwan.

Scaling in area and voltage and its interplay with reliability of MFM capacitors are explored in scaled FeRAM. Size-dependent ferroelectricity degradation due to edge dead domains is identified. The scaled MFM achieves high Psub>$_r$36μC/cm^2), small area (0.16μm ^{2}), excellent reliability(>10^{11}cycles; retention>10 years at 85ºC), low operating voltage(1.7V), and 100% 1-kb array yield.

3:15 PM Coffee Break

3:40 PM

6-5 Development of spatial nearest-neighbor analysis and Clustering/Gibbs statistical methodology for filament percolation in dielectric breakdown and forming process in ReRAM devices, E. Wu, F. Stelliar, T. Ando, P. Song, M. Frank

We develop a nearest-neighbor analysis to investigate spatial filament distributions from PEM, STM, IR-thermography measurements. For non-uniform BD spots, a clustering model is shown to agree with the data. For ReRAMs, a Gibbs model with a Markov-Chain Monte-Carlo approach is developed to explain filament interactions with a generalized Morse potential.

4:05 PM

6-6 Reliability Characterization for Advanced DRAM using HK/MG + EUV Process Technology, S. Lee, G.-J. Kim, N-H. Lee, KW. Lee, BW. Woo, J. Jin, JG. Kim, YS. Lee, HS. Kim, and S. Pae
Memory Division, Samsung Electronics, Hwasung, Republic of Korea.

Extensive reliability characterization of advanced DRAM with EUV process technology is presented. WLR reliability showed well above 10 years intrinsic performance and were also validated with long term stresses at package level. DIMMs were tested using server systems for more than 1 year, accurately validating the excellent reliability results.

Session 7: Emerging Device and Compute Technology - 2D Channel Transistors
Monday, December 13, 1:30 PM
Continental Ballroom 6
Co-Chairs: Nicolas Loubet, IBM Research
Eric Pop, Stanford University

1:35 PM

7-1 Advancing 2D Monolayer CMOS Through Contact, Channel and Interface Engineering, K. P. O'Brien, C. J. Dorow, A. Penumatcha, K. Maxey, S. Lee, C. H. Naylor, A. Hsiao, B. Holybee, C. Rogan, D. Adams, T. Tronic, S. Ma, A. Oni, A. Sen Gupta, R. Bristol, S. Clendenning, M. Metz, U. Avci, Intel Corporation

We demonstrate 2D monolayer transistor path towards silicon replacement and improved NMOS and PMOS contacts with manufacturable metals (i.e. 146 Ω-µm NMOS). We established BEOL 300mm wafer TMD growth, on-wafer seed growth and channel curing for improved performance. The results show best published drive currents for devices with good SS.

2:00 PM

7-2 Antimony Semimetal Contact with Enhanced Thermal Stability for High Performance 2D Electronics, A-S Chou*, T. Wu, C-C Cheng, S-S Zhan*, I-C Ni*, S-Y Wang**, Y-C Chang**, S-L Liew, E. Chen, W-H Chang**, C-I Wu*, J. Cai, H.-S. Philip Wong and H. Wang*, TSMC, * National Taiwan University, **National Yang Ming Chiao Tung University

L_{CH}=50nm Sb-contacted MoS_2 nFET achieved remarkable I_{ON} >600µA/µm at V_{DS}=1V with a low R_C ~0.66kΩ·µm, and also demonstrated fully operational after 400°C annealing in contrast to 300°C only for Bi-contacted devices, indicating the potential of Sb semimetal contact towards reaching thermal budget for BEOL compatibility and high performance 2D electronics.

2:25 PM

7-3 Sub-200 Ω·µm Alloyed Contacts to Synthetic Monolayer MoS2, A. Kumar, K. Schauble, K. M. Neilson, A. Tang, P. Ramesh, H.-S. Philip Wong, E. Pop, K. Saraswat. Stanford University

We demonstrate ultra-low contact resistance to monolayer MoS_2 of 190 Ω·µm using In-Au alloy and 270 Ω·µm using Sn-Au alloy contacts, which are among the best reported to date. We perform a statistical study of 720 transistors, revealing the 'best' and 'average' alloyed contacts, for the first time.

2:50 PM Coffee Break

3:15 PM

7-4 Dual gate synthetic MoS2 MOSFETs with 4.56µF/cm2 channel capacitance, 320µS/ µm Gm and 420 µA/ µm Id at 1V Vd/100nm Lg, X. Wu, D. Cott, Z. Lin, Y. Shi, B. Groven, P. Morin, D. Verreck, Q. Smets, H. Medina, S. Sutar, I. Asselberghs, I. Radu and D. Lin.IMEC, Leuven, Belgium

We have engineered dual gate MoS2 transistors with scaled top and back gate stacks. A GdAlOx interfacial layer has been introduced to improve Vt control, hysteresis, and mobility. Connected dual gate MOSFET with 1-2ML MoS_2 channel reaches 420µA/um drain current and 4.56µF/cm^2 capacitance.

3:40 PM

7-5 Demonstration of Vertically-stacked CVD Monolayer Channels: MoS2 Nanosheets GAA-FET with Ion>700 µA/µm and MoS2/WSe2 CFET, Xiong Xiong, Anyu Tong, Xin Wang*, Shiyuan Liu, Xuefei Li*, Ru Huang and Yanqing Wu*, Peking University, *Huazhong University of Science and Technology

In this work, we demonstrate the CVD 2-monolayer-MoS_2-stacked nanosheets using a gate-all-around fashion. The high I_{on} >400 µA/µm per channel footprint at V_d=1 V is achieved. Furthermore, the vertical-stacked CVD MoS_2/WSe_2 CFETs based are also demonstrated for the first time with about 50% footprint reduction compared with the planar devices.

Session 8: Modeling and Simulation - Memory Technology

Monday, December 13, 1:30 PM

Continental Ballrooms 7-9

Co-Chairs: Hemant Dixit, Wolfspeed

Philippe Blaise, Silvaco

1:35 PM

8- Multiscale Modeling of Al0.7Sc0.N-based FeRAM: the Steep Switching, Leakage and Selector-free Array,** C. Liu, Q. Wang*, W. Yang**, T. Cao,***, L. Chen, M. Li, F. Liu**, D. K. Loke*, J. Kang**, and Y. Zhu. A*STAR, * Singapore University of Technology and Design, **Peking University, ***Nanyang Technological University

By multiscale modeling, the steep switching and the leakage in ferroelectric $Al_{0.7}Sc_{0.3}N$ are investigated. The tight distribution of Ec is attributed to highly uniform material and the hopping assisted by N vacancies dominate the leakage current. A circuit model is established to project the behavior of the selector-free array.

2:00 PM

8-2 Computational Study for Spin-orbit Torque Magnetic Random Access Memory, Y. Jiang, H. Zhou, D. Zhu, C. Wang, Z. Wang, and W. Zhao, Beihang University

We provide the first comprehensive computational study of spin-orbit torque magnetic random-access memory (SOT-MRAM). A framework combining ab initio and micromagnetic/macrospin simulations is

proposed. We find IrMn with broken magnetic symmetry a promising candidate for high-performance SOT-MRAM. Our work paves the way to exploit new materials and optimize SOT-MRAM.

2:25 PM

8-3 First Theoretical Modeling of the Bandgap-Engineered Oxynitride Tunneling Dielectric for 3D Flash Memory Devices Starting from the Ab Initio Calculation of the Band Diagram to Understand the Programming, Erasing and Reliability, Wei-Chen Chen, Hang-Ting Lue, Sheng-Ting Fan, Tzu-Hsuan Hsu, Pei-Ci Jhang, *Ulrik G. Vej-Hansen, *Petr A. Khomyakov, **Keng-Hua Lin, Keh-Chung Wang, and Chih-Yuan Lu. Macronix International Co., Ltd. *Synopsys Denmark, **Synopsys Taiwan Co., Ltd.

For the first time we use the ab initio quantum simulation to model the bandgap for oxynitride, and explain the measured data of programming, erasing, and reliability aspects. It is demonstrated that a modest nitrogen-doped SiON provides VBO of 3.2eV from silicon, enabling efficient –FN hole erasing.

2:50 PM

8-4 Understanding the ISPP Slope in Charge Trap Flash Memory and its Impact on 3D NAND Scaling, D. Verreck, A. Arreghini, F. Schanovsky*, G. Rzepa*, Z. Stanojevic*, F. Mitterbauer*, C. Kernstock*, O. Baumgartner*, M. Karner*, G. Van den bosch, M. Rosmeulen. Imec, *Global TCAD Solutions GmbH

We present a physical description that explains the non-ideal ISPP slope in charge trap flash memories. We derive a mathematical model and implement a 2.5-D TCAD model to investigate 3D NAND flash devices with scaling vertical pitch. We assess high-k CTL and airgaps for program voltage mitigation.

3:15 PM Coffee Break

3:40 PM

8-5 A New Surface Potential and Physics Based Compact Model for a-IGZO TFTs at Multinanoscale for High Retention and Low-Power DRAM Application, J. Guo, *, K. Han**, S. Subhechha***, X. Duan, *, Q. Chen, *, D. Geng, S. Huang, *, L. Xu, J. An, G. Sankar Kar***, X. Gong**, L. Wang*, L. Li*, Institute of Microelectronics of the Chinese Academy of Sciences, *University of Chinese Academy of Sciences, **National University of Singapore (NUS), ***imec

A compact model for nanoscale a-IGZO TFTs is proposed accounting for the effect of scaling. Particularly, it is achieved with finite-size corrected hopping and percolation models derived using connected subnetworks. Final projections of current characteristics are in excellent agreement with experiments, considering extreme-scaling induced severe short channel and contact effects.

4:05 PM

8-6 High-Density and High-Speed 4T FinFET SRAM for Cryogenic Computing, V. Pi-Ho Hu, C-J Liu*, H-L Chiang**, J-F Wang,**, C-C Cheng**, T-C Chen**, M-F Chang**
National Taiwan University, Taipei, Taiwan. *National Central University, Taoyuan, Taiwan. **Taiwan Semiconductor Manufacturing Company

The 4T FinFET SRAMs with reduced dynamic energy are proposed for cryogenic computing applications for the first time. We demonstrate that the 4T cryogenic FinFET SRAM at 77K surpasses the 6T SRAMs in the cell area (-20.3%), read access time (-44%), write time (-46%), write stability (2.3x), and EDP (-53%).

Session 9: Optoelectronics, Displays, and Imaging - Emerging Detectors and Displays Technologies
Monday, December 13, 1:30 PM
Imperial Ballroom A
Co-Chairs: Rachel Grange, ETH Zurich
Lucio Pancheri, University of Trento

1:35 PM
9-1 TiOx/Ti/TiOx Tri-layer Film-based Waveguide Bolometric Detector for On-Chip Si Photonic Sensors, J. Shim, J. Lim, D-M Geum, J-B You*, H. Yoon, J. Pyo Kim, W. Jin Baek, J-H Han**, SH Kim, Korea Advanced Institute of Science and Technology (KAIST), *National Nanofab Center (NNFC), **Korea Institute of Science and Technology (KIST)

We demonstrate an on-chip optical power monitoring at the near-infrared using TiOxTi/TiO$_x$tri-layer film-based waveguide bolometric detector on silicon-on-insulator platform for the optical sensors, which can be extended to the mid-infrared. It exhibits the record-high temperature-coefficient of resistance of -2.296%/K and sensitivity of -46.45%/mW with low wavelength-dependency among waveguide bolometers.

2:00 PM
9-2 Macroscopic-Assembled-Graphene Nanofilms/Germanium Broadband Photodetectors, L. Liu, X. Cao*, L. Peng**, S. Chanakya Bodepudi, S. Wu, W. Fang**, J. Liu***, Y. Xiao***, X. Wang, Z. Di***, R. Cheng*, Y. Xu, C. Gao**, B. Yu*

ZJU-UIUC Joint Institute, *ZJU-Hangzhou Global Scientific and Technological Innovation Center, **Zhejiang University, ***Chinese Academy of Sciences

By integrating Ge with the large-scale, high-quality multilayer graphene, we demonstrated a high-performance Schottky diode, which shows a wide detection bandwidth of 1.5 to 7 µm with corresponding responsivities ranging from 1.1 A/W to 40 mA/W, D* between $10^{11}$to 10^{9} Jones, and fast photoresponse time of ~ 80 ns.

2:25 PM
9-3 World-first 1 µm-pixelated 72K large area active matrix spatial light modulator on glass for digital holographic display, J. H. Choi, J.-E . Pi, J.-H. Yang, Y.-H. Kim, G. H. Kim, H.-O. Kim, W.-J. Lee, J. Y. Kim, J. Kim, M. Kim*, K. K. Kim*, H. K. Lee**, C.-S . Hwang. Electronics and Telecommunications Research Institute (ETRI),* LX Semicon, ** MVTech

A world-first 1 µm-pixelated 72K ultra-high-resolution SLM on glass (SLMoG) for digital holographic display was developed. It was confirmed that the SLMoG could serve 2π phase modulation. Based on 3.05-inch diagonal large-sized display, 30mm-sized holographic image could be fully observed within 30° of viewing angle without any additional optical elements.

2:50 PM
9-4 Monolithic 3D µ-LED displays through BEOL integration of large-area MoS2 TFT matrix, W. Meng, F. Xu, X. Shen*, T. Tao, Zhihao Yu**,K. Wen***, J. Wang***, F. Qin****, X# Tu, J. Ning*, D. Wang*, Y. Zheng, B. Liu, R. Zhang+, Y. Shi, X. Wang, Nanjing University,*Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials, **Xidian University, ***Nanjing University of Posts and Telecommunications, ****Nanjing Tech University, #Tianma Microelectronics Co., LTD, ## Nanjing University, Nanjing + Xiamen University, Xiamen, ++Tan Kah Kee Innovation Laboratory

Using low-temperature BEOL process, we realize M3D ultra-high-resolution µ-LED displays driven by CVD-MoS₂ TFTs with maximum mobility of 73 cm^2 $V^{-1}s^{-1}$, drive current >200 µA/µm, and

excellent uniformity. The 1T-1D cell delivers low voltage and high luminance of 7.1×10^7 cd/m^2. We further demonstrate prototypical 32×32 AM displays at 1270 PPI.

3:15 PM Coffee Break

Session 10: Memory Technology - Charge-based Memories
Tuesday, December 14, 9:00 AM
Grand Ballroom A
Co-Chairs: Hsiang-Lan Lung, Macronix
John Paul Strachan, Forschungszentrum Jülich & RWTH Aachen

9:05 AM
10-1 Highly Reliable Cell Characteristics with CSOB(Channel-hole Sidewall ONO Butting) Scheme for 7th Generation 3D-NAND, J-K Kang, J. Lee, Y. Yim, S. Park, H. S. Kim, E. S. Cho, T. Kim, J. Hoon Lee, J. Kim, R. Lee, J. Lim, S. Hur, S. Jin Ahn, J. Song, Samsung Electronics Co.

Architecture change from BCS scheme to CSOB scheme for the 7th-generation 3D-NAND flash memory is discussed, which has been driven to adopt COP scheme. Device considerations in the 7th-generation 3D NAND are reviewed and solutions are suggested that lead to the world smallest unit cell volume in flash memory.

9:30 AM
10-2 Understanding the kinetics of Metal Induced Lateral Crystallization process to enhance the poly-Si channel quality and current conduction in 3-D NAND memory, S. Ramesh, S. Vadakupudhu Palayam, A. Ajaykumar, K. Opsomer, J. Bastos, L.-Å. Ragnarsson, L. Breuil, A. Arreghini, L. Wouters, V. Spampinato, P. Favia, A. Nalin Mehta, P. Carolan, L. Nyns, K. Katcko, J. Stiers, G. Van den bosch, M. Rosmeulen, IMEC

The kinetics of Ni-metal induced lateral crystallization (MILC) in a Si channel has been thoroughly investigated. The impact of thermal treatments on the quality of Si channel formed are reported. We show that it is possible to achieve enhanced channel control and conduction with a controlled MILC process.

9:55 AM
10-3 Investigation of Methods That Greatly Improve 3D NOR Flash to Either Gain Superb Retention or Become DRAM-like with High Endurance (>1G cycling) and High Write-bandwidth (>4Gb/s), H-T Lue, T-H Hsu, C. (Roger) Lo, T-H Yeh, K-C Wang, and C-Y Lu, Macronix International Co., Ltd.

We propose three efficient methods to improve the novel 3D NOR device with micro wall heater. (1) 3DIC design method with additional heater controller chip; (2) Sample S1 with thicker BE-Tox and heater-assisted "refill" programming method to improve retention; (3) Sample S2 with heater-assisted endurance (1G) and high write bandwidth.

10:20 AM
10-4 Dielectric Confinement Impact on Electrical Performance of Highly Scaled Saddle-Fin Cell Transistor for High Density DRAM, D. Oh, S. Lee, S. Kim, J. Moon, S. Lee, S. Park, J. Kim, SK Hynix

For the first time, we investigated the impact of dielectric confinement effect on the resistance of saddle-fin transistor using TCAD and experiments. This study shows the need for accurate resistance prediction and how to mitigate this effect when introducing low-k materials to ensure a sensing margin in DRAM cell design

10:45 AM Coffee Break

11:10 AM

10-5 Novel Vertical Channel-All-Around(CAA) IGZO FETs for 2T0C DRAM with High Density beyond 4F* by Monolithic Stacking, X. Duan, K. Huang,*, J. Feng*, J. Niu, H. Qin*, S. Yin*, G. Jiao*, D. Leonelli*, X. Zhao*, W. Jing*, Z. Wang*, Q. Chen, X. Chuai, C. Lu, W. Wang, G. Yang, Di Geng*, L. Li*, M. Liu Institute of Microelectronics of the Chinese Academy of Sciences, *Huawei Technologies Co., LTD.

First demonstration of Vertical Channel-all-around(CAA) IGZO FETs for high-density 4F2 and long retention 2T0C DRAM application. The experimental test of the CAA IGZO 2T0C-bit-cell shows the retention time can be as long as 300s, making it is a potential candidate for 2T0C DRAM with ultralow refresh frequency and energy consumption.

11:35 AM

10-6 Tailoring IGZO-TFT architecture for capacitorless DRAM, demonstrating > 1E3s retention, >1E11 cycles endurance and Lg scalability down to 14nm, A. Belmonte, H. Oh, S. Subhechha, N. Rassoul, H. Hody, H. Dekkers, R. Delhougne, L. Ricotti, K. Banerjee, A. Chasin, M. J. van Setten, H. Puliyalil, M. Pak, L. Teugels, D. Tsvetanova, K. Vandersmissen, S. Kundu, J. Heijlen, D. Batuk. J. Geypen, L. Goux, G. S. Kar, imec

We demonstrate a fully 300-mm BEOL-compatible IGZO-based capacitorless DRAM cell with >1E3s retention and >1E11 endurance lifetime. We evaluate the impact of the IGZO-TFT architecture on the memory performance, and we demonstrate >100s retention down to Lg=17nm. We also demonstrate capacitorless DRAM cell functionality with conformal IGZO deposition.

Session 11: Microwave, Millimeter Wave and Analog - III-V technologies and their Applications to THz/6G

Tuesday, December 14, 9:00 AM
Continental Ballrooms 1-3
Co-Chairs: Mitsuru Takenaka, University of Tokyo
Qiangfei Xia, University of Massachusetts

9:05 AM

11-1 Advanced Scaling of 300mm Enhancement Mode High-K Gallium Nitride-on-Si(111) Transistor and 3D Layer Transfer GaN-Silicon Finfet CMOS Integration, H. W. Then, M. Radosavljevic, P. Koirala, N. Thomas, N. Nair, I. Ban, T. Talukdar, P. Nordeen, S. Ghosh, S. Bader, T. Hoff, T. Michaelos, R. Nahm, M. Beumer, N. Desai, P. Wallace, V. Hadagali, H.Vora,A. Oni, X. Weng, K. Joshi, I. Meric, C. Nieva, S. Rami, P. Fischer, Intel Corporation

We demonstrate scaling of enhancement-mode high-k GaN-on-300mm-Si(111) transistor and achieve for GaN-on-Si: record f_T=300GHz/f_{MAX}=400GHz/G_M>2100µS/µm with industry-thinnest T_{OXE}=14.8Å; record V_{DS}=65V for L_G=30nm; record-low ON-gate-drive V_{Gon}=1.8V and I_{OFF}=25pA/µm (V_D=30V)($V_{G,}$=0V); industry's first Cu backend-interconnect; $V_{TH-}1\sigma$-variation=38mV on 300mm-wafer. We demonstrate a 3D-layer transfer GaN/Si-CMOS inverter featuring GaN-NMOS-finfet with the narrowest GaN-fin ever been demonstrated.

9:30 AM

11-2 Monolithic 3D Integrated InGaAs HEMTs on Si for Next-Generation Communication: Record fMAX and Relaxed Self-Heating of Top Devices by a Novel M3D Structure, J. Jeong, S. Kwang Kim, J. Kim*, D-M Geum, S. Kim*, KAIST, Korea Advanced Nano Fab Center (KANC)

We have demonstrated M3D InGaAs HEMT on Si for next-generation communication. InGaAs top HEMTs showed f_T=301GHz and f_{MAX}=716GHz. The f_{MAX} value is the highest ever reported in M3D RF transistors. Furthermore, we experimentally demonstrated that the self-heating of top devices can be relaxed by a novel M3D structure.

9:55 AM

11-3 InxGa1-xAs quantum-well high-electron-mobility transistors with a record combination of fT and fmax: From the mobility relevant to ballistic transport regimes, Seung-Won Yun, Hyeon-Bhin Jo, Ji-Hoon Yoo, Wan-Soo Park, Hyeon-Seok Jeong, Su-Min Choi, Hyo-Jin Kim, Sethu George, Ji-Min Beak, In-Guen Lee, Tae-Woo Kim*, Sang-Kuk Kim**, Jacob Yun**, Ted Kim**, Takuya Tsutsumi***, Hiroki Sugiyama***, Hideaki Matsuzaki***, and *Dae-Hyun Kim, Kyungpook National University (KNU), * University of Ulsan (UoU), **QSI, *** NTT Corporation

We report In_xGa_{1-x} As quantum-well high-electron mobility transistors with a superior DC and high-frequency characteristics. We fabricated with various epi-layer structures,10um~sub-30nm. We modeled experimental figures of merit,correlated from DC FOMs to high-frequency FOMs. Our approach explained both DC&high-frequency characteristics. The fabricated composite-$In_{0.8}$ Ga $_{0.2}$. As HEMT with L_g=30nm represented the best balance of f_T&f_{max}.

10:20 AM Coffee Break

10:45 AM

11-4 InP/GaAsSb Double Heterojunction Bipolar Transistor Technology with f_{MAX} = 1.2 THz, A.M. Arabhavi, F. Ciabattini, S. Hamzeloui, R. Flückiger, T. Popovic, D. Han, D. Marti, G. Bonomo, R. Chaudhary, O. Ostinelli, and C.R. Bolognesi. Millimeter-Wave Electronics Group, ETH-Zurich

We report a new InP/GaAsSb DHBT emitter architecture with a record f_{MAX} = 1.2 THz and BV_{CEO} = 5.4V. The resulting $BV_{CEO} \times f_{MAX}$ = 6.48 THz-V is unparalleled, in any technology. Also, f_{MAX} >1THz is achieved with a 9.4μm emitter length and an area of 1.645μm^2, a clear breakthrough in THz transistor scalability.

11:10 AM

11-5 Enabling Device Technologies for Photonics-assisted Millimeter and Terahertz Wave Applications (Invited), T. Nagatsuma, M. Fujita, L. Yi, Osaka University, Japan

This paper presents device technologies for practical combination of telecom-based photonics and electronic devices in millimeter-wave and terahertz systems, which include high-speed wireless communications and sensing applications. Enabling semiconductor devices and their integrated modules are also highlighted.

Session 12: Memory Technology - NOR Flash and RRAM for In-Memory Computing

Tuesday, December 14, 9:00AM
Continental Ballroom 4
Co-Chairs: Subhali Subhechha, imec
Qiangfei Xia, University of Massachusetts

9:05 AM

12-1 Design-Technology Co-Optimizations (DTCO) for General-Purpose In-Memory Computation Based on 55nm NOR Flash Technology, Y. Feng, B. Chen*, J. Liu**, Z. Sun, H. Hu**, J. Zhang***, X. Zhan, J. Chen, *Shandong University, * Zhejiang University, **Institute of Microelectronics of Chinese Academy of Sciences, ***Neumem Co., Ltd

Based on 55nm NOR flash technology, a general-purpose in-memory-computation architecture is proposed. By using DTCO approach, a partial differential equation solver is constructed with the 32-bit floating point calculation ability. Memory cells (4bit/cell) work at the quasi-saturation region, and the hot hole injection (HHI) is utilized to tune cell individually.

9:30 AM
12-2 RRAM-enabled AI Accelerator Architecture (Invited), X. Wang, Y. Wu, and W. D. Lu, University of Michigan

Resistive random-access memory (RRAM) offers high-density non-volatile storage and potential for efficient in-memory computing. RRAM-enabled accelerators can solve the von Neumann bottleneck and meet the computing needs of applications such as Artificial Intelligence (AI). In this paper, we discuss progress in RRAM-based accelerators for AI inference, training and arithmetic applications.

9:55:00 AM
12-3 Improved On-chip Training Efficiency at Elevated Temperature and Excellent Inference Accuracy with Retention (> 108 s) of Pr0.7Ca0.3MnO3-x ECRAM Synapse Device for Hardware Neural Network, C. Lee, M. Kwak, W. Choi, S. Kim, H. Hwang, Pohang University of Science and Technology (POSTECH)

We demonstrated $Pr_{0.7}Ca_{0.3}MnO_{3-x}$ (PCMO) based Electro-Chemical Random-Access Memory (ECRAM) to achieve excellent on-chip training efficiency and inference accuracy. Accelerated oxygen ion migration through electrolyte at elevated temperature provides linearity and symmetry of weight update, multi-level conductance states as well as excellent retention (> 10^8 s) characteristic.

10:20 AM
12-4 Implementation of Discrete Fourier Transform using RRAM Arrays with Quasi-Analog Mapping for High-Fidelity Medical Image Reconstruction, Han Zhao, Zhengwu Liu, Jianshi Tang*, Bin Gao, Ying Zhou, Peng Yao, Yue Xi, He Qian, Huaqiang Wu*
BNRist, *Tsinghua University, Beijing, China;

We report the first experimental implementation of discrete Fourier transform (DFT) on RRAM arrays. We developed a novel RRAM conductance mapping strategy, quasi-analog mapping, to realize high-precision mapping. High-fidelity medical image reconstruction was demonstrated, achieving a software-comparable PSNR of 26.1 dB. RRAM-enabled DFT achieved ~128× higher energy efficiency than CPU.

10:45 AM Coffee Break

11:10 AM
12-5 A 128kb Stochastic Computing Chip based on RRAM Flicker Noise with High Noise Density and Nearly Zero Autocorrelation on *8-nm CMOS Platform, Tiancheng Gong, Qiao Hu, Danian Dong, Haijun Jiang*, Jianguo Yang*,*, Xiaoxin Xu*, Xiaoming Chen**, Qing Luo, Qi Liu***, Steve S. Chung****, Hangbing Lyu, Ming Liu, Institute of Microelectronics of Chinese Academy of Sciences, *Zhejiang Lab, **Institute of Computing Technology of Chinese Academy of Sciences,
***Fudan University, China; ****National Yang Ming Chiao Tung University

In this work, a 128kb RRAM flicker noise based Stochastic Computing (SC) chip is demonstrated on 28-nm HKMG CMOS platform for the first time. Flicker noise in RRAM is selected as the entropy source owing to the higher noise density compared with the conventional logic devices.

11:35 AM

12-6 Forming-free and Annealing-free V/VOx/HfWOx/Pt Device Exhibiting Reconfigurable Threshold and Resistive switching with high speed (<30ns) and high endurance (>10^{12}/>10^{10}), Y. Fu, Y. Zhou, X. Huang, B. Gao*, Y. He, Y. Li, Y. Chai** and X. Miao*, Huazhong University of Science and Technology, * Tsinghua University, ** The Hong Kong Polytechnic University

Fully reconfigurable switching between selector and RRAM is demonstrated in one V/VO_x/$HfWO_x$/Pt device while with no electroforming or high-temperature annealing processes involved in fabrication. The devices with ultra-high endurance (>10^{12} for selector, >10^{10} for RRAM) and high operation speed (<30ns) are further utilized to emulate solid neurons and synapses.

Session 13: Advanced Logic Technology - Platform Technologies and Advanced Gate Stack
Tuesday, December 14, 9:00 AM
Continental Ballroom 5
Co-Chairs: Rinus Lee, TEL Technology Center, America, LLC
/Dechao Guo, IBM

9:05 AM

13-1 18nm FDSOI Technology Platform embedding PCM & Innovative Continuous-Active Construct Enhancing Performance for Leading-Edge MCU Applications, D. Min, J. Park, O. Weber*, A. Villaret*, E. Vandenbossche*, F. Arnaud*, E. Bernard*, S. Elghouli*, C. Boccaccio*, L. Favennec*, R. Gonella*, J. Galvier*, J. Yun, J. Park, M. Lee, P. Yoon, I. Lee, H. Seo, H. Choi, C. Oh, J. Kang, S. Park, H. Lee, Y. Choi, I. Kim, J. Jo, Y. Park, J. Park, Y. Lee, J. Jung, J. Lee, H. Jang, J. Kang, J. Kwon, J. Kim, S. Maeda and Y. Hong, Samsung Electronics Co., Ltd., *STMicroelectronics

For the first time in the industry, 18nm FDSOI technology platform meeting the performance target for next MCU is presented showing good yield in 64Mb SRAM array including ultra low leakage bitcell with Iret < 1pA, passed 500hrs HTOL for all SRAM bitcells, passed WLR for TGO and co-integrated ePCM.

9:30 AM

13-2 Design Technology Co-Optimization for Cold CMOS Benefits in Advanced Technologies (Invited), H-L Chiang, J-J Wu, C-H Chou, Y-F Hsiao, Y-C Chen, L. Liu, J-F Wang, T-C Chen, P-JJun Liao, J. Cai, X. Bao, A. Cheng, M-F Chang, Taiwan Semiconductor Manufacturing Company

Cold CMOS is a feasible technology to obtain HPC or power reduction by offering a reliable way for a steeper subthreshold slope. In this paper, we focus on DTCO and PPA analyses for memory cells and their peripherals to maximize the PPA benefits from Cold CMOS at the system level.

9:55 AM

13-3 High Performance 4nm FinFET Platform (4LPE) with Novel Advanced Transistor Level DTCO for Dual-CPP/HP-HD Standard Cells, Y. Yasuda-Masuoka, J. Jeong, K. Son, S. Lee, S. Park, Y. Lee, J. Y. Kim, J. Lee, M. Cho, S. Lee, S. Hong, H. Hong, Y. Jung, C. Yoon, Y. Ko, K. Jung, T. Myung, J. M. Youn and G. Jeong, Samsung Electronics

Leading edge High performance 4nm FinFET Platform (4LPE) is demonstrated, featuring a novel Transistor-level-DTCO in MOL/BEOL and careful process-optimization, which enables dual-CPP/HP-HD standard cell with Gate-contact-over-RX scheme. Compared to 5nm(5LPE), Performance+7~10%/Power-12% gain are successfully obtained, as well as a flat layout dependence. 4LPE enhancement is accomplished by design-manufacturing favorable approaches.

10:20 AM Coffee Break

10:45 AM

13-4 Al-doped and Deposition Temperature-engineered HfO2 Near Morphotropic Phase Boundary with Record Dielectric Permittivity (~68), J. Zhou, Z. Zhou, L. Jiao, X. Wang, Y. Kang, H. Wang, K. Han, Z. Zheng, and X. Gong, National University of Singapore (NUS)

For the first time, we demonstrate Al-doped HfO_2 films near morphotropic-phase-boundary with the highest permittivity (~68) among all the reported works using a novel technique of deposition temperature engineering, showing many good performance, including, J_{leak} @ 1 V, lifetime, and endurance characteristics. Such films open up opportunities for future nanoelectronic devices.

11:10 AM

13-5 Dipole-First Gate Stack as a Scalable and Thermal Budget Flexible Multi-Vt Solution for Nanosheet/CFET Devices, H. Arimura, L.-Å. Ragnarsson, Y. Oniki, J. Franco, A. Vandooren, S. Brus, A. Leonhardt*, P. Sippola*, T. Ivanova*, G. Alessio Verni*, R.-J. Chang**, Q. Xie**, M. Givens**, J. Mitard, S. Biesemans, E. Dentoni Litta, and N. Horiguchi, imec, *ASM Microchemistry, **ASM

We present dipole-first multi-Vt gate stack as a thermal budget flexible and wide-/fine-tunable multi-Vt solution applicable to 3D-integrated nanosheet/CFET devices. Key results include the proof-of-concept of zero-thickness dipole-first, limited mobility degradation with LaO dipole-first, and an improved fine-tunability and gate stack properties using a novel ALD n-type shifter.

11:35 AM

13-6 Demonstration of Low EOT Gate Stack and Record Transconductance on Lg=90 nm nFETs Using 1.8 nm Ferroic HfO2-ZrO2 Superlattice, W. Li, L. C. Wang*, S. S. Cheema*, N. Shanker, J. H. Park, Y. H. Liao, S. L. Hsu, C. H. Hsu, S. Volkman, U. Sikder, A. J. Tan, J. H. Bae, C. Hu, S. Salahuddin. University of California, *University of California

Enhanced gate capacitance and associated low EOT is demonstrated in a 1.8-nm ferroic HfO_2ZrO_2 superlattice gate stack on n-MOSFETs without any IL scavenging, resulting in record-high intrinsic transconductance of 1.5 mS/μm and a 14% I_{on} increase in 90-nm transistors. The capacitance enhancements show no dispersion up to 25 GHz.

Session 14: Emerging Device and Compute Technology-Focus Session- Device Technology for Quantum Computing

Tuesday, December 14, 9:00 AM
Continental Ballroom 6
Co-Chairs: Woon-Bin Song, Samsung Electronics Co.
Kirsten Moselund, IBM Zurich

9:05 AM

14-1 Si MOS and Si/SiGe quantum well spin qubit platforms for scalable quantum computing (Invited), R. Pillarisetty, T.F. Watson, B. Mueller, E. Henry, H.C. George, S. Bojarski, L. Lampert, F. Luthi, R. Kotlyar, O. Zietz, S. Neyens, F. Borjans, R. Caudillo, D. Michalak, R. Nahm, J. Park, M. Ramsey, J. Roberts, S. Schaal, G. Zheng, T. Krähenmann*, M. Lodari*, A.M.J. Zwerver*, M. Veldhorst*, G. Scappucci*, L.M.K. Vandersypen*, J.S. Clarke, Intel Corporation, *QuTech and Kavli Institute of Nanoscience, TU Delft

In this article we discuss the engineering and device-physics of both Si MOS and SiGe/Si quantum well based spin qubit platforms, which are fabricated in a full 300mm process compatible with high-volume

CMOS manufacturing. Key electrical metrics for both quantum dot and qubit performance will be compared across both architectures.

9:30 AM
14-2 Material and integration challenges to enable large scale Si quantum computing, (Invited) M Vinet, T. Bédécarrats, B. Cardoso Paz*, B. Martinez**, E. Chanrion*, E. Catapano, L Contamin, V Mazzocchi, H. Niebojewski, B. Bertrand, N. Rambal, C Thomas, J Charbonnier, PA Mortemousque, J.-M. Hartmann, E. Nowak, M. Cassé, M. Urdampilleta*, Y.-M. Niquet**, F Perruchot, S. De Franceschi**, T. Meunier*, CEA Leti, *CNRS Neel Institute, **Univeristy Grenoble Alpes

Si spin qubits are very promising to enable large scale quantum computing as they are fast, of high quality and small. Though they are still lagging behind in terms of number of qubits. Indeed there are material and integration challenges that have to be tackled before fully expressing their potential.

9:55 AM
14-3 High-fidelity two and three spin operations in Si with triple quantum dots (Invited), S. Tarucha

We use Si/SiGe triple quantum dots to operate two and three spin qubits with high fidelities. For the two qubit we faster the single qubit and exchange control to achieve the fidelity > 99 %. For the three qubits we control two exchange couplings to generate a three-spin entangled state.

10:20 AM
14-4 Silicon-based Quantum Computing: High-density, High-temperature Qubits (Invited), A. S. Dzurak. UNSW, School of Electrical Engineering, Sydney, Australia.

We review prospects for full-scale quantum computing (QC) based on silicon quantum dots. These are attractive due to the long spin coherence times available in silicon and its compatibility with CMOS manufacturing. We discuss qubit fidelities, processor architectures and issues for scaling, including wiring challenges, quantum interconnects and operation temperature.

10:45 AM Coffee Break

11:10 AM
14-5 3D Integration Technology for Quantum Computer based on Diamond Spin Qubits (Invited), R. Ishihara*, J. Hermias*, S. Yu*, K. Y. Yu*, Y. Li*, S. Nur*, T. Iwai**, T. Miyatake**, K. Kawaguchi**, Y. Doi** , S. Sato**. *Delft University of Technology and Kavli Institute of Nanoscience Delft, **Fujitsu Limited, Quantum Computing Research Center

Quantum computer chips based **on spin** qubits in diamond uses modules that are entangled with on-chip optical links. 3D integration is the key enabling technology for large-scale integration of the diamond spin qubits with photonic circuits and CMOS electronics. We will review challenges and discuss future outlook of the technology.

11:35 AM
14-6 Quantum Photonics with SnV Centers in Diamond (Invited), S. Aghaeimeibodi, J. Vuckovic. E. L. Ginzton Laboratory, Stanford University, Stanford, CA 94305, USA,

We discuss our recent efforts on realizing a quantum photonic platform for diamond color centers. We demonstrate integration of tin vacancy spin qubits in diamond to optical waveguides, cavities, and nanopillars. We show that SnV centers created using shallow ion implantation and overgrowth maintain their quality when placed in nanostructures.

12:00 PM
14-7 Packaging and integration challenges in a superconducting-qubit-based quantum computer (Invited), M. Giustina, Google QuantumAI

A fault-tolerant error-corrected quantum computer based on superconducting microwave qubits places unique demands on devices, packaging, and system integration. We present an overview of some near-term system challenges in scaling up device IO, as well as some performance metrics for relevant component technologies.

Session 15: Modeling and Simulation - Modeling and Simulation – Ferroelectric Microwave, Millimeter Wave and Analogerials, Devices and Applications
Tuesday, December 14, 9:00 AM
Continental Ballrooms 7-9
Co-Chairs: Anne S. Verhulst, imec
Joddy Wang, Synopsys

9:05 AM
15-1 Surface-Functionalized Hafnia with Bespoke Ferroelectric Properties for Memory and Logic Applications, D.-H. Choe, H. Bae, H. Lee, Y. Lee, T. Moon, S. G. Nam, S. Jo, H. J. Lee, E. Lee, J. Heo. Materials Research Center, Samsung Advanced Institute of Technology (SAIT), Suwon, Gyeonggi-do, 16678, Korea

By developing a novel optimization algorithm, we, for the first time, model surface-functionalized $HfO_2$from first-principles and demonstrate that their ferroelectric properties can be widely controlled via surface treatment. This work provides practical guidelines for the rational design and fabrication of advanced memory and logic devices made of ferroelectric hafnia.

9:30 AM
15-2 Variation and Stochasticity in Polycrystalline HZO based MFIM: Grain-Growth Coupled 3D Phase Field Model based Analysis, R. Koduru, A. K. Saha, M. Si, X. Lyu, P.D. Ye, S. K. Gupta. Department of Electrical and Computer Engineering, Purdue University, United States

We present grain growth coupled 3D phase field simulation framework for Ferroelectric $Hf_{1-x}Zr_xO_2$(HZO) based MFIM stack that captures the effects of polycrystallinity. We study the multi domain polarization switching in polycrystalline HZO and analyze the sample-to-sample variations and cycle-to-cycle stochasticity and their dependance on Ferroelectric thickness

9:55 AM
15-3 On the Channel Percolation in Ferroelectric FET Towards Proper Analog States Engineering, K. Ni, S. Thomann*, O. Prakash**, Z. Zhao, S. Deng, and H. Amrouch*. Rochester Institute of Technology, *University of Stuttgart, **Karlsruhe Institute of Technology

The channel percolation in FeFET is investigated through extensive theoretical investigations. It is found that channel percolation is not universally present in FeFETs. The conventional resistor network model, when applied to predict percolation, neglects the critical carrier diffusion in the channel, thus missing the neighbor interactions.

10:20 AM Coffee Break

10:45 AM

15-4 NLS based Modeling and Characterization of Switching Dynamics for Antiferroelectric/Ferroelectric Hafnium Zirconium Oxides, Y-C Chen, K-Y Hsiang,*, Y-T Tang**, M-H Lee* and P. Su, National Yang Ming Chiao Tung University, * National Taiwan Normal University **Taiwan Semiconductor Research Institute, National Central University

We have conducted an NLS-based Monte-Carlo modeling and characterization for antiferroelectric/ferroelectric $Hf_{1-x}Zr_xO_2$. With the coexistence of orthorhombic-phase and tetragonal-phase grains and the consideration of back-switching field, our model can describe the switching dynamics and frequency response of AFE/FE. Our model can be beneficial to future memory applications and neuromorphic computing.

11:10 AM
15-5 Predictive Modeling of Ferroelectric Tunnel Junctions for Memory and Analog Weight Cell Applications, Y. Xiao, S. Deng*, Z. Zhao*, V. Narayanan, and K. Ni*. Pennsylvania State University, *Rochester Institute of Technology

A predictive metal-ferroelectric-insulator semiconductor(MFIS) FTJ model is developed by incorporating a polarization-switching module and a multi-band tunneling module. The model can predict the asymmetric polarization states induce by positive/negative write pulses in MFIS FTJ due to absence of minority carriers and enable write aware design space exploration.

11:35 AM
15-6 Modelling of vertical and ferroelectric junctionless technology for efficient 3D neural network compute cube dedicated to embedded artificial intelligence (Invited), C. Maneux, C. Mukherjee, M. Deng, M. Dubourg, L. Reveil, G. Bordea, A. Lecestre[2], G. Larrieu*, J. Trommer**, E.T. Breyer**, S. Slesazeck**, T. Mikolajick**, O. Baumgartner***, M. Karner***, D. Pirker***, Z. Stanojevic***, David A. Atienza****, A. Levisse****, G. Ansaloni****, A. Poittevin#, A. Bosio#, D. Deleruyelle#, C. Marchand#, I. O'Connor#, IMS, University of Bordeaux, UMR CNRS, *LAAS-CNRS, Université de Toulouse, **NaMLab gGmbH, ***Global TCAD Solutions GmbH, ****EPFL, #INL, University of Lyon

This paper presents the set of simulation means used to develop the N^2C^2 concept (neural network compute cube) based on vertical transistor technology platform. Compact modeling, TCAD and EM simulation are leveraged through Design-Technology Co-Optimization to achieve 3D circuit architectures. System-Technology Co-Optimization implications on 3D NN system architecture are explored.

Session 16: Sensors, Mems, and Bioelectronics - Biomedical Devices
Tuesday, December 14, 9:00 AM
Imperial Ballroom A
Co-Chairs: Wen Li, Michigan State University
Gaelle Lissorgues, University Gustave EIFFEL

9:05 AM
16-1 Biohybrid Nanostructuring (Invited), W. van der Wijngaart, KTH Royal Institute of Technology, Stockholm Sweden

Life is hierarchically structured down to the nanoscale and humankind has been engineering on the same scale. I here show some recent examples where we combine the merits of both worlds, synthesizing biohybrid constructs of synthetic and biologic matter with new functionalities on the sub-micrometre scale.

9:30 AM

16-2 Double-Gate Si Nanowire FET Sensor Arrays For Label-Free C-Reactive Protein detection enabled by antibodies fragments and pseudo-super-Nernstian back-gate operation, L. Capua, Y. Sprunger**, H. Elettro**, A. Grammoustianou**, R. Midahuen***, T. Ernst***, S. Barraud***, R. Gill** and A.M. Ionescu, EPFL, **Xsensio SA, ***CEA, LETI, MINATEC Campus and Univ. Grenoble Alpes

We report first CMOS-compatible CRP differential-mode sensor based on double-gate Si nanowires FET arrays, characterized by super-Nernstian sensitivity of 3.17V/pH in back-gate configuration. The BG configuration is exploited to detect CRP on the physiological range between 0.6μg/ml - 100μg/ml, with a sensitivity of 1.2nA/decade, and low drift over time (<20pA/decade).

9:55 AM

16-3 RF Powered Flexible Printed Ion-sensitive Organic Field Effect Transistor Chip with Design-to-manufacturing Automation for Mobile Bio-sensing, B. Ouyang, Y. Song, H. Zhou, W.Cai, Y.Si, X. Yin, S. Chen, B. Huang, X. Guo. Shanghai Jiao Tong University, China.

Ion-sensitive organic field-effect transistor (ISOFET) is built based on maskless printing processes with automatic design-to-manufacturing. The printed OFETs exhibit excellent low voltage operation behaviors and bias stability. A battery-less flexible hybrid integration system was constructed by integrating the ISOFET chip with a 13.56 MHz RFID chip for a mobile

10:20 AM Coffee Break

10:45 AM

16-4 High Stretchability Ultralow-Power All-Printed Thin Film Transistor Amplifier on Strip-Helix-Fiber, C. Jiang*, C. P. Tsangarides, X. Cheng, L. Ding, H. Ma**, A. Nathan***, University of Cambridge, * Tsinghua University, **SIBET, Chinese Academy of Sciences, ***Darwin College, Cambridge University

A universal strip-helix architecture for integrating thin-film transistors and amplification circuits for high stretchability is presented, allowing devices/circuits to be weaved/knitted into smart textiles. The subthreshold organic device/circuit demonstrates high stretchability under high strain of 50%, with ultralow power (681pW) and high gain (214V/V), compelling for real-time wearable electrophysiological monitoring.

11:10 AM

16-5 High Throughput Neuromorphic Brain Interface with CuOx Resistive Crossbars for Real-time Spike Sorting, Y. Shi, A. Ananthakrishnan, S. Oh, X. Liu, G. Hota, G. Cauwenberghs, D. Kuzum, University of California San Diego

We present a real-time spike sorting processor that performs in-memory spike segregation using high-density BEOL-integrable CuOx resistive crossbars. Our hardware implementation could sort spikes from in vivo extracellular recordings with high accuracy, and promises substantial performance gains in area, power, and latency compared with state-of-the-art FPGA and microcontroller implementations.

11:35 AM

16-6 Wearable Pulse Wave Sensor and Interface for Real-Time Dynamic Blood Pressure Monitoring, H. Li, A. Li, Z. Zhou, B. Jiang, Q. Yang, X. Liu*, and K. Wang*, Sun Yat-sen University, *Shenzhen Chipwey Innovation Technologies Co., Ltd.

Real-time pulse wave that contains ample information on blood pressure (BP) is crucial to cardiovascular monitoring. In this work, we introduce a flexible piezoelectric array sensor and a thin-film transistor-based

sensor interface aiming for efficient acquisition of redundant pulse waveforms sufficient for extracting BPs using deep learning method.

Career Luncheon
Tuesday, December 14, 12:20 PM
Grand Ballroom B
Speakers: Sophie Vandebroek, Strategic Vision Ventures LLC
Deji Akinwande, University of Texas

In this IEDM Career Luncheon, the IEDM Executive Committee invites student conference attendees, aspiring professionals, and the IEDM community at-large to join two invited veterans in a casual, buffet lunch setting to discuss topics related to their careers and their experience in the semiconductor community. Our distinguished speakers this year, Sophie Vandebroek of Strategic Vision Ventures LLC and Deji Akinwande of the University of Texas, will share their perspectives on the future of semiconductor technology. We encourage the audience to attend this luncheon and engage with the distinguished speakers as they seek answers to their career development questions and the overall evolution of the semiconductor industry.

Session 17: Memory Technology - Emerging Non-Volatile Memories
Tuesday, December 14, 2:15 PM
Grand Ballroom A
Co-Chairs: Sou-Chi Chang, Intel
Xinyu Bao, TSMC

2:20 PM
17-1 Lifelong Learning with Monolithic 3D Ferroelectric Ternary Content-Addressable Memory, S. Dutta, A. Khanna, H. Ye, M.M. Sharifi, A. Kazemi, M. San Jose, K.A. Aabrar, J.G. Mir, M. Niemer, X.S. Huand, S. Datta, University of Notre Dame

We present array-level demonstration of few-shot learning using a first time fabricated monolithic 3D TCAM using BEOL FeFETs. We experimentally demonstrate write voltage of 1.6V,20ns write latency for BEOL FeFETs , in situ computation of Hamming distance between a 20-bit search vector and stored vectors, and high write endurance> 10^{10} cycles.

2:45 PM
17-2 High Performance and Self-rectifying Hafnia-based Ferroelectric Tunnel Junction for Neuromorphic Computing and TCAM Applications, Y. Goh, J. Hwang, M. Kim, M. Jung, S. Lim*, S-O Jung*, S. Jeon, Korea Advanced Institute of Science and Technology (KAIST), * Yonsei University

Self-rectifying hafnia-based ferroelectric tunnel junction with high performance has been proposed using stress engineering, diffusion barrier technology and imprint field effect for neuromorphic computing and TCAM applications. The proposed FTJ shows a giant TER value (~100), high rectifying ratio (~1000), excellent endurance properties (>10^8) and low power consumption (~0.185fJ).

3:10 PM
17-3 A Novel High-Endurance FeFET Memory Device Based on ZrO2 Anti-Ferroelectric and IGZO Channel, Z. Liang, K. Tang, J. Dong, Q. Li*, Y. Zhou, R. Zhu, Y. Wu, D. Han, and R. Huang, Peking University, *Huazhong University of Science and Technology

A novel FeFET based on ZrO2 anti-ferroelectric and IGZO channel is fabricated for the first time. We report the high- performance with high endurance up to 109 cycles, good retention of > 10 years, and low working voltage of 2 V, which fit the device for future embedded memory applications.

3:35 PM Coffee Break

4:00 PM

17-4 High-Peformance BEOL-Compatible Atomic-Layer-Deposited In2O3 Fe-FETs Enabled by Channel Length Scaling down to 7 nm: Achieving Performance Enhancement with Large Memory Window of 2.2 V, Long Retention > 10 years and High Endurance > 10^8 Cycles, Z. Lin, M. Si, Y.-C. Luo*, X. Lyu, A. Charnas, Z. Chen, Z. Yu*, W. Tsai**, P. C. McIntyre**, R. Kanjolia***, M. Moinpour***, S. Yu*, P. D. Ye*, Purdue University, *Georgia Institute of Technology, **Stanford University, ***EMD Electronics

In this work, we report ultra-scaled ALD In2O3Fe-FETs with channel length down to 7 nm as back-end-of-line compatible non-volatile memory devices, achieving memory performance enhancement with a memory window of 2.2 V, retention over 10 years, and endurance over 10⁸ cycles, demonstrating the key advantage of scaling in Fe-FETs.

4:25 PM

17-5 First demonstration of three terminal MRAM devices with immunity to magnetic fields and 10 ns field free switching by electrical manipulation of exchange bias, D.Q. Zhu, Z.X. Guo, A. Du, D.R. Xiong, R. Xiao, W.L. Cai, K.W. Shi, S.Z. Peng, K.H. Cao, S.Y. Lu, D.P. Zhu, G.F. Wang**, H.X. Liu**, Q.W. Leng, and W.S. Zhao**, Beihang University, *Truth Memory Tech Corporation

For the first time, we demonstrate three terminal MRAM devices with immunity to magnetic fields up to 2T, 10ns field free switching and endurance > 1×10^{10} at 1µs write pulses. Our work addresses the scalability challenge of the in-plane SOT-MRAM and provides a new strategy for field free data writing.

4:50 PM

17-6 Demonstration of a Free-layer Developed With Atomistic Simulations Enabling BEOL Compatible VCMA-MRAM with a Coefficient ≥100fJ/Vm, R. Carpenter*, W. Kim*, K. Sankaran*, N. Ao*/**, M. Ben Chroud*/**, A. Kumar*, A. Trovato*, G. Pourtois*/***, S. Couet*, G. S. Kar*. *IMEC, **KU Leuven, ***University of Antwerp

For the first time, a VCMA coefficient >100fJ/Vm is reported in BEOL compatible magnetic tunnel junctions with good device characteristics such as TMR~180%, $\Delta\geq40$ and write endurance of $1x10^8$ events. This was enabled by using an imec developed non-perfect epitaxial model to drive development of a VCMA specific FL.

Session 18: Modeling and Simulation - Advanced simulation and modeling of FETs

Tuesday, December 14, 2:15 PM
Continental Ballrooms 1-3
Co-Chairs: Joddy Wang, Synopsys
Thierry Poiroux, CEA-Leti

2:20 PM

18-1 Exascale TCAD Simulations Enabled by Hardware-Accelerated High Performance Computing (Invited), N. Xu, Z. Jiang, P-S Lu*, Y. H. Chang*, J.-T. Li*, K.-C. Ong*, Z.-R. Xiao*, J. Wu*. TSMC North-America, *TSMC, Hsinchu

Rapid development of hardware accelerators and their software infrastructure has enabled tremendous progress in scientific computing which presented an opportunity to achieve reasonable turn-around time for physics-based, multi-level computations. Many TCAD modules and solvers need to be re-developed or renovated leveraging these to extend TCAD to "exascale" with ultimate predictiveness.

2:45 PM

18-2 Restructuring TCAD System: Teaching Traditional TCAD New Tricks, S. Myung, Wonik Jang, S. Jin*, J. M. Choe, C. Jeong, and D. Sin Kim, Samsung Electronics, Samsung Semiconductor Inc.

This paper presents a novel algorithm restructuring the traditional TCAD system. The proposed algorithm 1) predicts three-dimensional TCAD simulation in real-time while capturing a variance, 2) enables deep learning and TCAD to complement each other, 3) fully resolves convergence errors.

3:10 PM
18-3 Optimum Design of Channel Material and Surface Orientation for Extremely-Thin-Body nMOSFETs under New Modeling of Surface Roughness Scattering, K. Sumita, C.-T. Chen, K. Toprasertpong, M. Takenaka, S. Takagi. The University of Tokyo, Japan.

Assessment of surface-roughness-limited mobility, which dominates the mobility in Extremely-Thin-Body channels, for SOI, GOI and III-V-OI with various surface orientation has been delivered under new modeling of surface roughness scattering. As a result, (111) GOI has excellent mobility even in 2-nm-thick channels in comparison with other materials including 2D materials.

3:35 PM
18-4 Quantum Transport Simulation with the First-Order Perturbation: Intrinsic AC Performance of Extremely Scaled Nanosheet MOSFETs in THz Frequencies, P.-H. Ahn, S.-M. Hong. Gwangju Institute of Science and Technology

The first-order perturbation is included in the Non-Equilibrium Green Function (NEGF) simulation. The DC convergence behavior can be drastically improved. Even the small-signal (AC) analysis becomes available. The theoretical limit of the cutoff frequency in an extremely scaled nanosheet MOSFET is calculated.

4:00 PM Coffee Break

4:25 PM
18-5 Geometric Variability Aware Quantum Potential based Quasi-ballistic Compact Model for Stacked 6 nm-Thick Silicon Nanosheet GAA-FETs, S. Huang,*†, Z. Wu†, H. Xu*, J. Guo,* L. Xu, X. Duan,*, Q. Chen,*, G. Yang, Q. Zhang, H. Yin, L. Wang*, L. Li*, M. Liu, Institute of Microelectronics of the Chinese Academy of Sciences, *University of Chinese Academy of Sciences

Quantum-corrected quasi-ballistic compact model is developed for Stacked Silicon Nanosheet (SiNS) Gate-all-around (GAA) FETs. Theories of Density-Gradient-Poisson (DG-P), Singular perturbation and quasi-ballistic to interpret quantum mechanicals on density profile and charge transport are employed in analytical expressions of current, terminal charge and trans-capacitance.

4:50 PM
18-6 Physics-based Compact Modeling of Statistical Flicker Noise in FinFET Technology, M. Liu, J. Zhang, Z. Sun, R. Wang, R. Huang, Peking University

In this paper, a new compact model of flicker noise statistics for FinFET technology is proposed, based on inelastic trapping/de-trapping physics rather than elastic tunneling in conventional model of flicker noise. The proposed model is validated with measurement data of multiple technology nodes (16/14/12/7 nm) and different bias conditions.

Session 19: Emerging Device and Compute Technology - Ferroelectric based FET: From Fundamentals to Applications
Tuesday, December 14, 2:15 PM
Continental Ballroom 4
Co-Chairs: Uygar E. Avci, Intel

Woo-Bin Song, Samsung Electronics Co.

2:20 PM

19-1 In-Depth Understanding of Polarization Switching Kinetics in Polycrystalline Hf0.5Zr0.5O2 Ferroelectric Thin Film: A Transition From NLS to KAI, W. Wei**, W. Zhang, L. Tai**, G. Zhao, Pengpeng Sang, Q. Wang, F. Chen, M. Tang, Y. Feng, X. Zhan, Q. Luo*, Y. Liand J. Chen, *Shandong University, *Institute of Microelectronics of Chinese Academy of Sciences, **with Shandong University and Institute of Microelectronics of Chinese Academy of Sciences

The intrinsic switching characteristics of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) are measured accurately by using a novel pulse sequence. The average switching time decreases sharply with l scaling and sub-ns switching behavior is predicted at l≤3.89μm. Our observations imply that a transition happens from NLS to KAI model when T≤161K or l≤30nm.

2:45 PM

19-2 Apparent 'Negative Capacitance' Effects in the Pulse Measurements of Ferroelectrics, Z. Liu, H. Jiang*, and T.P. Ma, Yale University, *now at Micron Technology

In this work, we study the 'negative capacitance' (NC) effects observed in the pulse measurements of ferroelectric-resistor circuits (FE-R) and ferroelectric-dielectric (FE-DE) bilayer capacitors. Through numerical simulations based on Nucleation Limited Switching (NLS) model and experiments, we show that these presumable NC effects are the results of the ferroelectric switching.

3:10 PM

19-3 Standby Bias Improvement of Read After Write Delay in Ferroelectric Field Effect Transistors, Zheng Wang, Nujhat Tasneem, Jae Hur, Hang Chen, Shimeng, Yu, Winston Chern, Asif Khan, Georgia Institute of Technology

Read after write is a significant challenge in FEFETs because the speed limitation of neutralizing interfacial traps. We investigated two approaches to bypassing the fundamental limitation. We reduced the delay to 400 ns by applying a standby bias of ±1.5V, making the device 10^5 times faster.

3:35 PM

19-4 FeFETs for Near-Memory and In-Memory Compute (Invited), S. Salahuddin, A. Tan, S. Cheema, N. Shanker, M. Hoffmann, J.-H Bae, University of California Berkeley

Ferroelectric Field Effect Transistors (FeFETs) have seen resurgence in the recent years with the advent of doped HfO^2 as a ferroelectric material
[1]. Here we will discuss the potential and challenges for FeFETs as a memory solution for near-memory and in-memory computing.

4:00 PM Coffee Break

4:25 PM

19-5 Energy- and Area-efficient Fe-FinFET-based Time-Domain Mixed-Signal Computing In Memory for Edge Machine Learning, J. Luo, W. Xu, Y. Du, B. Fu, J. Song, Z. Fu, M. Yang, Y. Li, L. Ye, Qianqian Huang, and Ru Huang, Peking University

This work reports the first experimental demonstration of FeFET-based area- and energy-efficient time-domain CIM with 3T FE-delay-unit with dual-edge operation, and FeFET for activation with memory trace.

High-accuracy recognition and accelerated reinforcement learning are demonstrated under scaled VDD with record energy efficiency, showing its great potential for edge AI computing.

4:50 PM
19-6 BEOL Compatible Superlattice FerroFET-based High Precision Analog Weight Cell with Superior Linearity and Symmetry, K.A. Aabrar, J. Gomez, S.G. Kirtania, M.S. Jose, Y. Luo*, P.G. Ravikumar**, P.V. Ravindran*, H. Ye, S. Banerjee, S. Dutta, A.I. Khan*, S. Yu*, S. Datta. University of Notre Dame, *Georgia Institute of Technology, **Indian Institute of Technology Palakkad

We engineer the ferroelectric domain in a superlattice (SL) FE/DE stack, to demonstrate high precision FEFET analog weight cells with linearity and symmetry during potentiation and depression. We demonstrate switching speed of 100 ns. We integrate the SL with a BEOL compatible IWO transistor to demonstrate 128 conductance states .

Session 20: Optoelectronics, Displays, and Imaging - SPADs and LiDAR
Tuesday, December 14, 2:15 PM
Continental Ballroom 5
Co-Chairs: Sozo Yokogawa, Sony Semiconductor Solutions
Chiao Liu, Facebook Reality Labs

2:20 PM
20-1 A Back Illuminated 6 µm SPAD Pixel Array with High PDE and Timing Jitter Performance, S. Shimada, Y. Otake, S. Yoshida, S. Endo, R. Nakamura, H. Tsugawa, T. Ogita, T. Ogasahara, K. Yokochi, Y. Inoue*, K. Takabayashi*, H. Maeda*, K. Yamamoto*, M. Ono*, S. Matsumoto, H. Hiyama, and T. Wakano. Sony Semiconductor Solutions, *Sony Semiconductor Manufacturing

This paper presents a 6µm pitch silicon SPAD pixel array using 3D-stacked technology. A PDE of 20.2% and timing jitter FWHM of 137ps at λ=940nm with 3V excess bias were achieved. These state-of-the-art performances were allowed via the implementation of a pyramid surface structure and pixel potential profile optimization.

2:45 PM
20-2 3.2 Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing (Late News), K. Morimoto, J. Iwata, M. Shinohara, H. Sekine, A. Abdelghafar, H. Tsuchiya, Y. Kuroda, K. Tojima, W. Endo, Y. Maehashi, Y. Ota, T. Sasago, S. Maekawa, S. Hikosaka, T. Kanou, A. Kato, T. Tezuka, S. Yoshizaki, T. Ogawa, K. Uehira, A. Ehara, F. Inui, Y. Matsuno, K. Sakurai, T. Ichikawa. Canon Inc.

We present a new generation of scalable photon counting image sensors for low-light imaging and depth sensing, featuring read-noise-free operation. Newly proposed charge focusing SPAD is employed to a prototype 3.2 megapixel 3D backside-illuminated image sensor, demonstrating the best-in-class pixel performance with the largest array size in APD-based image sensors.

3:10 PM
20-3 InGaAs/InP SPAD detecting single photons at 1550 nm with up to 50% efficiency and low noise, F. Signorelli, F. Telesca, E. Conca, A. Della Frera*, A. Ruggeri*, A. Giudice*, A. Tosi. Politecnico di Milano, *Micro Photon Devices Srl

We present an InGaAs/InP single-photon avalanche diode (SPAD) for fiber-based quantum optics applications. Thanks to a redesigned structure, at 225 K our detector achieves a photon detection efficiency

up to 50% at 1550 nm, low noise, a timing jitter of ~70 ps (FWHM) and almost 1 Mcps maximum count rate.

3:35 PM Coffee Break

4:00 PM
20-4 Single-Chip Beam Scanner LiDAR Module for 20-m Imaging, H. Byun, Y. Cho, I. Hwang, B. Jang, J. Kim, C. Lee, E. Lee, J. Lee, T. Otsuka, D. Shim, C. Shin, D. Shin, K. Son, H. Choo, K. Ha. Samsung Electronics

We have implemented a light-detection and ranging system using a single-chip solid-state beam scanner and demonstrated 20-m ranging and imaging operation. The beam scanner is integrated with a 32-channel optical-phased-array, 37 optical amplifiers, and a tunable laser diode, and everything fits on an 8.7×3.0-mm^2 single chip fabricated using III-V-on-silicon processes.

Session 21: Emerging Device and Compute Technology - Compute-in-memory (CiM) with emerging devices and integration technology
Tuesday, December 14, 2:15 PM
Continental Ballroom 6
Co-Chairs: Suman Datta, University of Notre Dame
Nicolas Loubet, IBM Research

2:20 PM
21-1 Low-Power and Scalable Retention-Enhanced IGZO TFT eDRAM-Based Charge-Domain Computing, J. Liu, C. Sun**, W. Tang, Z. Zheng*, Y. Liu, H. Yang, C. Jiang, K. Ni**, X. Gong*, X. Li, Tsinghua University, *National University of Singapore, **Rochester Institute of Technology

This paper presents a power-efficient, scalable, and robust approach to the design of eDRAM-based compute-in-memory (CiM) accelerator for artificial neural networks using BEOL-compatible a-IGZO TFT technology. Highlighted with low-leakage devices, novel differential eDRAM and charge-domain computing, this work outperforms the prior TFT and CMOS-based CiM approaches with higher computing efficiency.

2:45 PM
21-2 Novel Analog in-Memory Compute with < 1 nA Current/Cell and 143.9 TOPS/W Enabled by Monolithic Normally-off Zn-rich CAAC-IGZO FET-on-Si CMOS Technology, H. Baba, S. Ohshita, T. Hamada, Y. Ando, R. Hodo, T. Ono, T. Hirose, Y. Kurokawa, T. Murakawa, H. Kunitake, T. Nakura*, M. Kobayashi**, H. Yoshida***, M.-C. Chen***, M.-H. Liao****, S.-Z. Chang***, S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd., *Fukuoka University, **The University of Tokyo, ***Powerchip Semiconductor Manufacturing Corporation, ****National Taiwan University

We demonstrate V_{th} stabilization in CAAC-IGZO FET (OSFET) and a monolithic Si CMOS + OSFET analog in-memory compute chip utilizing the low-leakage OSFET to drive Si CMOS devices in the subthreshold region. The chip achieves an ultra-low cell current below 1 nA/cell and an excellent operation efficiency of 143.9 TOPS/W.

3:10 PM
21-3 In-Memory Annealing Unit (IMAU): Energy-Efficient (2000 TOPS/W) Combinatorial Optimizer for Solving Travelling Salesman Problem, M.-C. Hong, L.-C. Cho, C.-S. Lin, Y.-H. Lin*, P.-A. Chen, I-T. Wang, P.-J. Tzeng*, S.-S. Sheu*, W.-C. Lo*, C.-I Wu*, and T.-H. Hou,

National Yang Ming Chiao Tung University, *Industrial Technology Research Institute, **National Taiwan University

An IMAU for solving TSP has been demonstrated for the first time through hardware-algorithm co-optimization. The binary RRAM-based IMAU with embedded simulated-annealing achieves energy efficiency of 2000TOPS/W. A multi-step simulated-annealing algorithm is proposed to solve floating-point TSP using merely 5-level weights and achieves the shortest route for the 10-city TSP.

3:35 PM Coffee Break

4:00 PM
21-4 Experimental Demonstration of Non-volatile Capacitive Crossbar Array for In-memory Computing, Y-C Luo, J. Hur, T-H Wang, A. Lu, S. Li, A. Islam Khan, S. Yu. Georgia Institute of Technology

Non-volatile ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ capacitive-crossbar array has been experimentally demonstrated with highly-linear vector-matrix multiplication. This design consumes only dynamic power, has no DC sneak paths and negligible IR drop along wires, and is compatible with 3D-stacking architecture. Array-level SPICE simulation shows 20~200x lower energy consumption than that of a resistive counterpart.

4:25 PM
21-5 Monolithic 3D Integration of Logic, Memory and Computing-In-Memory for One-Shot Learning, Yijun Li, Jianshi Tang,*, Bin Gao, Jian Yao*, Yue Xi, Yuankun Li, Tingyu Li, Ying Zhou, Zhengwu Liu, Qingtian Zhang, Song Qiu*, Qingwen Li*, He Qian, and Huaqiang Wu, Tsinghua University, * Chinese Academy of Science

We demonstrated a monolithic 3D integration (M3D) of Si-MOSFET, $HfAlO_x$-based analog RRAM, CNTFET and Ta_2O_5-based digital RRAM. Extensive structural analysis and electrical measurements were carried out. The M3D chip achieves GPU-equivalent classification accuracy (97.8%) in the one-shot learning task, and has a significant advantage in energy consumption and inference time.

4:50 PM
21-6 3D Stackable Broadband Photoresponsive InGaAs Biristor Neuron for a Neuromorphic Visual System with Near 1 V Operation, J.-K. Han, J. Sim, D.-M. Geum, S. K. Kim, J.-M. Yu, J. Kim*, S. Kim, and Y.-K. Choi, Korea Advanced Institute of Science and Technology, South Korea. *Korea Advanced Nano Fab Center

A photoresponsive InGaAs biristor neuron for neuromorphic visual systems is demonstrated. Visible and infrared light photoresponse with near 1 V operation was achieved thanks to narrow bandgap energy. Furthermore, monolithic 3D integration of neurons over the synapses is available to construct 3D neuromorphic visual system because of low temperature fabrication.

Session 22: Advanced Logic Technology - Front- and back-side advanced interconnects
Tuesday, December 14, 2:15 PM
Continental Ballrooms 7-9
Co-Chairs: Fadoua Chafik, Qualcomm
Francois Andrieu, CEA Leti

2:20 PM

22-1 Fully Self-Aligned Via Integration for Interconnect Scaling Beyond 3nm Node, A. Author, H.P. Chen, Y.H. Wu, H.Y. Huang, C.H. Tsai, S.K. Lee, C.C. Lee, T.H. Wei, H.C. Yao, Y.C. Wang, C.Y. Liao, H.K. Chang, C.W. Lu, Winston S. Shue, Min Cao. Taiwan Semiconductor Manufacturing Company

Two fully self-aligned via (SAV) integration schemes by metal recess approach and area-selective dielectric-on-dielectric (DoD) method are reported in this paper.

2:45 PM
22-2 Electromigration and Line R of Graphene Capped Cu Dual Damascene Interconnect, T. Nogami, S. Nguyen, H. Huang, N. Lanzillo, H. Shobha, J. Li, B. Peethela, A. Parbatani*, B. van Schravendijk*, B. Varadarajan*, I. Narkeviciute*, E. Srinivasan*, K. Sharma*, R. Knarr*, S. Schmitz*, V. Ramanan*, D. Edelstein. IBM Corp., IBM Research, USA. *Lam Research Corp, USA.

Selective graphene-CVD for 300 mm-wafers at BEOL temperatures(<400 °C) and dielectric deposition on graphene-cap without impacting graphene quality were developed to fabricate dual-damascene 30nm-pitch Cu/low-k interconnects. Poor electromigration of graphene-capped Cu agreed with Ab-Initio calculated binding energy of graphene/Cu. Instead, Graphene/Co-capped Cu showed decent electromigration with line resistance reduction(5 %).

3:10 PM
22-3 System Design Technology Co-Optimization for 3D Integration at <5nm nodes (Invited), S.C. Song, G. Nallapati, I. Khan, N. Nikfar, M. Miranda, B. Lim, V. Sanaka, V. Boynapalli, P. Gupta, S. Pandey, B. Xie, P. Feng, J. Choi, T. Rakshit, R. Shenoy, M. Nemani, C. Verrilli, J. Zhu, J. Chen, M. Nakamoto, L. Zhao, Y. Sun, F. Atallah, J. Kim, R. Attar, C. Chidambaram, Qualcomm Technology Inc

Partition of monolithic 2D (M2D) chip and heterogeneous integration of resultant chiplets are inevitable in near future. 3D stacking is required to maintain tight cross IP communication and fit into the limited footprint. We discuss M2D logic scaling knobs and choice criteria of 3DIC technology flavor for optimized system performance.

3:35 PM Coffee Break

4:00 PM
22-4 Design and Optimization of SRAM Macro and Logic Using Backside Interconnects at 2nm node, R. Chen, G. Sisto*, A. Jourdain, G. Hiblot, M. Stucchi, N. Kakarla, B. Chehab, S. M. Salahuddin, F. Schleicher, A. Veloso, G. Hellings, P. Weckx, D. Milojevic**, G. Van der Plas, J. Ryckaert, E. Beyne 1IMEC, *also with Cadence and University libre de Bruxelles, **also with University libre de Bruxelles

We explore the resource of backside (BS) interconnect for signal routing in SRAM macro and logic at 2nm technology node to tackle the technology scaling induced frontside (FS) BEOL routing congestion challenge. Compared to the FS BEOL, the BS routing is very beneficial in improving performance of long interconnect signals.

4:25 PM
22-5 Buried Power Rail Metal exploration towards the 1 nm Node, A. Gupta, D. Radisic, J. W. Maes*, O. Varela Pedreira, J-P. Soulié, N. Jourdan, H. Mertens, S. Bandyopadhyay, Q. T. Le, A. Pacco, N. Heylen, K. Vandersmissen, K. Devriendt, C. Zhu**, S. Datta**, F. Sebaai, S. Wang, M. Mousa***, J. Lee***, J. Geypen, B. De Wachter, B. Chehab, S. M. Salahuddin, G. Murdoch, S. Biesemans, Zs. Tőkei, E. Dentoni Litta, N. Horiguchi, imec vzw, *ASM Belgium NV, **ASM Microchemistry Oy, ***ASM America Inc

BPR & Via-to-BPR metal exploration towards 1 nm node is reported. W-BPR stack optimized to minimize line resistivity. W-BPR-W-VBPR in parallel with W-Contact-to-Active(M0A)-S/D contact R tuning discussed. Mo-BPR introduced for 2/1 nm nodes, benchmarking its resistance & electromigration against W & Ru. Mo-BPR recess & Mo-compatible VBPR clean are shown.

Session 23: Sensors, Mems, and Bioelectronics - Novel Sensor Technologies
Tuesday, December 14, 2:15 PM
Imperial Ballroom A
Co-Chairs: Arvind Balijepalli, NIST
Hyunjoo Jenny Lee, KAIST

2:20 PM
23-1 Hardware Neural Network using Hybrid Synapses via Transfer Learning: WOx Nano-Resistors and TiOx RRAM Synapse for Energy-Efficient Edge-AI Sensor, W. Choi, M. Kwak, S. Heo, K. Lee, S. Lee and H. Hwang, Pohang University of Science and Technology

We present a neural network (NN) based intelligent sensor for biomedical applications on edge using nano-electronic synapses. The proposed NN comprises newly developed WO_x resistors and TiO_x based RRAMs. We have confirmed high classification accuracy at the edge even with a limited training data and parameters (5.4%) of entire system.

2:45 PM
23-2 Low-power and Self-powered Environmental Sensor Assisted by Deep-Learning Technology (Invited), I. Park, KAIST

Microfabricated MEMS devices and functional nanomaterials can enable low-power and self-powered gas sensors for the internet-of-things (IoT) applications. In this **paper**, various low-power / self-powered gas sensors and deep learning-based sensor signal processing technologies developed by our research group are presented.

3:10 PM
23-3 Human Retinal Photoreceptor-Inspired Sensor with Adjustable Gain from 0.1-106 and Wide Dynamic Range Over 140dB, Y. Qi*, X. Liu*, Z. Feng, Q. Li, K. Su, X. Zhou, J. Guo, and K. Wang*, Sun Yat-sen University, *also with Pazhou Lab

Inspired by a human retina, we report on a sensor that is formed by a photodiode-body-biased MOSFET (PD-MOSFET). Study suggests that the proposed sensor behaves similarly to a human retinal photoreceptor in terms of photosensing functionalities with a gain tunable, a dynamic range of >140dB in a broad spectral range.

3:35 PM Coffee Break

4:00 PM
23-4 1.62µm Global Shutter Quantum Dot Image Sensor Optimized for Near and Shortwave Infrared, J. S. Steckel, E. Josse, A. G. Pattantyus-Abraham, M. Bidaud, B. Mortini, H. Bilgen, O. Arnaud, S. Allegret-Maret, F. Saguin, L. Mazet, S. Lhostis, T. Berger, K. Haxaire, L. L. Chapelon, L. Parmigiani, P. Gouraud, M. Brihoum, P. Bar, M. Guillermet*, S. Favreau, R. Duru, J. Fantuz, S. Ricq, D. Ney, I. Hammad, D. Roy, A. Arnaud , B. Vianne, G. Nayak, N. Virollet, V. Farys, P. Malinge, A. Tournier, F. Lalanne, A. Crocherie, J. Galvier, S. Rabary, O. Noblanc, H. Wehbe-Alause , S. Acharya, A. Singh, J. Meitzner, D. Aher, H. Yang, J. Romero, B. Chen, C.Hsu, K. C. Cheng, Y. Chang, M. Sarmiento, C. Grange, E. Mazaleyrat, K. Rochereau,STMicroelectronics

We have developed a 1.62µm pixel pitch global shutter sensor optimized for imaging in the NIR and SWIR. This breakthrough was made possible through the use of our colloidal quantum Dot thin film technology. We have scaled up this new platform technology to our 300mm manufacturing toolset.

4:25 PM

23-5 CMOS-MEMS multi-sensor single chip with high heat dissipation and low-temperature hermetic sealing, C. Y. Chang, S. H. Tseng, M. H. Chiang, C. T. Hsin , L. Y. Ke, Y. J. Wang, C. Y. Yeh, H. H. Tsai, Y. Z. Juang, and W. K. Yeh. Taiwan Semiconductor Research Institute, Hsinchu, Taiwan.

This paper presents a single chip of a three-axis CMOS-MEMS accelerometer, a chopper-stabilized automatic offset calibration readout circuit driven by a MEMS resonator oscillator, and a built-in Pirani vacuum sensor for verification of low-temperature hermetic gold-bumps sealing and thermal effects (204 µV/°C) within the pressure range of $0.05–10^3$
mbar.

4:50 PM

23-6 Study of DC-Driven MEM Relay Oscillators for Implementation of Ising Machines, X, Hu*, L. Prospero Tatum*, S. Fabian Almeida**, T. Kedir Esatu*, and T-J King Liu*
*University of California, Berkeley, **DiDi Labs

DC-bias-dependent oscillatory behavior of micro-electro-mechanical (MEM) relays is investigated via experimental study and replicated with finite-element-method-based computer simulations. Sub-harmonic injection locking and coupled oscillation behaviors of MEM relays then are demonstrated via simulation, indicating that coupled MEM relays can be used to implement an Ising machine.

Session 24: Panel Discussion
Tuesday, December 14, 8:00 PM – 10:00 PM
Continental Ballrooms 4-6

Is HW/SW co-design a necessary evil or a symbiotic partner?
Moderator: Myung-hee Na, SK Hynix

Session 25: Memory Technology/Modeling And Simulation/Advanced Logic Technology Focus Session - STCO for memory-centric computing and 3D integration
Wednesday, December 15, 9:00 AM
Grand Ballroom A
Co-Chairs: Qiangfei Xia, University of Massachusetts
Xinyu Bao, TSMC

9:05 AM

25-1 Human-centric Computing (Invited), J.M. Rabaey, University of California at Berkeley and imec

A human intranet concept complementing the nervous system for revalidation and augmentation is introduced. Addressing the computational aspects of such an intranet is complicated by extreme energy and form-factor limitations, and requires innovation on all fronts ranging from computational models to heterogeneous integration.

9:30 AM

25-2 In-Memory Computing with Associative Memories — A Cross-Layer Perspective (Invited), X. S. Hu, M. Niemier, A. Kazemi, A.F. Laguna, K. Ni*, R. Rajaei, X. Yin**, University of Notre Dame, *Rochester Institute of Technology, **Zhejiang University

Associative memory (AM), which efficiently "associates" an input query with appropriate data words/locations in the memory, is a powerful in-memory-computing core. This paper showcases representative AM designs based on non-volatile memory technologies. End-to-end evaluations for machine learning applications are discussed to demonstrate the benefits contributed by each design layer.

9:55 AM
25-3 Monolithic 3D Compute-in-Memory Accelerator with BEOL Transistor based Reconfigurable Interconnect (Invited), Y. Luo, S. Dutta*, A. Kaul, S-K Lim, M. Bakir, S. Datta*, S. Yu, Georgia Institute of Technology, *University of Notre Dame

CIM-based inference engine's area scaling is limited by availability of logic voltage compatible NVM at leading-edge node. This work performs system-technology co-design (STCO) of a monolithic 3D (M3D) CIM accelerator using the back-end-of-line (BEOL) compatible oxide channel (IWO) MOSFET for write circuit and the IWO-based FeFET for reconfigurable interconnect.

10:20 AM
25-4 The Future of Hardware Technologies for Computing: N3XT 3D MOSAIC, Illusion Scaleup, Co-Design (Invited), R.M. Radway, K. Sethi, W.-C. Chen, J. Kwon, S. Liu, T.F. Wu*, E. Beigne*, M.M. Shulaker**, H.-S.P. Wong, and S. Mitra, Stanford University, *Facebook, Inc.,**MIT

The next leap in computing performance requires the next leap in integration. Just as integrated circuits brought together discrete components, this next level of integration must seamlessly fuse disparate parts of a system – e.g., compute, memory, inter-chip connections – synergistically for large energy and execution time benefits. We present this vision, its challenges, and discuss recent advances at the technology, architecture, and system levels.

10:45 AM
25-5 Enabling RRAM-Based Brain-Inspired Computation by Co-design of Device, Circuit, and System (Invited), C. Dou, X. Xu, X. Zhang*, L. Wang, W. Ye, J. An, J. Yang, Q. Luo, D. Dong, T. Shi, J. Liu, D. Shang, F. Zhang, Q. Liu*, M. Liu*, Institute of Microelectronics of the Chinese Academy of Sciences, *Fudan University

In this work, we discussed developing RRAM-based brain-inspired computation, including computing-in-memory and neuromorphic computing, by co-design device, circuit and system. We proposed optimized the synaptic array, the sparsity-aware analog-to-digital converter (ADC), and the energy- and area-efficient NbO_x devices-based spiking neurons. Several RRAM CIM chip designs are presented at the last.

11:10 AM
25-6 Co-design in High Performance Computing Systems (Invited), J. H Moreno, HF Wen, IBM Research

The paper will first share a co-design experience for designing and building the CORAL supercomputers delivered to the Department of Energy Labs (DoE) in 2018. The second part is to focus on Cloud Computing and how the hybrid-cloud approach will change future computing environments.

11:35 AM

25-7 Mm-wave automotive radar: from evolution to revolution, (Invited) K. Doris, F. Jansen, M. Lont, T.V. Dinh, W. Syed, G. Carluccio, L. Tiemeijer, E. Janssen, T. Saric, Z. Zong, J. Osorio, E. Janssen, S. Thuries, M. Ganzerli, A. Filippi, A. d. Graauw, D. Salle, and C. Vaucher, NXP Semiconductors

This paper describes the evolving landscape of 77GHz automotive radar at technology, circuit, and waveform level and shows in the horizon the opportunities and challenges ahead when stepping over to even higher frequencies.

Session 26: Advanced Logic Technology - Advances in Nanosheet FET devices
Wednesday, December 15, 9:00 AM
Grand Ballroom B
Co-Chairs: Myunggil Kang, Samsung
Naomi Yoshida, Applied Materials

9:05 AM
26-1 Vertical-Transport Nanosheet Technology for CMOS Scaling beyond Lateral-Transport Devices, H. Jagannathan, B. Anderson, C-W. Sohn*, G. Tsutsui, J. Strane, R. Xie, S. Fan, K-I. Kim*, S. Song*, S. Sieg, I. Seshadri, S. Mochizuki, J. Wang, A. Rahman, K-Y. Cheon*, I. Hwang*, J. Demarest, J. Do*, J. Fullam, G. Jo*, B. Hong*, Y. Jung*, M. Kim*, S. Kim*, R. Lallement, T. Levin, J. Li, E. Miller, P. Montanini, R. Pujari, C. Osborn, M. Sankarapandian, G-H. Son*, C. Waskiewicz, H. Wu, J. Yim*, A. Young, C. Zhang, A. Varghese, R. Robison, S. Burns, K. Zhao, T. Yamashita, D. Dechene, D. Guo, R. Divakaruni, T. Wu, K-I. Seo*, H. Bu. IBM Research, *Samsung Electronics

We demonstrate, for the first time, Vertical-Transport Nanosheet (VTFET) CMOS logic transistors at sub-45nm gate pitch to overcome the Contacted Gate Pitch barrier faced by Lateral-Transport-FETs. Hardware results show excellent electrostatics, symmetric SS/DIBL with Si/SiGe source/drain, Zero Diffusion Break isolation, I/O FETs, functional ring oscillators, and significant Ceff reduction (~50%).

9:30 AM
26-2 Comparison of Electrical Performance of Co-Integrated Forksheets and Nanosheets Transistors for the *nm Technological Node and Beyond, R. Ritzenthaler, H. Mertens, G. Eneman, E. Simoen, E. Bury, P. Eyben, F. M. Bufler, Y. Oniki, B. Briggs, B.T. Chan, A. Hikavyy, G. Mannaert, B. Parvais,*, A. Chasin, J. Mitard, E. Dentoni Litta, S. Samavedam, and N. Horiguchi, IMEC, * Vrije Universiteit Brussels

Forksheets are proposed to reduce the footprint of transistors. We report on a comparison of DC performance of co-integrated Forksheets/Nanosheets. We show that short channel control and transport properties are comparable down to L_G=22nm, and that gate stack reliability and S/D strain boosters option do not suffer from Forksheet process.

9:55 AM
26-3 Critical Elements for Next Generation High Performance Computing Nanosheet Technology, R. Bao, C. Durfee, J. Zhang, L. Qin, J. Rozen, H. Zhou, J. Li, S. Mukesh, S. Pancharatnam, K. Zhao, C. D. Adams, E. Leobandung, V. Narayanan, D. Guo, H. Bu. IBM Semiconductor Technology Research, Albany, NY

We show a simple NS pFET SiGe provides 40% mobility increase and 10% performance over Si with reduced Vt and improved NBTI. Volumeless multi-Vt and metal multi-Vt enhance the performance due to

good Vt uniformity and improved reliability. We also demonstrate the suspension can be reduced for performance improvement.

10:20 AM

26-4 Highly Stacked 8 Ge0.9Sn0.1 Nanosheet pFETs with Ultrathin Bodies (~3nm) and Thick Bodies (~30nm) Featuring the Respective Record ION/IOFF of 1.4E7 and Record ION of 92µA at VOV=VDS= -0.5V by CVD Epitaxy and Dry Etching, C-E Tsai, Y-C Liu, C-T Tu, B-W Huang, S-R Jan, Y-R Chen, J-Y Chen, S-J Chueh, C-Y Cheng, C-J Tsen, Y. Ma, and C. W. Liu, National Taiwan University

The 8 stacked $Ge_{0.9}Sn_{0.1}$ ultrathin bodies (~3nm) are realized by the mutual optimization between epitaxy and etching. Thanks to the quantum confinement, the record I_{ON}/I_{OFF} ($1.4x10^7$) is achieved among GeSn/Ge 3D pFETs. For thick nanosheets, the record I_{ON} of 92µA per stack at V_{OV}=V_{DS}=-0.5V is achieved among GeSn/Ge 3D pFETs.

10:45 AM

26-5 Gate-Last IO Transistors based on Stacked Gate-All-Around Nanosheet Architecture for Advanced Logic Technologies, M. Bhuiyan, M. Kim*, H. Zhou, H. Lo*, S. Siddiqui, M. Stolfi*, T. Guarini*, R. Pujari, E. Davey*, E. Stuckert, J. Li, A. Chou, K. Zhao, M. Wang, D. Guo, B. Colombeau*, N. Loubet, B. Haran*, H. Bu. IBM Research, *Applied Materials, USA.

For the first time, we demonstrate gate-all-around nanosheet based I/O transistors with gate-last fabrication showing high V_{bd} reaching >5.5V and a good range of V_{bd}/V_{max} tuning. Novel oxidation process enables thick gate oxide formation by expanding space between silicon sheets. I/O devices with T_{sus} of 12nm have been demonstrated.

Session 27: Modeling and Simulation - Low-dimensional and spin-based devices

Wednesday, December 15, 9:00 AM
Continental Ballrooms 1-3
Co-Chairs: Zlatan Stanojevic, Global TCAD Solutions
Lan Wei, University of Waterloo

9:05 AM

27-1 Self-energies in Atomistic Quantum Transport for Energy Transfer at Irregular Interfaces (Invited), J. Charles, D. Lemus, T. Kubis, Purdue University

This presentation gives an introduction to NEGF and its self-energies. Atomistic examples of phonon and impurity scattering agree quantitatively with experiments. The latest NEGF development, ROBIN, will be presented as well. ROBIN overcomes periodic boundary conditions in material simulations and gives critical material insights.

9:30 AM

27-2 Two Dimensional Silicon Atomic Layer Field-Effect Transistors: Electronic Property, Metal-Semiconductor Contact, and Device Performance, P. Sang, Q. Wang, W. Wei, L. Tai, X. Zhan, Y. Li, Jiezhi Chen, Shandong University

Focusing on three 2D silicon semiconductors, we in-depth studied the intrinsic transport, metal-semi contact, and device performance of the 2D silicon. LHD-Si and hhk-Si present great potentials in nanoelectronics. Employing proper electrode, the sub-60 mV/dec SS (Cold-source) and high I_{on} (Schottky-free) were respectively achieved for LHD-Si base FET.

9:55 AM

27-3 Extended Scale Length Theory Targeting Low-Dimensional FETs for Carbon Nanotube FET Digital Logic Design-Technology Co-optimization, C. Gilardi, B. Chehab*, G. Sisto*, P. Schuddinck*, Z. Ahmed*, O. Zografos*, Q. Lin, G. Hellings*, J. Ryckaert*, H.-S. P. Wong, S. Mitra, Stanford University, Stanford, CA, *imec

We present a new extended scale length theory and derive a new Carbon Nanotube FET (CNFET) leakage compact model including inelastic band-to-band tunneling. Our extensive design-technology co-optimization quantifies large (up to 7×) Energy Delay Product benefits of CNFET ring oscillators (vs. silicon NanoSheet, ForkSheet, CFET) at the 2nm node.

10:20 AM

27-4 Design Guidelines of Magnetic Tunnel Junctions with Two-dimensional Tunneling Barrier Layer: Atomistic study from material to device, X. Ma, *, J. Chen**, K. Wang*, R. Wang, *, R. Huang, Peking University, *Chinese Academy of Sciences, **Shandong University

Based on DFT and NEGF formalism, the MTJs with 2D tunneling barrier material is systematic numerical simulations from the physical level to the device level. The magnetic properties , spin-orbit-coupling , tunneling magnetoresistance and I-V characteristics are thoroughly discussed.The effects of TB doping and interfacial layer engineering are also discussed.

10:45 AM

27-5 Large-Scale 2D Spin-Based Quantum Processor with a Bi-Linear Architecture, F. A. Mohiyaddin, R. Li, S. Brebels, G. Simion, N. I. Dumoulin Stuyck*, C. Godfrin, M. Shehata*, A. Elsayed*, B. Gys*, S. Kubicek, J. Jussot, Y. Canvel, S. Massar, P. Weckx, P. Matagne, M. Mongillo, B. Govoreanu, I. P. Radu. Imec, * also with KU Leuven

We propose a bi-linear device architecture for silicon-based quantum processors. Using advanced modeling, we report critical dimensions, gate-times, fidelities, and on-chip resources for error correction. Our design is compact, realizable with existing fabrication technology, and allows planar integration of control circuitry, thereby providing a scalable route for silicon quantum computers.

11:10 AM

27-6 Time Division Multiplexing Ising Computer Using Single Tunable True Random Number Generator Based on Spin Torque Nano-Oscillator, B. Zhang, Y. Liu, T. Gao, D. Zhang, W. Zhao, L. Zeng, Beihang University, and with Beihang Hangzhou Innovation Institute Yuhang

A Time Division Multiplexing (TDM) Ising computer using single tunable true random number generator which is comprised of a Spin Torque Nano-Oscillator (STNO). A novel incremental coupling rule is proposed. Our digital TRNG can be simply reused acting as a P-Bit array by time division multiplexing.

Session 28: Memory Technology - Memory Technology - Emerging memory (PCRAM/OTS)

Wednesday, December 15, 9:00 AM

Continental Ballroom 4

Co-Chairs: SangBum Kim, Seoul National University

Hsiang-Lan Lung, Macronix

9:05 AM

28-1 Heater system optimization for robust ePCM reliability and scalability in 28nm FDSOI technology, R. Ranica, R. Berthelon, A. Gandolfo, G. Samanni, E. Gomiero, J. Jasse, P. Mattavelli, J. Sandrini, M. Querre, Y. Le-Friec, J. Poulet, V. Caubet, L. Favennec, C. Boccaccio, G. Ghezzi, C. Gallon,

JC. Grenier, B. Dumont, O. Weber, A. Villaret, R. Beneyton, N. Cherault, D. Ristoiu, S. Del Medico, O. Kermarrec, JP. Reynard, P. Boivin, A. Souhaite*, L. Desvoivres*, S. Chouteau*, PO. Sassoulas, L. Clement, A. Valery, E. Petroni, D. Turgis, A. Lippiello, L. Scotti, F. Disegni, A. Ventre, D. Ornaghi, M. De Tomasi, A. Maurelli, A. Conte, F. Arnaud, A. Redaelli, R. Annunziata, P. Cappelletti, F. Piazza, P. Ferreira, R. Gonella, E. Ciantar, STMICROELECTRONICS, *CEA-LETI Grenoble

Optimization of Heater system in ePCM realized with 28nm FDSOI technology is reported in this paper. ePCM reliability, considering retention and endurance, is characterized. The key role played by Heater is demonstrated. Finally, TiSiN ALD deposition process is proposed as the solution to improve uniformity and scalability of Heater resistance.

9:30 AM
28-2 Uncertainty Quantification Based on Multilevel Conductance and Stochasticity of Heater Size Dependent C-doped $Ge_2Sb_2Te_5$ PCM Chip, L. Yan, X. Li*, Y. Zhu, B. Yan, Y. Lu, T. Zhang, Y. Yang, Z. Song*, R. Huang, Peking University, *Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences

Here we fabricate 4Mb C-GST PCM chip with varied heater electrode size of 3 and 4 nm to realize uncertainty quantification of deep learning. The system constructed is able to dramatically improve OOD detection accuracy while maintaining classification and misclassification accuracies, with significant time and energy reductions compared with GPU.

9:55 AM
28-3 Temperature sensitivity of analog in-memory computing using phase-change memory, I. Boybat, B. Kersting, S. Ghazi Sarwat, X. Timoneda, R. L. Bruce*, M. BrightSky*, M. Le Gallo, A. Sebastian, IBM Research Europe, *IBM T.J. Watson Research Center

We focus on phase-change memory (PCM)-based deep learning acceleration and investigate for the first time the impact of temperature on multi-level PCM conductance states used to store the synaptic weights. With more than 1.1M PCM devices, we demonstrate high inference accuracies for various network architectures under ambient temperature variations.

10:20 AM
28-4 Polarity-dependent threshold voltage shift in ovonic threshold switches: Challenges and opportunities, T. Ravsher, R. Degraeve*, D. Garbin*, A. Fantini*, S. Clima*, G. Luca Donadio*, S. Kundu*, H. Hody*, W. Devulder*, J. Van Houdt, V. Afanas'ev, R. Delhougne*, G. Sankar Kar*. KU Leuven, *imec

We investigate the operation of Si-Ge-As-Te Ovonic Threshold Switch (OTS) selectors under bipolar pulses. Threshold voltage increases noticeably if the previous pulse had opposite polarity. This effect is long-lasting and present under different test conditions. Its impact on 1S1R operation is discussed, including possible applications, such as OTS-only memory element.

10:45 AM
28-5 Low variability high endurance and low voltage arsenic-free selectors based on GeCTe, E. Ambrosi, C. H. Wu, H. Y. Lee, P. C. Chang, C. F. Hsu, C. M. Lee, C. C. Chang, Y. Y Chen, D. W. Heh, D. H. Hou, P. J. Liao, T. Y. Lee, M. F. Chang, H.-S. P. Wong, and X. Y. Bao, Taiwan Semiconductor Manufacturing Company, Ltd.

This work studies the mechanisms and performance of low voltage arsenic-free GeCTe-based selectors. A remarkable endurance of $4x10^{11}$ cycles around 100µA is demonstrated, together with a projected endurance

~10^{13} cycles at 20μA. The nitrogen-doped GeCTe selectors are also presented with enhanced thermal stability (400°C, 30min) and ultra-low threshold voltage cycle-to-cycle variation (,30mV/σ).

11:10 AM

28-6 Optimizing AsSeGe Chalcogenides by Dopants for Extremely Low I_{OFF}, High Endurance and Low V_{th} Drift 3D Crosspoint Memory, H. Y. Cheng, W C. Chien, I. T. Kuo, C. H. Yang, Y. C. Chou, R. L. Bruce*, E. K. Lai, D. Daudelin*, C. W. Yeh, L. Gignac*, C. W. Cheng*, A. Grun, C. Lavoie*, N. Gong*, L. Buzi*, H. Y. Ho, A. Ray*, H. Utomo*, M. BrightSky* and H. L. Lung, Macronix International Co., Ltd., *IBM T. J. Watson Research Center

The doping effect on AsSeGe OTS materials is comprehensively studied. While B, C, S doped selectors suffer a stringent trade-off, Si and In doped selectors demonstrate an extremely low V_{tS} and V_{tR} drift characteristics. We demonstrated crosspoint operation in a 1k by 1k cross-point ADM memory arrays.

Session 29: Optoelectronics, Displays, and Imaging - Integrated Photonics

Wednesday, December 15, 9:00 AM
Continental Ballroom 5
Co-Chairs: Yuriko Maegami, National Institute of Advanced Industrial Science and Technology (AIST)
Na Young Kim, University of Waterloo

9:05 AM

29-1 Reconfigurable Si-based Active Metasurface with Ultra Low Loss and Crosstalk for LiDAR, B. G. Jeong, J. Park, S. I. Kim, M. Lee, J. Jang, K. Ha, and H. Choo, Samsung Electronics

We have demonstrated a Si-based SLM using asymmetric resonator composed of p-i-n diode structure and DBR. We obtained the world-record reflection efficiency over 50% and the phase modulation of 300°. We also measured the maximum side-mode-suppression-ratio of 10.53 dB, also the world record, excellent SNR and steering capability.

9:30 AM

29-2 Silicon Photonics Beyond Optical Interconnects (Invited), F. Boeuf, C. Barrera (Invited), A. Fincato, H. Tang**, S. Guerber*, S. Monfray, S. Ohno**, D. Fowler*, I. Charlet, L. Gianini*, A. Simbula***, L. Maggi, M. Shaw, K. Toprasertpong**, S. Takagi**, and M. Takenaka**, STMicroelectronics,
*CEA-LETI, **The University of Tokyo, ***University of Cagliari

In this paper we present the use of a 300mm Si-Photonic platform for applications beyond the data-communication. Beam steering and beam shaping for freespace-optics and hybrid III-V/Si optical switch for computing applications are discussed.

9:55 AM

29-3 Nanolasers: towards large-scale phase-locked laser arrays (Invited), Y. Fainman, S. Jiang. University of California San Diego

Nanolasers are extensively studied as on-chip light sources due to their ultra-small footprint and other advantages. This paper introduces the development of the metallo-dielectric nanolasers towards their applicability in large-scale laser arrays, ranging from their design and demonstration to the on-going work on the demonstration of phase-locking in bridge-coupled nanolasers.

10:20 AM

29-4 First demonstration of monolithic waveguide-integrated group IV multiple-quantum-well photodetectors on 300 mm Si substrate for 2 µm optoelectronic integrated circuits, H. Wang, Y. Chen, G. Zhang, J. Zhang, H. Xu, Y.-C. Huang*, X. Gong, National University of Singapore, *Applied Materials Inc.

We report a monolithic waveguide integrated $Ge_{0.92}Sn_{0.08}Ge$ MQW photodetector for 2-µm detection on 300-mm Si wafer. The first of such device for group IV materials. Our approach offers a cost-effective, large-scale manufacturable, and CMOS compatible solution for 2-µm optoelectronic integrated systems. PD exhibits low dark current density and high responsivity.

Session 30: Optoelectronics, Displays, and Imaging - Image Sensors
Wednesday, December 15, 9:00 AM
Continental Ballroom 6
Co-Chairs: Boyd Fowler, OmniVision
Albert Theuwissen, Harvest Imaging / Delft University of Technology

9:05 AM
30-1 Highly Efficient Color Separation and Focusing in the Sub-micron CMOS Image Sensor, S. Yun, S. Roh, S. Lee, H. Park, M. Lim, S. Ahn, and H. Choo. Samsung Advanced Institute of Technology

We report nanoscale metaphotonic color-routing (MPCR) structure that can significantly improve the low-light performance of a sub-micron CMOS image sensor. Fabricated on the Samsung's commercial 0.8µm-pixel sensor, MPCR structures confirms increased quantum efficiency (+20%), a luminance SNR improvement (+1.22 dB@5lux), a comparably low color error and great angular tolerant response.

9:30 AM
30-2 Automotive 8.3 MP CMOS Image Sensor with 150 dB Dynamic Range and Light Flicker Mitigation (Invited), M. Innocent, S. Velichko, D. Lloyd*, J. Beck, A. Hernandez, B. Vanhoff, C. Silsby, A. Oberoi, G. Singh, S. Gurindagunta, R. Mahadevappa, M. Suryadevara, M. Rahman*, and V. Korobov, ON Semiconductor, *not currently with ON Semiconductor

New 8.3 MP image sensor for automotive applications has 2.1 µm pixel with overflow and triple gain readout. In comparison to earlier 3 µm pixel, flicker free range increased to 110 dB and total range to 150 dB. SNR in transitions stays above 25 dB up to 125°C.

9:55 AM
30-3 A 2.9µm Pixel CMOS Image Sensor for Security Cameras with high FWC and 97 dB Single-Exposure Dynamic Range, T. Uchida, K. Yamashita, A. Masagaki, T. Kawamura, C. Tokumitsu, S. Iwabuchi*,. Onizawa*, M. Ohura*, H. Ansai, K. Izukashi, S. Yoshida, T. Tanikuni*, S. Hiyama*, H. Hirano, S. Miyazawa, and Y. Tateshita, Sony Semiconductor Solutions, *Sony Semiconductor Manufacturing,

We developed a new photodiode structure for CMOS image sensors with a pixel size of 2.9µm. It adds the following two structures: one forms a strong electric field P/N junction on the full-depth deep-trench isolation side wall, and the other is a dual-vertical-gate structure.

10:20 AM
30-4 3D Sequential Process Integration for CMOS Image Sensor, K. Nakazawa, J. Yamamoto, S. Mori, S. Okamoto, A. Shimizu, K. Baba, N. Fujii, M. Uehara, K. Hiramatsu, H. Kumano, A. Matsumoto, K. Zaitsu, H. Ohnuma, K. Tatani, T. Hirano, and H. Iwamoto, SONY Semiconductor Solutions Corporation, Kanagawa Japan

We developed a new structure of pixel transistors stacked over photodiode fabricated by 3D sequential process integration. With this technology, we successfully increased AMP size and demonstrated backside-illuminated CMOS image sensor of 6752 x 4928 pixels at 0.7um pitch to prove its functionality and integrity.

Session 31: Reliability of Systems and Devices - Advanced Logic Device Reliability
Wednesday, December 15, 9:00 AM
Continental Ballrooms 7-9
Co-Chairs: Xavier Garros, CEA-LETI
Byoung Min, Globalfoundries

9:05 AM
31-1 Understanding and modelling the PBTI reliability of thin-film IGZO transistors, A. Chasin, J. Franco, K. Triantopoulos, H. Dekkers, N. Rassoul, A. Belmonte, Q. Smets, S. Subhechha, D. Claes, M. J. van Setten, J. Mitard, R. Delhougne, V. Afanas'ev, B. Kaczer, G. S. Kar, imec

PBTI in IGZO transistors is controlled by the gate-dielectric pre-existent electron traps and its hydrogen content. The degradation process can be composed of up to four mechanisms with different kinetics, voltage acceleration factors and activation energies. Optimized devices achieve record lifetime of 1 year continuous operation at 95°C and V_{ov}=1V.

9:30 AM
31-2 Understanding Hot Carrier Reliability in FinFET Technology from Trap-based Approach (Invited), R. Wang, Z. Sun, Y.-Y. Liu*, Z. Yu, Z. Wang, X. Jiang*, R. Huang, Peking University, *Chinese Academy of Sciences

The recent advances of our studies on HCD are presented from trap-based approach. The microscopic speculation of interface trap generation is carried out by time-dependent DFT (TDDFT) simulation in "real-time". A unified compact model has been proposed which can accurately predict hot carrier degradation and variation in full V_{gs}/V_{ds} bias.

9:55 AM
31-3 Evidence of Tunneling Driven Random Telegraph Noise in Cryo-CMOS, J. Michl, A. Grill*, B. Stampfer, D. Waldhoer, C. Schleich, T. Knobloch, E. Ioannidis**, H. Enichlmair**, R. Minixhofer**, B. Kaczer*, B. Parvais*, B. Govoreanu*, I. Radu*, T. Grasser, and M. Waltl, TU Wien, *imec, **ams AG

Using single defect measurements, we show that even at 4 K, there are active defects causing Random Telegraph Noise. With nuclear tunneling being the dominant charge transition we can explain the temperature dependence of charge trapping. Our measurements and simulations indicate that interface defects are responsible for cryogenic RTN.

10:20 AM
31-4 Low-temperature atomic and molecular hydrogen anneals for enhanced chemical SiO2 IL quality in low thermal budget RMG stacks, J. Franco, H. Arimura, J.-F. de Marneffe, Z. Wu, A. Vandooren, L.-Å Ragnarsson, E. Dentoni Litta, N. Horiguchi, K. Croes, D. Linten, V. Afanas'ev*, T. Grasser**, B. Kaczer, Imec, *KU Leuven, Belgium. **T.U. Wien

We present (combination of) atomic and molecular hydrogen exposures of the SiO_2 interfacial layer yielding excellent pMOS NBTI reliability in a low-temperature RMG flow ≤450°C), and compatible with

multi-V,sub$_{th}$ solutions. The treatment is demonstrated in a transistor vehicle, showing sufficient thermal stability for BEOL, enhanced carrier mobility and breakdown reliability.

10:45 AM

31-5 Next Generation of Robust Aviation Electrification - Challenges and Opportunities (Invited), P. Kshirsagar, J. Ewanchuk, M. Kheraluwala*, B. Wood**, Raytheon Technologies Research Center, *Collins Aerospace, **Pratt and Whitney

This paper will highlight challenges and opportunities in aviation electrification in achieving high power density, efficiency and reliability highlight ongoing efforts towards aviation decarbonization. The key topics considered are (a) more electric aircrafts and (b) hybrid and turbo-electric propulsion systems along with sustainable aviation fuels (SAF).

Session 32: Emerging Device and Compute Technology - CMOS+X Devices: New Microwave, and Spintronics

Wednesday, December 15, 9:00 AM
Imperial Ballroom A
Co-Chairs: Jean Anne Incorvia, University of Texas at Austin
Uygar E. Avci, Intel

9:05 AM

32-1 Sub-10-nm Diameter GaSb/InAs Vertical Nanowire Esaki Diodes with Ideal Scaling Behavior: Experiments and Simulations, Y. Shao, M. G. Pala*, D. Esseni**, J. A. del Alamo. Massachusetts Institute of Technology, *Université Paris-Saclay, **University of Udine

We present the first demonstration of sub-10-nm diameter GaSb/InAs vertical nanowire Esaki diodes. High current densities at Esaki peak and at V_{ds} = 0.3 V are achieved, both with excellent current scaling behavior over nearly two decades of diameter. Quantum transport simulations show the key role of inelastic phonon scattering.

9:30 AM

32-2 High-Speed Ternary CMOS Inverter by Monolithic Integration of NbO_2 Threshold Switch with MOSFET, S. Heo, J. Lee, S. Lee, S. Lee, C. Lee, R. Baek, H. Hwang. Pohang University of Science and Technology

To realize a step-shaped ternary transistor capable of high-speed operation, NbO_2 Threshold switch (TS) device was integrated on the drain side of the conventional MOSFET. The fast switching speed(,63ps), excellent reliability, and moderate OFF-current level of NbO_2 TS device enable sub-10ns clock operations of ternary CMOS Inverter.

9:55 AM

32-3 Magnetic domain walls: from physics to devices (Invited), E. Raymenants, D. Wan, S. Couet, Y. Canvel, A. Thiam, D. Tsvetanova, L. Souriau, I. Asselberghs, R. Carpenter, N. Jossart, M. Manfrini, A. Vaysset, O. Bultynck, S. Van Beek, M. Heyns, D.E. Nikonov*, I.A. Young*, S. Ghosh**, L. Vila**, K. Garello**, S. Pizzini***, V.D. Nguyen, and I.P. Radu, imec, *Intel Corporation, **University Grenoble Alpes, CEA, CNRS, Grenoble INP, SPINTEC, ***University Grenoble Alpes, CNRS, Institut Néel

Domain wall (DW) motion offers a flexible design for novel computational schemes. This paper provides an overview of DW physics and its applications. Experimentally, we demonstrate a full electrical operation of nanoscale DW devices, fabricated on 300 mm wafer. Finally, the prospective of device geometries for logic functionalities is discussed.

10:20 AM

32-4 Functional Demonstration of a Fully Integrated Magneto-Electric Spin-Orbit Device, D. C. Vaz, C.-C. Lin*, J. Plombon*, W. Y. Choi, I. Groen, I. Arango, V. T. Pham, D. E. Nikonov*, H. Li*, P. Debashis*, S. B. Clendenning*, T. A. Gosavi*, V. Garcia**, S. Fusil**, M. Bibes**, Y.-L. Huang***, B. Prasad***, R. Ramesh***, F. Casanova, and I. A. Young*, nanoGUNE, *Intel Corporation, **CNRS/Thales, Université Paris-Saclay, ***University of California, Berkeley

We present the first experimental realization of a magneto-electric spin-orbit (MESO) logic device at room temperature. Two logic states are determined by the magnetization direction of a nanostructured CoFe element, which is switched by a magnetoelectric $BiFeO_3$ layer (WRITE) and detected through spin-to-charge conversion in a Pt element (READ).

10:45 AM

32-5 Narrow-Band Semiconductor Heterostructures for Efficient Spintronic Memory Device Applications, F. Xue, Y. Zhang*, Y. Zhang, L. Liao, L. Li, H. Ruan, L. Sun, J. Dong*, C. Tang, G. Yu*, Y. Yang, and X. Kou, Shanghai Tech University, *Institute of Physics

We report a new semiconductor-based heterostructure system InSb/CdTe in which effective band-bending and quantum confinement at the hetero-interface guarantee high carrier mobility and large spin-orbit coupling. The discovered gate-tunable Rashba effect and large spin-orbit torque (SOT) efficiency enable ultra-low switching current in the InSb/CdTe-based SOT-MRAM device prototype at room temperature.

Session 33: Memory Technology - Ferroelectric Memory

Wednesday, December 15, 1:30 PM
Grand Balroom A
Co-Chairs: Etienne Nowak, CEA-Leti
Sou-Chi Chang, Intel

1:35 PM

33-1 16kbit HfO_2:Si-based 1T-1C FeRAM Arrays Demonstrating High Performance Operation and Solder Reflow Compatibility, T. Francois, J. Coignus , A. Makosiej*, B. Giraud*, C. Carabasse, J. Barbot, S. Martin, N. Castellani, T. Magis, H. Grampeix, S. Van Duijn, C. Mounet, P. Chiquet**, U. Schroeder***, S. Slesazeck*** , T. Mikolajick***, E. Nowak, M. Bocquet**, N. Barrett^, F. Andrieu, L. Grenouillet, CEA, LETI, University Grenoble-Alpes, *CEA, LIST, University Grenoble-Alpes, **Aix Marseille University, Université de Toulon, ***NaMLab gGmbH, ^University Paris-Saclay

16kbit TiN/HfO_2:Si/TiN FeRAM arrays BEOL integrated are demonstrated at 130nm node. Zero bit failure is reported, memory window fully open down to 2.5V, capacitor area down to 0.16µm², switching speed down to 4ns and endurance up to 10^7 cycles. For the first time, HfO_2-based FeRAM solder reflow compatibility is demonstrated.

2:00 PM

33-2 FeRAM using Anti-ferroelectric Capacitors for High-speed and High-density Embedded Memory, S. -C. Chang, N. Haratipour, S. Shivaraman, C. Neumann, S. Atanasov, J. Peck, N. Kabir, I. -C. Tung, H. Liu, B. Krist, A. Oni, S. Sung, B. Doyle, G. Allen, C. Engel, A. Roy, T. Hoff, H. Li, F. Hamzaoglu, R. Bristol, M. Radosavljevic, B. Turkot, M. Metz, I. Young, J. Kavalieros, and U. Avci, Intel Corporation

This paper demonstrates industry-best hafnium-based FeRAM performance and reliability by showing (i) read/write speed scaled down to ~2ns, (ii) read/write endurance beyond 10^{12} cycles, and (iii) tail-bit

variations of scaled capacitors working at 4σ across a 300mm wafer at elevated temperature, by switching anti-ferroelectric (AFE) capacitors at -1.6V and 1.2V.

2:25:00 PM
33-3 Low Voltage and High Speed 1Xnm 1T1C FE-RAM with ultra thin 5nm HZO, M. Sung, K. Rho, J. Kim, J. Cheon, K. Choi, D. Kim, H. Em, G. Park, J. Woo, Y. Lee, J. Ko, M. Kim, G. Lee, S. W. Ryu, D. S. Sheen, Y. Joo, S. Kim, C. H. Cho, M.-H. Na, J. Kim, SK hynix

World-first 8Gb 1Xnm half-pitch FE-RAM with 5nm-thick ultra-thin HZO was fabricated, and operation was confirmed. We showed that memory operation is possible even at a low voltage of ±0.6V by using the pinched hysteresis. We measured the switching speed. 70% of the total polarization can be switched within 20ns.

2:50 PM
33-4 Embedding ferroelectric HfO_x in memory hierarchy: Material – defects – device entanglement (Invited), M. Pešić, B. Beltrando, Applied Materials Inc.

Ferroelectric (FE) HfO_x enabled multiple flavors of CMOS-compatible non-volatile memories (NVM) with potential to revolutionize technology landscape and enable in-memory computing (IMC). Starting from material and device results we successfully capture behavior of various FE based memories, analyze variability, reliability, and mechanisms to tame on path towards high-volume production.

3:15 PM
33-5 Atomic-scale characterization of defects generation during fatigue in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ films: vacancy generation and lattice dislocation, Y. Zheng, Y. Zheng, Z. Gao*, J. Yuan**, Y. Cheng, Q. Zhong, T. Xin, Y. Wang, C. Liu, Y. Huang, R. Huang, X. Miao**, K. Xue**, H. Lyu*, East China Normal University, *Chinese Academy of Sciences, **Huazhong University of Science and Technology

For the first time, we directly observed the lattice dislocation and monoclinic (m-) phase formation in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) films during fatigue, thorugh the spherical aberration (Cs)-corrected transmission electron microscopy (TEM) technique.

3:40 PM
33-6 Comprehensive Understanding of the HZO-based n/pFeFET Operation and Device Performance Enhancement Strategy, S. Kuk, S. Han*, B. Kim, S.-H. Baek*, J. Han*, S. Kim. Korea Advanced Institute of Science and Technology(KAIST), *Korea Institute of Science and Technology(KIST)

We report comprehensive understanding of HZO-based n/pFeFET operation using (double-pulsed) quasi-static CV and pulsed IV techniques, providing the true nonvolatile polarization and excess trap density. Also, we show new insight into the trapped charge in n/pFeFET. Finally, we propose a new erasing operation and physical models of the FeFET operation.

Session 34: Advanced Logic Technology - Future Technologies: 3D Integration and 2D Channel Materials
Wednesday, December 15, 1:30 PM
Grand Ballroom B
Co-Chairs: Dechao Guo, IBM
Gong Xiao, National University Singapore

1:35 PM

34-1 Opportunities in 3-D stacked CMOS transistors (Invited), M. Radosavljević, C.-Y. Huang, W. Rachmady, S.H. Seung, N. K. Thomas, G. Dewey, A. Agrawal, K. Owens, C. C. Kuo, C. J. Jezewski, R. Nahm, N. Briggs, T. A. Tronic, T. Michaelos, N. A. Kabir, B. Holybee, K. Jun, P. Morrow, A. Phan, S. Shivaraman, H. W. Then, V. Kapinus, M. K. Harper, P. D. Nguyen, K. L. Cheong, S. Ghose, K. Ganguly, C. Bomberger, J. M. Tan, M. Abd El Qader, A. A. Oni, P. Fischer, R. Bristol, M. Metz, S. B. Clendenning, B. Turkot, R. Schenker, M. J. Kobrinsky, J. Kavalieros, Intel

3-D stacked CMOS transistors offer an opportunity to enable further standard cell and SRAM scaling. We review recent developments and state-of-the-art demonstrations 3-D CMOS stacking by using either sequential approach or self-aligned approach. Both approaches demonstrate a well-balanced CMOS inverter built from transistors in top and bottom device layer.

2:00 PM
34-2 Scaling of double-gated WS_2 FETs to sub-5nm physical gate length fabricated in a 300mm FAB, Q. Smets, T. Schram, D. Verreck, D. Cott, B. Groven, Z. Ahmed, B. Kaczer, J. Mitard, X. Wu, S. Kundu, H. Mertens, D. Radisic, A. Thiam, W. Li, E. Dupuy, Z. Tao, K. Vandersmissen, T. Maurice, D. Lin, P. Morin, I. Asselberghs, I. Radu, imec

We present an analysis of gate length scaling of WS_2 transistors fully fabricated in a 300mm pilot line. I_{max}=100µA/µm is enabled by low side contact resistance. We demonstrate that switch-off can still be achieved with extremely scaled L_g=2nm, and we show better short-gate control with connected dual gate configuration.

2:25 PM
34-3 Enabling Hybrid Bonding on Intel Process, A.Elsherbini, K. Jun, R. Vreeland, W. Brezinski, H. K. Niazi, Y. Shi, Q. Yu, Z. Qian, J. Xu, S. Liff, J. Swan, J. Yao, P. Liu, C. Pelto, S. Rami, A. Balankutty, P. Fischer, B. Turkot, Intel Corporation

In this paper, we holistically discuss the recent design, wafer fabrication and die assembly changes needed to enable hybrid bonding interconnect (HBI) on Intel advanced logic process. We also show the design, fabrication, assembly and test results of active and passive test chips.

2:50 PM
34-4 First Demonstration of Heterogeneous IGZO/Si CFET Monolithic 3D Integration with Dual Workfunction Gate for Ultra Low-power SRAM and RF Applications, S.-W.Chang, T.-H. Lu** , C.-Y. Yang* , C.-J. Yeh* , M.-K. Huang* , C.-F. Meng** , P.-J. Chen*** , T.-H. Chang*** , Y.-S. Chang*** , J.- W. Jhu*** , T.-Z. Hong, C.-C. Ke^^, X.-R. Yu* , W.-H. Lu* , M. A. Baig, T.-C. Cho, P.-J. Sung, C.-J. Su, F.-K. Hsueh, B.-Y. Chen, H.-H. Hu**, C.-T. Wu, K.-L. Lin, W. C.-Y. Ma*** , D.-D. Lu* , K.-H. Kao* , Y.-J. Lee, C.-L. Lin^^, K.-P. Huang^^^, K.- M. Chen, Y. Li+, S. Samukawa++, T.-S. Chao^, G.-W. Huang, W.-F. Wu, W.-H. Lee*, J.-Y. Li+++, J.-M. Shieh, J.-H. Tarng^^, Y.-H. Wang*, W.-K. Yeh, Taiwan Semiconductor Research Institute, * National Cheng Kung University, ** National Taipei University of Tech., *** National Sun Yat-Sen University, ^National Yang Ming Chiao Tung University, ^^Feng Chia University, ^^^Industrial Technology Research Institute, +Nat. Yang Ming Chiao Tung University, ++Tohoku University, +++National Taiwan University

We demonstrate stacked heterogeneous dual-gate CFET inverters and 6T-SRAM with n-type α-IGZO channel and p-type polysilicon channel. The dual-workfunction gate structure with adjusted gate biasing allows adjusting nFET threshold voltage for CMOS and SRAM operation. High frequency and low power α-IGZO RF devices are fabricated simultaneously with the same process.

3:15 PM

34-5 Ge Single-Crystal-Island (Ge-SCI) Technique and BEOL Ge FinFET Switch Arrays on Top of Si Circuits for Monolithic 3D Voltage Regulators, H.T. Chung, B.J. Shih, C.C. Yang*, N.C. Lin, P.T. Huang, Y.P. Lan, K.F. Lai, W.T. Hsu, Y.M. Pan, Z.J. Hong, H.W. Hu, H.C. Cheng, C.H. Shen*, J.M. Shieh*, F.K. Hsueh*, B.Y. Chen*, D.C. Chang*, W.K. Yeh*, K.N. Chen, and C. Hu, National Yang Ming Chiao Tung University, *Taiwan Semiconductor Research Institute

A Ge Ge-SCI technique and M3D BEOL Ge FinFET were demonstrated for the first time. The functionality of the underlying Si standard logic cells and a 19-stage ring oscillator were unaffected by the Ge-SCI FinFET process. The M3D FIVR can achieve 1.6x response time improvement and 36% voltage droop reduction.

Session 35: Sensors, Mems, and Bioelectronics/Optoelectronics, Displays, and Imaging - Focus Session - Technologies for VR and Intelligence Sensors

Wednesday, December 15, 1:30 PM
Continental Ballrooms 1-3
Co-Chairs: Arvind Balijepalli, NIST
Chang-Won Lee, Hanbat National University

1:35 PM

35-1 Integrating Taste Technology with Audiovisual Media (Invited), H. Miyashita. Meiji University

This paper describes a mechanism for recording and reproducing taste similarly as humans record and reproduce audiovisual perception. The ion-phoretic and spray mixing methods are described for presenting taste; these methods are compared, and their prospects are discussed.

2:00 PM

35-2 A Miniature Electronic Nose for Breath Analysis (Invited) Z. Li, S.-H. Sie, J.-L. Lee, Y.-R. Chen, T.-I Chou, P.-C. Wu, Y.-T. Chuang*, Y.-T. Lin*, I-C. Chen**, C.-C. Lu**, Y.-Z. Juang*, S.-W. Chiu***, C.-C. Hsieh, M.-F. Chang and K.-T. Tang, National Tsing Hua University, *Taiwan Semiconductor Research Institute, **Industrial Technology Research Institute, ***Enosim Bio-tech Co., Ltd.

This paper proposes a miniature electronic nose for breath analysis. The conductive gas sensor array are micro-heating sensing devices deposited by nanomaterials. The sensor signal is processed by an AI edge accelerator based on computing-in-memory architecture, achieving an advanced system energy efficiency of 18.42 TOPs/W.

2:25 PM

35-3 Computational Imaging with Vision Sensors embedding In-pixel Processing (Invited), J.N.P. Martel, G. Wetzstein, Stanford University

Emerging vision sensors embedding in-pixel processing capabilities enable new ways to capture visual information. We review some of our work in designing new systems and algorithms using such vision sensors with applications in video-compressive imaging, high-dynamic range imaging, high-speed tracking, hyperspectral or light-field imaging.

2:50 PM

35-4 AI SoCs for AR/VR User-Interaction, (Invited) J. Ryu, D. Im, H.J. Yoo, Korea Advanced Institute of Science and Technology (KAIST)

3 Functional CIS and a UI processor are explained; ‘Eye-Mouse’ with gaze tracking, Event-driven ultra-low-power face detection, video-based HAR (HAR), and CNN-based HGR. AR/VR application processors are also explained with their architecture and featured functions. Future SoC will utilize more DNN functional blocks for PNN and fusion of more sensors.

3:15 PM
35-5 AR Glasses: Fatigue-free Optical Engines and Energy-efficient SLAM Sensors (Invited), H.-S. Lee, S. Kim, Y.-T. Kim, M. Jeon, W. Seo, D. Yang, C.-K. Lee, S. Moon, N. Kwon, J. Seo, J.-S. Chung, B. Shin, J. Pi, Y. Kim, V. Druzhin, G. Sung, and S. Hong, Samsung Electronics,

Augmented reality glasses are considered as a next generation mobile platform after smartphones. For consumer market penetration, many improvements in hardware and software are needed. We will talk about some of the most important part, the fatigue-free displays and the energy-efficient pose and localization sensors.

Session 36: Power Devices and Systems - Recent Advancements in Power Semiconductor Devices
Wednesday, December 15, 1:30 PM
Continental Ballroom 4
Co-Chairs: Sei-Hyung Ryu, Wolfspeed
Christina DiMarino, Virginia Tech

1:35 PM
36-1 Physics and Innovative Technologies in SiC Power Devices (Invited), T. Kimoto, M. Kaneko, K. Tachiki, K. Ito, R. Ishikawa, X. Chi, D. Stefanakis, T. Kobayashi, and H. Tanaka. Kyoto University

Mobility anisotropy, junction breakdown, and MOS interface of SiC is reviewed. A record electron mobility was attained along ,0001>. Small electron impact ionization coefficients along ,0001> give SiC artificially high critical electric field. By excluding oxidation of SiC, the interface state density was remarkably reduced, leading to two-fold mobility improvement.

2:00 PM
36-2 Toward High Performance 4H-SiC MOSFETs Using Low Temperature Annealing Process with Supercritical Fluid, M. Wang, M. Yang, W. Liu, S. Yang, C. Han, L. Geng, and Y. Hao*, Xi’an Jiaotong University, *Xidian University

An annealing process at 120°C with supercritical fluid N_2O is proved to be highly efficient in improving the quality of 4H-SiC/SiO_2 system. The field-effect mobility of the lateral 4H-SiC MOSFET on (0001) Si face is improved to 72.3 $cm^2/V\cdot s$, while the reliability of the dielectric layer is significantly enhanced.

2:25 PM
36-3 Gate Oxide Instability against a Wide Range of Negative Electric Field Stress of SiC MOSFETs, M. Noguchi, A. Koyama, T. Iwamatsu, H. Watanabe, and N. Miura, Mitsubishi Electric Corporation

For the first time, it is demonstrated for SiC MOSFETs that threshold voltage shift under NBTI testing can be universally described by gate injected charges. Additionally, the generation processes of interfacial traps are found to have two distinct phases. Finally, power-law model is presented to express lifetime under NBTI testing.

2:50 PM
36-4 Recent Progress in Silicon Devices for Ultra-High Power Applications (Invited), J. Vobecky, U. Vemulapati, T. Wikström, B. Boksteen, F. Dugal, T. Stiasny, C. Corvasce, Hitachi ABB Power Grids

Silicon high-voltage power devices dominate the power conversion necessary for generation, transmission and distribution grid systems. Recent advancements in the design and performance of Bipolar and BiMOS device concepts are presented to show how they can support the power conversion also in the coming years.

3:15 PM
36-5 1.2 kV GaN/SiC-based Hybrid High Electron Mobility Transistor with Non-destructive Breakdown, A. Nakajima, H. Hirai, Y. Miura, and S. Harada, National Institute of Advanced Industrial Science and Technology

A concept of GaN/SiC-based hybrid high electron mobility transistors (hyHEMTs) are proposed and demonstrated. A GaN-based HEMT and a SiC-based PN diode are monolithically integrated in the hyHEMT. The hyHEMTs have been fabricated on 4H-SiC substrates with a diameter of 100-mm. Measured non-destructive breakdown voltage was 1.27 kV.

3:40 PM
36-6 First Demonstration of RESURF and Superjunction β-Ga_2O_3 MOSFETs with p-NiO/n-Ga_2O_3 Junctions, Y. Wang, H. Gong*, X. Jia**, G. Han, J. Ye*, Y. Liu, H. Hu, X. Ou***, X. Ma, and Yue Hao, Xidian University, *Nanjing University, **Zhejiang Lab, ***Chinese Academy of Sciences

We for the first time demonstrate the conceptual superjunction (SJ) and reduced-surface-field (RESURF) β-Ga_2O_3 MOSFETs, which exhibit significantly improved breakdown voltage (V_{br}) as compared to the control devices without p-NiO. The fabricated SJ-MOSFET achieves the 2.42 and 4.86 times higher Vbr and PFOM, respectively, compared to the control transistors.

Session 37: Emerging Device and Compute Technology - Two-Dimensional and Oxide Semiconductors: Optimization and Applications
Wednesday, December 15, 1:30 PM
Continental Ballroom 5
Co-Chairs: Eric Pop, Stanford University
Suman Datta, University of Notre Dame

1:35 PM
37-1 Superior electrostatic control in uniform monolayer MoS_2 scaled transistors via in-situ surface smoothening, Y. Shi, B. Groven, Q. Smets, S. Sutar, S. Banerjee, H. Medina, X. Wu, C. Huyghebaert, S. Brems, D. Lin, P. Morin, M. Caymax, I. Asselberghs, I. Radu. IMEC

An in-situ surface smoothening method is designed to precisely control the monolayer thickness of MOCVD MoS_2. By analyzing >15000 devices, smooth monolayer MoS_2 scaled transistors show improved electrostatic control with good off-state current, $I_{ON}/I_{OFF}>10^7$, median SS_{min} of 68mV/dec, and low V_T variation, which is on par with advanced Si FinFETs.

2:00 PM
37-2 Contact Engineering for High-Performance N-Type 2D Semiconductor Transistors (Invited), Y. Lin, P.-C. Shen, C. Su*, A.-S. Chou**, T. Wu**, C.-C. Cheng**, J.-H. Park, M.-H. Chiu, A.-Y. Lu, H.-L. Tang, M. M. Tavakoli, G. Pitner**, X. Ji, C. McGahan^, X. Wang^^, Z. Cai, N. Mao, J. Wang, Y. Wang^^^, W. Tisdale, X. Ling^^, K. E. Aidala^, V. Tung^^^, J. Li1 , A. Zettl, C.-I. Wu***, Jing Guo+, H. Wang**, J. Bokor*, T. Palacios, L.-J. Li** , J. Kong, Massachusetts Institute of Technology, *University of California, Berkeley, **TSMC, ***National Taiwan University, ^Mount Holyoke College, ^^Boston University, ^^^Tsinghua University, +University of Florida

2D semiconductors are promising channel materials, but a major bottleneck is the Schottky barrier and the large contact resistance, due to the gap-state pinning effects. In this paper, we review the recent progress on the elimination of these and the resulting improved contact resistance and on-state current.

2:25 PM
37-3 High-Performance CVD MoS_2 Transistors with Self-Aligned Top-Gate and Bi Contact, W. Li, D. Fan, L. Shao, F. Huang, L. Liang, T. Li, Y. Xu, X. Tu, P. Wang, Z. Yu, Y. Shi, H. Qiu, and X. Wang, Nanjing University

We fabricated high-performance FETs featuring CVD MoS_2 channel, self-aligned top-gate, and semi-metallic Bi Ohmic contact. For the first time, Bi was used in the top-gate 2D FET as source/drain contacts. The demonstrated I_{ON} of 680μA/μm at 60nm L_g and R_C of 280Ω·μm are the best-reported values among top-gate 2D FETs.

2:50 PM
37-4 Short-Channel Double-Gate FETs with Atomically Precise Graphene Nanoribbons, Z. Mutlu, Y. Lin, G. B. Barin*, Z. Zhang**, G. Pitner***, S. Wang*, R. Darawish*, M. Di Giovannantonio*, H. Wang***, J. Cai***, M. Passlack***, C. H. Diaz***, A. Narita^, K. Müllen^, F. R. Fischer, P. Bandaru**, A. C. Kummel**, P. Ruffieux*, R. Fasel*, and J. Bokor, University of California, Berkeley, *Swiss Federal Laboratories for Materials Science and Technology, **University of California, San Diego, ***Taiwan Semiconductor Manufacturing Company, ^The Max Planck Institute for Polymer Research

We evaluate the performance of bottom-up synthesized graphene nanoribbons as transistor channels. Transistor structures include back-and double-gate FETs. Devices exhibit excellent switching and on-state current performance. Double-gate offers superior electrostatic control. Challenges and opportunities of graphene nanoribbons as channels are discussed, together with possible further improvements, for high-performance logic applications.

3:15 PM
37-5 Source/Drain Engineering by Tantalum Nitride (TaN_x) Electrode for Boosting OSFET Performance, N. Okuno, Y. Sato, Y. Jimbo, H. Honda, M. Kurata, M. Wakuda, H. Kunitake, M. Kobayashi*, and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd., *The University of Tokyo

For scaling down of oxide semiconductor FETs, the choice of source/drain electrode material is crucial. We have achieved CAAC-IGZO FETs with high performance and reliable electrical characteristics by adopting tantalum nitride (TaN_x). Owing to the composition ratio adjustment and strong compressive stress of TaN_x, the FETs exhibit high on-current.

3:40 PM
37-6 Computational Associative Memory Based on Monolithically Integrated Metal-Oxide Thin Film Transistors for Update-Frequent Search Applications, Z. Zhao, J. Gomez*, H. Ye*, M. Imani**, X. Yin***, S. Deng, B. Melanson, J. Zhang, X. Gong^^, A. Abusleme^^^, S. Datta*, and K. Ni, Rochester Institute of Technology, *University of Notre Dame, **University of California, ^Zhejiang University, ^^National University of Singapore, ^^^Pontificia Universidad Católica de Chile

Monolithic 3D TCAM designs based on TFTs that can achieve high density and excellent write performance for update-frequent search applications are demonstrated. Logic-compatible write voltage (,1.5V), ,20ns write latency, $>10^{10}$ endurance are achieved. Up to 14x/35x improvement in speed/energy over GPU in accelerating the K-Means clustering algorithm.

Session 38: Emerging Device and Compute Technology/Optoelectronics, Displays, and Imaging - Focus Session - Topological Materials, Devices, and Systems
Wednesday, December 15, 1:30 PM
Continental Ballroom 6
Co-Chairs: Jean Anne Incorvia, University of Texas Austin
Chang-Won Lee, Hanbat National University

1:35 PM
38-1 Spin-charge interconversion in topological insulators and topological semimetals for spin-orbit torque devices (Invited), N. Samarth, W. Yanez, and Y. Ou, The Pennsylvania State University

This talk provides an overview of experimental studies of spin-charge interconversion in heterostructures that combine topological insulators (such as Bi_2Se_3) and topological semimetals (such as Cd_3As_2) with metallic and insulating ferromagnets, highlighting the opportunities and challenges for exploiting these materials in spin-orbit torque devices.

2:00 PM
38-2 Proposal for a Negative Capacitance Topological Quantum Field-Effect Transistor (Invited), M.S. Fuhrer, M.T. Edmonds, D. Culcer, M. Nadeem, X. Wang, N. Medhekar, Y. Yin, J.H Cole, ARC Centre of Excellence in Future Low-Energy Electronics Technologies

A topological quantum field effect transistor (TQFET) uses electric field to switch from topological insulator to conventional insulator ("off"). We propose a negative capacitance TQFET which uses a ferroelectric to amplify the electric field and potentially achieve low switching voltages and energies. Materials challenges for realizing the NC-TQFET are discussed.

2:25 PM
38-3 Essential Design Criteria for Topological Electronics and Spintronics (Invited), G. J. de Coster and M. J. Gilbert*, Army Research Laboratory, *University of Illinois at Urbana-Champaign

We elucidate the required design specifications placed on magnetic and topological materials (TM) to realize the effective transfer of magnetization from the magnetic material into the underlying TM with the goal of maximizing the magnitude of the magnetism in the TM to enable the possibility of devices operating at room-temperature.

2:50 PM
38-4 Topological Semimetals for Electronic Devices (Invited), A. Rashidi, O. F. Shoron, Manik Goyal, David A. Kealhofer, S. Stemmer, University of California, Santa Barbara

Topological materials such as Cd_3As_2 feature exceptionally high Fermi velocities, high charge densities and can be integrated with semiconductors, making them attractive for high frequency devices. We discuss a MOSFET that uses Cd_3As_2 as the channel and a HET that uses Cd_3As_2 as the base.

3:15 PM
38-5 Semiconductor Topological Nanophotonics (Invited), Y. Ota, Y. Arakawa*, S. Iwamoto*, Keio University, *Nanoquine

We discuss possible applications of topological photonics to photonic integrated circuit technologies. We design nanophotonic elements based on topological edge states and apply them to compact semiconductor

lasers and waveguides. Such topological photonic devices are known to be immune to fabrication imperfections and therefore suitable to build robust optical circuitry.

3:40 PM
38-6 Symmetry-Enabled New Microlasers (Invited), L. Feng, Z. Zhang, and X. Qiao, University of Pennsylvania

Explorations of symmetry and topology on a photonic platform not only deepen our understanding of fundamental physics, but also enable novel material properties to facilitate technological breakthroughs for photonic applications. By harnessing new symmetries, we demonstrated orbital angular momentum (OAM) microlasers and higher-dimensional microlaser phaser arrays.

Session 39: Reliability of Systems and DEVICES - Reliability in RF/Power/Security Applications
Wednesday, December 15, 1:30 PM
Continental Ballrooms 7-9
Co-Chairs: Byoung Min, Global Foundries
Andreas Kerber, ON Semiconductor

1:35 PM
39-1 From reliability to security of devices (Invited), A. Tria, J. Fournier. CEA, LETI, University Grenoble Alpes,

Reliability issues constitute a major concern for electronic devices. With the emergence of new generations of integrated circuits and democratization of critical IoT applications, new challenges have to be met to address those security issues.In this paper, we provide an overview of how reliability issues are linked to security issues.

2:00 PM
39-2 Unified 0.75pJ/Bit TRNG and Attack Resilient 2F^2/Bit PUF for Robust Hardware Security Solutions with 4-layer Stacking 3D NbO$_x$ Threshold Switching Array, Q. Ding, H. Jiang*, J. Li**, P. Chen, C. Liu, Y. Zhao, J. Yu, Y. Ding, Q. Luo, J. Yang, H. Lv, and M. Liu, Institute of Microelectronics of Chinese Academy of Sciences, *Zhejiang Lab

For the first time, a unified in-memory TRNG and PUF utilizing the dynamic threshold switching (TS) variations and static leakage current mismatch is proposed and demonstrated based on a 4-layer 3D NbO$_X$ array.

2:25 PM
39-3 65nm RFSOI Power Amplifier Transistor Ageing at mmW frequencies, 14 GHz and 28 GHz, A. Divay, J. Forest*,V. Knopik*, J. Hai*, N. Revil*, J. Antonijevic*, A. Michard*, F. Cacho*, E. Vincent*, F. Gaillard, X. Garros, CEA-LETI, Université Grenoble Alpes, *ST Microelectronics

RF performance and reliability of Stand-Alone MOS devices and stacked Power Amplifier cells have been investigated. The Stand-Alone has a very good immunity against TDDB when operating under most of 5G modulations signals and hot carrier ageing in DC and RF large signal is modelled considering V_T and R_d drift.

2:50 PM
39-4 Thorough Investigation of Low Frequency Noise Mechanisms in AlGaN/GaN and Al2O3/GaN HEMTs, R. Kom Kammeugne, C. Theodorou*, C. Leroux, X. Mescot*, L. Vauche, R. Gwoziecki, S. Becu, M. Charles, E. Bano* and G. Ghibaudo*, CEA-LETI, University Grenoble Alpes, *University Grenoble Alpes, University Savoie Mont Blanc, CNRS, Grenoble INP, IMEP-LAHC

AlGaN/GaN and Al2O3/GaN interface quality on GaN MIS-HEMT are investigated using low frequency noise measurements (LFN). LFN has a 1/f-like behaviour related to border traps. Extracted traps density are found better than previously reported GaN data and close to Si-MOSFET ones. Finally, a new model including 2DEG noise is proposed.

3:15 PM
39-5 ESD HBM Discharge Model in RF GaN-on-Si (MIS)HEMTs, W.-M. Wu, S.-H. Chen, A. Sibaja-Hernandez, S. Yadav, U. Peralagu, H. Yu, A. Alian, V. Putcha, B. Parvais, G. Groeseneken, M.-D. Ker, and N. Collaert, imec

Mis-correlation between TLP failure current and HBM ESD robustness has been observed in GaN (MIS)HEMTs. Using transient HBM IV characteristics, a novel discharge model is proposed to well explain the transient discharge mechanism. The TCAD and SPICE simulations further indicate this mis-correlation is attributed to 2DEG channel resistance modulation.

Session 40: Emerging Device and Compute Technology - Cryogenic, Exploratory and Quantum Computing Devices
Wednesday, December 15, 1:30 PM
Imperial Ballroom A
Co-Chairs: Kirsten Moselund, IBM Zurich
Jan Hoentschel, Globalfoundries

1:35 PM
40-1 Pseudo-Static 1T Capacitorless DRAM using 22nm FDSOI for Cryogenic Cache Memory, W. Chakraborty, R. Saligram*, A. Gupta, M. San Jose, K. A. Aabrar, S. Dutta, A. Khanna, A. Raychowdhury* and S. Datta, University of Notre Dame, *Georgia Institute of Technology

We experimentally demonstrate, for the first time, pseudo-static random access memory operation of a 1T Capacitorless Floating Body DRAM using 22nm FDSOI transistor, down to 4.8K, for cryogenic cache memory. We demonstrate a 1T Cryo-DRAM that exhibit record high sensing current and sense margin, pseudo-static retention characteristics >10^5sec

2:00 PM
40-2 Overcoming the Accuracy vs. Performance Trade-off in Oscillator Ising Machines, A. Mallick, M. K. Bashar, D. S. Truesdell, B. H. Calhoun*, N. Shukla, University of Virginia, Charlottesville

We demonstrate a 600 CMOS-oscillator-based Ising machine with >29000 coupling-elements. Using this platform, we reveal the fundamental trade-off in solution-accuracy vs. compute-time for solving NP-hard MaxCut. Subsequently, we develop a hybrid approach to overcome this trade-off, and show 3-100x reduction in compute-time compared to digital-algorithms while yielding the same solution-quality.

2:25 PM
40-3 Computing with Invertible Logic: Combinatorial Optimization with Probabilistic Bits, (Invited) N. A. Aadit, A. Grimaldi*, M. Carpentieri**, L. Theogarajan, G. Finocchio*, K. Y. Camsari, University of California Santa Barbara, *University of Messina, ** Politecnico di Bari

Probabilistic Computing with p-bits has been a strong contender for solving combinatorial optimization problems (COP) with dedicated hardware. Here, we present the latest results on solving COPs with interconnected p-bits. Using simulated annealing and parallel tempering, we show how p-computers solve Boolean satisfiability and integer factorization up to 25-bit semiprimes.

2:50 PM

40-4 A new FDSOI spin qubit platform with 40nm effective control pitch, T. Bédécarrats, B. Cardoso Paz*, B. Martinez Diaz**, H. Niebojewski, B. Bertrand , N. Rambal, C. Comboroure, A. Sarrazin, F. Boulard, E. Guyez, J.-M. Hartmann, Y. Morand, A. Magalhaes-Lucas, E. Nowak, E. Catapano, M. Cassé, M. Urdampilleta*, Y.-M. Niquet**, F. Gaillard, S. De Franceschi**, T. Meunier*, M. Vinet, Université Grenoble Alpes and CEA-Leti, *CNRS Institut Néel, **CEA-Irig

We present a novel Si quantum device integration that halves the effective gate pitch and provides full controllability in 1D FDSOI QD arrays. Advantages of this architecture are explored through numerical simulations. Functionality of the fabricated structure is validated via 300K statistical characterization. Tunnel-coupling control is demonstrated at cryogenic temperature.

3:15 PM

40-5 High-Performance 300mm Integrated Superconducting Resonators for Quantum Computing Applications, M. Mongillo, A. Potočnik, J. Verjauw, F.A. Mohiyaddin, T. Ivanov, R, Acharya, X. Piao, D. Perez Lozano, D. Wan, A.Pacco, J. Jussot, L. Souriau, A. M. Vadiraj, J. Swerts, S Couet, L. Goux, B. Govoreanu, and Iuliana P. Radu, Imec

We report on the electrical performance of integrated superconducting microwave resonators at millikelvin temperatures. Several resonator materials were successfully integrated into a 300mm process with record-high quality factors. This work paves the way towards a robust development platform for superconducting qubit technologies.

3:40 PM

40-6 Fine-Pitch (≤10 µm) Nb-based Superconducting Silicon Interconnect Fabric for Large-Scale Quantum System Application, Y.-T. Yang, C. Hu, P. Zhang, H. Ren, N. Ni, K. L. Wang, and S. S. Iyer, University of California, Los Angeles (UCLA)

For large-scale quantum computing, a System-on-Wafer high-density I/O (>10000 per mm^2) assembly scheme is proposed. Qubits can be heterogeneously integrated with superconducting control electronics through the fine-pitch Au interlayer on the Superconducting Silicon Interconnect Fabric. This platform is experimentally validated. Potential advantages include few-nanosecond control/readout cycles and 10^{-4} error rate.