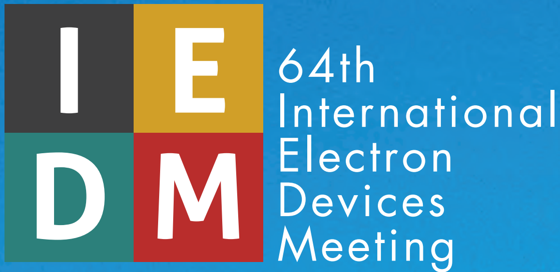

2018 IEDM Conference Proceedings

Device Breakthroughs from Quantum to 5G and Beyond

For More Information
IEDM Online: ieee-iedm.org

Social Networks:
ieee-iedm.org/social-media

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Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

Digital & Social Media

- LinkedIn: https://www.linkedin.com/groups/7475096/
- Twitter: https://twitter.com/ieee_iedm
- Facebook: https://www.facebook.com/IEEE.IEDM
- YouTube: https://www.youtube.com/channel/UC9X-8YPHtsy3SMQwU0yZdTg
- Wikipedia: https://en.wikipedia.org/wiki/International_Electron_Devices_Meeting

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Topics of Interest

CIRCUIT AND DEVICE INTERACTION (CDI)

Papers are solicited in the areas of CMOS platform technology, circuit design challenges at advanced nodes, and device technology co-optimization solutions. Platform technologies include beyond Si channel such as SiGe/Ge, and advanced device technologies such as Gate-all-around Nanowire and Stacked Nanosheet CMOS technologies are of strong interest. Topics also include digital and analog device and circuit performance and scaling issues, power-performance-area analysis, and architectural implications of interconnect technology and performance. Submission of papers discussing interactions between advanced device technology and design issues such as variability, aging, power constraints, physical layout effects and design is encouraged. Papers addressing stacked and monolithic 3D integration, interconnect bottleneck and design challenges are solicited. Emerging circuit design and technology concepts supporting new computing models such as processing-in-memory, machine learning acceleration, neuromorphic computing, and other non-von Neumann computing approaches are of interest.

CHARACTERIZATION, RELIABILITY and YIELD (CRY)

Papers are solicited in all areas of electrical and physical characterization, reliability evaluation and yield analysis of transistors, interconnects and circuits. Specific reliability topics include, for FEOL: transistor degradation due to hot carriers and bias temperature instabilities; dielectric wear-out and breakdown; self-heating effects; process charging damage; latch-up and ESD; soft error mechanisms in logic and memories and error correction techniques; noise and mismatch behavior. For MEOL/BEOL topics include: electromigration failure of contacts and interconnects; breakdown of BEOL dielectrics and MEOL spacers; mechanical stress-related mechanisms;thermal management; chip-package interaction. Of particular interest are investigations of degradation mechanisms for: resistive devices; emerging memories; III-V power devices, and More-than-Moore applications. Also solicited are papers discussing variability / reliability interactions and failure analysis techniques.

COMPOUND SEMICONDUCTOR AND HIGH SPEED DEVICES (CHS)

Papers are solicited in the areas of compound semiconductor electronic devices and high-speed device technologies based on GaAs, InGaAs, InP, GaN, InAlN, Si, SiGe, Antimonides and their related alloys. Devices of interest include III-V MOSFETs, ballistic devices, HBTs (III-V and group IV) and HEMTs, RF/microwave/millimeter-wave/THz devices, SAW/BAW devices, low noise amplifiers, RF power amplifiers, RF and millimeter-wave switches and filters, and active and passive electron devices for analog applications. Topics include device physics, design, modeling, reliability and manufacturing processes.

MEMORY TECHNOLOGY (MT)

Papers are solicited covering all memory technology topics, including storage-class and embedded memories, as well as in-memory and neuromorphic computing applications. Topics span from novel cell concepts to fully integrated memories, from prototyping to manufacturing issues and performance. Specific areas of interest include both conventional and novel memory cells including ReRAM, STT-MRAM, PCRAM, FeRAM, 3D NAND, crosspoint and selectors, organic memory and NEMS-based devices, including their design and scaling, processing, reliability, and modeling. Novel concepts and demonstrations that enhance memory properties or apply to neural computing paradigms are of interest. Higher level topics include 3D architectures, novel read/program/erase schemes, solid state drive (SSD) applications, novel hierarchies and architectures for memory-centric systems, security, computing-in-memory and non-volatile memory-enabled emerging logic applications.

MODELING and SIMULATION (MS)

Papers are solicited in the areas of analytical, numerical, and statistical approaches to model electronic, optical, hybrid devices including sensors, and their isolation and interconnects. Topics include physical and compact models for logic and memory devices (e.g. steep-slope devices, RRAM, CBRAM) and interconnects, modeling and emulation of fabrication processes and equipment, material modeling, parameter extraction, compact models for advanced technologies and novel devices, performance evaluation, reliability, variability, and benchmarking methodologies. Other topics include novel computing approaches

(e.g. neuromorphic computing) and modeling of interactions between process, device, circuit, and packaging. Submissions should advance the art of modeling and simulation or apply existing techniques to gain new device insights.

NANO DEVICE TECHNOLOGY (NDT)

Papers are solicited on novel or emerging solid state nanoelectronic devices and concepts. This includes devices based on novel transport mechanisms such as tunnel FETs, negative capacitance FETs, topological insulators, phase transitions, quantum effects, and non-von Neumann devices. Non-charge-based logic, magnetic logic, spintronics, plasmonics and quantum computing are also of interest. Furthermore, nanoelectronic devices based on low-dimensional systems are encouraged, including 2D materials, nanowires, nanotubes and quantum dots. Subsets of key topics include electron device physics, new device applications, technology scaling and integration issues, as well as innovative transistor structures. Papers in NDT focus primarily on device physics and unique concepts; more mature "platform candidate" papers should be submitted to CDI. Reliability assessment of emerging devices are also solicited here, while that for more mature technologies should be submitted to CRY.

OPTOELECTRONICS, DISPLAYS, and IMAGERS (ODI)

Papers are solicited on devices, structures, and integration for optoelectronics, displays, and imaging systems. Optoelectronics include photonic bandgap structures, light sources, polarization and wavelength manipulators, high speed photodetectors, as well as large scale heterogeneous integration of electronic and photonic circuits and optical interconnects. Papers on quantum photonics for computation, sensing and encryption are also of interest. Displays and imagers include CMOS imagers, high speed and high time resolution imagers, CCDs, TFTs, organic, amorphous, and polycrystalline devices, as well as emissive and reflective displays. Papers addressing flexible and/or stretchable electronics, printed electronics, stacked image sensors with Si or other photosensitive materials, organic and inorganic displays, and covering new technology trends in imagers and displays are encouraged.

POWER DEVICES (PD)

Papers are solicited on discrete and integrated power devices and modules using Si, diamond, and compound semiconductors. Papers exploring the system-level impact of power devices are also of interest. Topics of interest include power devices (FETs, superjunction devices, IGBTs, etc.), and materials (Si, SiC, GaN, Diamond, GaAs, AlN, Ga2O3, etc.), integrated passives (high Q inductors), manufacturing processes, device design, modeling, physics, and reliability. Devices targeting the full range of power and power conversion applications, including hybrid and electric vehicles, power supplies for computer and telecom and data centers, motor drives, utility and grid control, and wireless power transfer, are of interest besides fundamental studies on doping, interface state densities and device reliability for power switches.

PROCESS and MANUFACTURING TECHNOLOGY (PMT)

Papers are requested on innovations in individual process modules, process integration schemes and process control techniques that improve device or circuit performance or enable new functionality. Examples of process topics include substrate and isolation technologies; integration of heterogeneous channel materials; EUV lithography, deposition, planarization, etch and self-assembly techniques; novel dielectrics and metal electrodes for transistor gate stacks; shallow junctions; advanced metals, barriers and dielectrics for interconnections; contact and via processes; integration considerations for multi-level interconnects and for enhanced scaling techniques; additive manufacturing for microelectronics and emerging process modules. Further requested topics include photonics, 3D and advanced packaging integration; BEOL compatible transistors and memory devices. Examples of process control topics include defect detection as well as novel techniques for variability reduction and for enhancing process control and stability.

SENSORS, MEMS, and BioMEMS (SMB)

Papers are solicited in the area of sensors, micro/nano-electromechanical systems (MEMS and NEMS), microfluidics and BioMEMS, with particular emphasis on new device concepts, integrated implementations, CMOS co-integration, flexible devices and multi-sensors on a chip for wearable and IoT applications. Sensors area includes chemical, molecular and biological detection based on electrical, electrochemical, mechanical and optical principles. Topics of interest in the MEMS area include actuators, physical sensors, resonators, integrated inertial measurement units, RF MEMS, micro-optical and optomechanical devices, micro power generators, devices for energy harvesting and on-chip energy storage as well as micro/nanofluidics for thermal management. BioMEMS area covers organic-inorganic hybrid devices, bio-electronic interface, integrated biomedical sensing and implantable MEMS.

Program

See the Program Download for all abstracts and speaker bios.

Tutorials

The tutorials are in their eight year and are 90 minute stand alone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields, and facilitate understanding of the technical sessions. In contrast, the traditional short courses are intensive full-day events focused on a single technical topic.

The tutorial sessions will take place on Saturday, December 1st. Three tutorials are given in parallel in two time slots, at 2:45 p.m. and 4:30 p.m. respectively.

Tutorials 2:45 pm – 4:15 p.m.

- Emerging Device Technologies for Neuromorphic Computing, Damien Querlioz, CNRS
- Reliability Challenges in Advanced Technologies, Ryan Lu, TSMC
- Quantum Computing Primer, Mark B. Ritter, IBM

Tutorials 4:30 pm – 6:00 pm

- Design-technology Co-optimization at RF and mmWave, Bertand Parvais, Imec
- STT-MRAM Design and Device Requirement, Shinichiro Shiratake, Toshiba Memory
- Power Transistors in Integrated BCD Technologies, Hal Edwards, Texas Instruments

Short Courses

IEDM will offer two, full-day short courses with in-depth coverage of highly relevant topics from world experts. Advance registration is recommended. Details on the short courses will be published later this year.

Sunday, December 2, 2018, 9:00 a.m. – 5:30 p.m.

Short Course 1: Scaling Survival Guide in the More than Moore Era

Course Organizer: Jin Cai, TSMC

- Extreme UV Lithography: The Road to HVM and Beyond, Anthony Yen, ASML
- MOSFET Scaling Knobs (GAA, NCFET…) and Future Alternatives, Witek Maszara
- Overcoming Variation Challenges, Sivakumar Mudanai, Intel
- Embedded Memory: Present Status, and Emerging Architecture and Technology for Future Applications, Eric Wang, TSMC
- Advanced Packaging: the Next Frontier for Moore's "Law", Subramanian Iyer, UCLA
- 3D Integration for Density and Functionality, Julien Ryckaert, imec

Short Course 2: It's All About Memory, Not Logic!!!

Course Organizer: Nirmal Ramaswamy, Micron

- DRAM : Its Challenging History and Future, Dong Soo Woo, Samsung
- 3D Flash Memories: Overview of Cell Structures, Operations and Scaling Challenges, Makoto Fujiwara, Toshiba
- Emerging Memories including Cross-Point, Opportunities and Challenges, Kiran Pangal, Intel
- Memory Reliability, Qualification and their Relation to System Level Reliability Strategies, Todd Marquart, Micron
- Future of the Packaging Technologies for HBM, Nick (Namseog) Kim, SK Hynix
- Processing in Memory (PIM): Performance and Thermal Challenges and Opportunities, Mircea Stan, University of Virginia

Plenary Session

Welcome and Awards

General Chair: Ken Rim, Qualcomm

Plenary Papers

Technical Program Chair: Mariko Takayangi, Toshiba

1.1 4th Industrial Revolution and Foundry: Challenges and Opportunities (Invited), ES Jung, President of Foundry Business, Samsung Electronics

1.2 Venturing Electronics into Unknown Grounds (Invited), Gerhard P. Fettweiss, TU Dresden Vodafone Chair Mobile Communications System

1.3 Future Computing for AI (Invited), Jeff Welser, Vice President and Lab Director, IBM Research -Almaden

Focus Sessions

As every year, IEDM 2018 will offer Special Focus Sessions on emerging topics with invited talks from world experts to highlight the latest developments.

Session 5: Focus Session – Characterization, Reliability, and Yield — Interconnects to Enable Continued Scaling

Session 6: Focus Session – Nano Device Technology — Quantum Computing Devices

Session 14: Focus Session – Compund Semiconductor and High Speed Devices — Future Technologies Towards Wireless Communications: 5G and Beyond

Session 19: Focus Session – Compound Semiconductor and High Speed Devices — Challenges for Wide Bandgap Device Adoption in Power Electronics

Career Session

Tuesday, December 4, 12:15– 2:00 p.m.

Grand Ballroom B

Speakers:

John Chen, VP of Technology and Foundry Management, nVidia

Veena Misra, Distinguished Professor, North Carolina State University

Technical Program

See the Program Download for all abstracts and speaker bios.

Monday – December 9

- Session 1 — Plenary Session

Monday – 1:30 pm – 5:00 pm

- Session 2: Memory Technology — Charge Based Memories
- Session 3: Circuit and Device Interaction — Device and Algorithm Co-design for Neuromorphic and In-memory Computing
- Session 4: Sensors, MEMS, and BioMEMS — Micro and Nano Electromechanical Systems
- Session 5: Focus Session – Characterization, Reliability, and Yield — Interconnects to Enable Continued Scaling
- Session 6: Focus Session – Nano Device Technology — Quantum Computing Devices

- Session 7: Process and Manufacturing Technology — 3D Integration and Memory Technologies
- Session 8: Power Devices/ Compound Semiconductor and High-Speed Devices — Advances in Silicon Carbide and Gallium Oxide Silicon Power Devices
- Session 9: Modeling and Simulation — Modeling and Simulation of Negative Capacitance Transistors
- Session 10: Optoelectronics, Displays, and Imagers — Image Sensors

Monday 6:30 pm – 8:00 pm

- Session 11: Process and Manufacturing Technology — Material and Processes for Advanced Silicon Technologies
- Session 12: Sensors, MEMS, and BioMEMS — Integrated Ion and Gas Sensors
- Session 13: Nano Device Technology — Nano-Devices for Low-Power Technologies Session 4 NDT
- Session 14: Focus Session – Compund Semiconductor and High Speed Devices — Future Technologies Towards Wireless Communications: 5G and Beyond
- Session 15: Circuit and Device Interaction — Emerging Devices for Neural Network and IoT
- Session 16: Modeling and Simulation — Advanced Modeling of ferroelectric materials and devices
- Session 17: Characterization, Reliability, and Yield — Innovative Characterizations

Tuesday – 2:15 pm – 5:30 pm

- Session 18: Circuit and Device Interaction — Embedded Memory at Advanced CMOS Nodes
- Session 19: Focus Session – Power Devices — Challenges for Wide Bandgap Device Adoption in Power Electronics
- Session 20: Memory Technology — RRAM for Neuromorphic Applications
- Session 21: Process and Manufacturing Technology — Advanced Gate All Around Process
- Session 22: Nano Device Technology — 2D CMOS and Memory Devices
- Session 23: Optoelectronics, Displays, and Imagers — Silicon Photonics
- Session 24: Modeling and Simulation — 2D Materials, Modeling, and the Optimization of Beta-Ga2O3 Power Devices
- Session 25: Characterization, Reliability, and Yield — Emerging Memory Reliability

Tuesday – 8:00 pm – 10:00 pm

- Session 26 – IEDM Evening Panel Session

Wednesday – 9:00 am – 12:00 pm

- Session 27: Memory Technology — MRAM & PCRAM
- Session 28: Circuit and Device Interaction — Advanced CMOS Technology for Computing in the Nanoscale Era
- Session 29: Sensors, MEMS, and BioMEMS — Biosensors and Neural Interfaces
- Session 30: Power Devices/Compound Semiconductor and High-Speed Devices Committee — GaN Power Devices
- Session 31: Nano Device Technology — NCFET Physics and Devices
- Session 32: Optoelectronics, Displays, and Imagers — CMOS Photodetectors
- Session 33: Modeling and Simulation — Device, Process and Reliability Modeling
- Session 34: Characterization, Reliability, and Yield — Advanced Technology Reliability

Wednesday – 1:30 pm – 4:05 pm

- Session 35: Process and Manufacturing Technology — Advanced Channel and Contact Technologies
- Session 36: Nano Device Technology — Spintronic Devices and Applications
- Session 37: Memory Technology — 1S1R Arrays and Select Devices
- Session 38: Optoelectronics, Displays, and Imagers — Displays, TFTs, and Optical Synapses
- Session 39: Compound Semiconductor and High Speed Devices — High Performance III-V Devices and Technology Towards 5G
- Session 40: Modeling and Simulation — Simulation and Modeling of Advanced Process and Emerging Memory

SRC Student Showcase Poster Session

SRC is hosting a student research showcase at IEDM on Tuesday, December 4, 2018 from 2:00pm – 4:00pm in the Golden Gate Room. This all-student poster session highlights fundamental semiconductor research in universities worldwide, sponsored by industry members and government agencies. Semiconductor Research Corporation (SRC) drives advances in materials, devices, processing, metrology, and modeling that are all well-aligned to IEDM's future. This event is organized by SRC and appears as a special poster session scheduled for Tuesday afternoon in the IEDM program . It will be a great opportunity to engage with student researchers and their budding ideas.

Exhibits & Exhibit Events

IEDM 2018 will host an Exhibits area during the conference where you can learn more about the latest products and publications. This will be open in the Golden Gate Ballroom during the conference from Monday 12:00 pm, through Wednesday 12:00 pm. Stop by any time during the exhibition open hours to browse the booths and enjoy complementary coffee. The Exhibition will be open to all IEDM attendees as well as qualified Exhibit Only participants.

Exhibition Opening Times

Monday: 12:00 p.m. – 4:00 p.m.

Tuesday: 8:00 a.m. – 4:00 p.m.

Wednesday: 8:00 a.m. – 12:00 p.m.

Complementary coffee will be available in the exhibits area

INFORMATION ON EXHIBITING IN 2018

2018 IEEE – IEDM exhibits will feature products, equipment and services directly related to the areas covered by the Conference. Information is available by writing to:

Scien-Tech Associates, Inc., P.O. Box 2097, Banner Elk, NC 28604-2097

Tel: 1-828-898-7001

Email: dbarbsta@gmail.com

MRAM Posters and Forum

Technically sponsored by the IEEE Magnetics Society

Two IEEE Magnetics Society events at IEDM 2018

With the rising interest of the microelectronics industry in STT-MRAM, it is very important to strengthen the relationship between the microelectronics and magnetism communities since this technology requires expertizes from both areas. For that, two special events related to MRAM technology are being organized around IEDM by the IEEE Magnetics Society.

1) A special poster session dedicated to MRAM

(Wednesday 5 December, 2pm-5pm Plaza room)

Various topics will be covered including MRAM materials, phenomena, technology, testing, hybrid CMOS/MTJ technology and circuits, spin-logic. Similar MRAM poster sessions took place at IEDM 2016 and IEDM2017 which were very successful with more than 30 posters presented and very active cross-disciplinary discussions. This session is technically organized by the IEEE Magnetics Society. It will appear as a special MRAM poster session in the IEDM program. This event will be a great opportunity to bring together experts in magnetism and in microelectronics. Participants in this poster session need to register at IEDM as regular attendees. More information including the list of presented posters are posted on the IEEE Magnetics Society website: http://www.ieeemagnetics.org/

2) The 10th MRAM Global Innovation Forum

(Hilton Union Square, Golden Gate 2-5, 6 Dec 2018)

This is a one-day forum organized the day following IEDM (i.e on 6 December 2018, 8:45am – 5:30pm) in the same hotel as IEDM (Hilton Union Square, 333 O'Farrell St, San Francisco). The Forum will consist of 10 invited talks from leading experts and a panel discussion. Various MRAM related topics will be covered including STT-MRAM technology, memory and processor demonstrations, spin orbit torque MRAM, and the needs, challenges and potential of MRAM. The Forum was originally initiated by Samsung Semiconductor, and this forum marks the 10th edition of the series.

The Forum is entirely sponsored by Samsung Semiconductor. The registration to the Forum will be free of charge.

More information including the Forum program is posted on the IEEE Magnetics Society website: http://www.ieeemagnetics.org/

EDS Function

IEEE EDS Breakfast Meetup for Women in Engineering and Young Professionals

The time to make those important personal connections is now!

Attend the IEEE EDS Breakfast Meetup for Women in Engineering and Young Professionals

Monday, 3 December 2018 7:30 AM to 8:30 AM

Hilton San Francisco 4th Floor, Union Square 13

Meet and network with your peers and leaders in the electron devices community, like former IEDM General Chairs: Patrick Fay (IEDM'16) and Leda Lunardi (IEDM'03).

Stop by for a complimentary continental breakfast, and pick up important tips to help you make the most of the conference. This is a valuable experience you should not miss.

Registration for this event is now closed, but we welcome you to attend virtually, via social media. Details to be provided soon.

Sponsored by the IEEE EDS Young Professionals and Women in Electron Devices Committees.

Appendix - Abstracts, Bios & Technical Program

AWARD PRESENTATIONS

PLENARY SESSION AWARDS

Monday, December 3

2017 Roger A. Haken Best Student Paper Award

To: Felix Eltes, IBM Research - Zurich

For the paper entitled: "A Novel 25 Gbps Electro-optic Pockels Modulator Integrated on an Advanced Si Photonic Platform"

2017 EDS Paul Rappaport Award

To: Liesbethy Johanna Witters, Hiroaki Arimura, F. Sebaai, A. Hikavyy, A. P. Milenin, Roger Loo, A. De Keersgieter, G. Eneman, Tom Schram, Kurt Wostyn, Katia Devriendt, A. Schulze, Ruben Lieten, Steven Bilodeau, Emanuel Cooper, Peter Storck, Eddie Chiu, Crista Vrancken, Paola Favia, Eric Vancoille, Jerome Mitard, Robert Langer, Ann Opdebeeck, F. Holsteyns, Niamh Waldron, Kathy Barla, Vincent De Heyn, Dan Mocuta, Nadine Collaert

For the paper entitled: "Strained Germanium Gate-All-Around pMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition"

2017 EDS George Smith Award

To: Ali Saeidi, Farzan Jazaeri, Francesco Bellando, Igor Stolichnov, Gia V. Luong, Qing-Tai Zhao, Siegfried Mantl, Christian C. Enz, Adrian M. Ionescu

For the paper entitled: "Negative Capacitance as Performance Booster for Tunnel FETs and MOSFETs: An Experimental Study"

2018 EDS Distinguished Service Award

To: Shuji Ikeda, Tei Solutions Co. Ltd., Tsukuba, Japan

"To recognize and honor outstanding service to the Electron Devices Society"

2018 EDS Education Award

To: Ashraf Alam, Purdue University, West Lafayette, IN, USA

"For educating, inspiring and mentoring students and electron device professionals around the world"

2018 EDS J.J. Ebers Award

To: Michael Shur, Rennselaer Polytechnic Institute, Troy, NY, USA

"For pioneering the concept of ballistic transport in nanoscale semiconductor devices"

2018 IEEE/EDS Fellows

**This is a complete listing of the 2018 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2017 IEDM.*

Pamela Ann Abshire, Silver Spring, MD, USA
Timothy Boykin, University of Alabama Huntsville, AL, USA
Jeffrey Calame, Annapolis, MD, USA
Kun-yung Chang, Los Altos Hills, CA, USA
Kuan-neng Chen, National Chiao Tung Univeristy Hsinchu, Taiwan
Akira Fujiwara, NTT Basic Research Laboratories Atsugi, Japan
Michel Houssa, University of Leuven Leuven, Belgium
Jaroslav Hynecek, Allen, TX, USA
Thomas Kazior, Raytheon: Radio Frequency Components Andover, MA, USA
Michael Krames, Philips Lumileds Lighting Company San Jose, CA, USA
Isaac Lagnado, San Diego, CA, USA
Xiaobing Luo, Huazhong University of Science & Technology Wuhan, China
Chee Wee Liu, National Taiwan University Taipei, Taiwan
Ming Liu, Institute of Microelectronics of Chinese Academy of Sciences Beijing, China
Wei Lu, University of Michigan Ann Arbor, MI, USA
Zhenqiang Ma, University of Wisconsin-Madison Madison, WI, USA
Saibal Mukhopadhyay, Georgia Institue of Technology Atlanta, GA, USA
Hideo Ohno, Tohoku University Sendai, Japan
Hidetoshi Onodera, Kyoto University Kyoto, Japan
Philippe Paillet, University of Montpellier-CEA Paris, France
Joseph Pawlowski, Micron Technology, Inc. Boise, ID, USA
Seiji Samukawa, Tohoku University Sendai, Japan
Riichiro Shirota, National Chao-Tung University Hsinchu, Taiwan
Gregory Snider, University of Notre Dame Notre Dame, IN, USA
Shuji Tanaka, Tohoku University Sendai, Japan
Victor Veliadis, PowerAmerica Raleigh, NC, USA
Robert Weikle, University of Virginia-Charlottesville Charlottesville, VA, USA
Shien-yang Wu, Taiwan Semiconductor Manufacturing Company, Limited Hsinchu, Taiwan
Huikai Xie, University of Florida Gainesville, FL, USA
Jianbin Xu, Chinese University of Hong Kong Shatin NT, Hong Kong
Anthony Yen, ASML, San Jose, CA, USA

IEDM CAREER LUNCHEON

Tuesday, December 4

2018 IEEE Cledo Brunetti Award

To: Siegfried Selberherr

“For pioneering contributions to Technology Computer Aided Design.”

2018 IEEE Andrew S. Grove Award

To: Gurtej Singh Sandhu

"For contributions to silicon CMOS process technology that enable DRAM and NAND memory chip scaling."

2018 IEEE Leon K. Kirchmayer Graduate Teaching Award

To: Mark S. Lundstrom

"For creating a global online community for graduate education in nanotechnology as well as teaching, inspiring, and mentoring graduate students."

SRC Student Showcase Poster Session

Tuesday, December 4th, 2:00 – 4:00 pm
Golden Gate Ballroom

New to IEDM this year, Semiconductor Research Corporation (SRC) is hosting a student research showcase. SRC is sponsored by industry members and government agencies with the mission to drive advances in materials, devices, processing, metrology, and modeling, among other areas. Because these topics are relevant to the IEDM community, SRC is organizing a poster session led by students highlighting fundamental semiconductor research in universities worldwide. This session will be a great opportunity to engage with student researchers and their budding ideas.

IEDM Panel

Tuesday, December 4
Continental 1-5
Moderator: Sanjay Natarajan, Applied Materials

Title: **The Next 25 Years in Electronics**

IEEE Magnetics Society MRAM Poster Session

Wednesday, December 5th, 2:00 – 5:00 pm
Plaza Room

For the 3rd consecutive year, the IEEE Magnetics Society is organizing a special MRAM poster session to foster closer interactions between the microelectronics and magnetism communities. The posters will cover topics including MRAM materials, phenomena, technology, testing, hybrid CMOS/MTJ technology and circuits, and spin-logic.

Tutorials

Saturday, December 1
2:45 PM – 6:00 PM

Topics Presented at 2:45 PM – 4:15 PM
Continental 1-3 // Continental 4// Continental 5

Tutorial 1: Emerging Device Technologies for Neuromorphic Computing
Damien Querlioz, CNRS

In recent years, Artificial Intelligence (AI) has progressed to an astonishing level through the development of algorithms known as deep neural networks. Nevertheless, AI has to face a challenge: its considerable energy consumption, order of magnitudes higher than the brain on similar tasks. Neuromorphic computing aims at designing electronic systems whose operating principles are to some extent inspired by the brain, to reduce the energy consumption of AI. In this tutorial, we will first try to understand why the brain is more energy efficient than current AI. This will teach us fundamental lessons on the design of neuromorphic systems, which should avoid the von Neumann bottleneck by closely associating computational units (artificial neurons) and memory units (artificial synapses). We will see that one of the biggest challenges, however, is the inadequacy of current memory technologies. We will then study how resistive memories, phase change and spin torque memories, which naturally resemble synapses, can by contrast provide a solution. We will see that neuromorphic systems are sometimes less demanding in terms of device properties than conventional systems, which can allow using devices in a more optimal fashion. We will study the two main applications of neuromorphic hardware (inference and learning hardware) and show that they have very difference device requirements. We will also compare two visions for neuromorphic computing: the AI approach, which can bring immediate applications, and the longer term neuroscience-inspired approach. We will see that both approaches do not call for the same device work. Finally, we will study very recent developments that use the physics of conductive bridge and spin torque devices, directly for computing. We will see the benefits and the challenges of this approach to computing, which mimics very closely the way that brains use their own basic devices.

Tutorial 2: Reliability Challenges in Advanced Technologies
Ryan Lu, TSMC

Reliability Challenges in Advanced Technology – Ryan Lu, Deputy Director, TSMC – With logic technology moving toward 7nm, 5nm and beyond, reliability will become more and more critical. How to reserve just-enough reliability margin to comply with technology complexity and device performance requires thorough understanding of each reliability mechanism from physics, testing, reliability modeling to aging simulation. This tutorial will introduce reliability concepts and key reliability mechanisms at the beginning so attendees can have a good overview and background about reliability. Moving toward leading edge technologies, unique reliability challenges will be covered in detail to allow attendees to follow and to participate in reliability discussion. Aging simulation which can provide overall reliability risk assessments on circuit performance will be introduced so that attendees who are doing circuit design or working with designers on reliability evaluation can have an overall picture about aging simulation. Last, Memory reliability, specifically MRAM and RRAM reliability will be briefly discussed to give attendees background of such emerging memory technologies.

Tutorial 3: Quantum Computing Primer
Mark B. Ritter, IBM T.J. Watson Research Center

What sets apart quantum information and computation from conventional approaches? In this tutorial I will attempt to answer this question in layers. I will focus not only on basic physical principles which, if harnessed, promise a leap in computational power for certain problems, but also key advances in quantum technology implementations and algorithms. We will describe demonstrated qubit technologies and the methods to control and measure the quantum state of each, ranging from shaped microwave pulses to both optical and microwave pulses. We will describe single and two-qubit gates—all that is necessary to create universal quantum logic circuits—and basic algorithms which exploit superposition and entanglement of quantum information. We will then take a system-level view, describing the challenges of controlling and measuring systems of qubits. Finally, we will look at the basic types of universal quantum computers: near-term Noisy Intermediate Quantum systems (NISQ), and fully error-corrected Fault Tolerant Quantum

Computers (FTQC), the types of algorithms that can be run on these machines and the estimated system resource to run different algorithms.

Topics Presented at 4:30 PM – 6:00 PM
Continental 1-3 // Continental 4// Continental 5

Tutorial 4: Design-technology Co-optimization at RF and mmWave for 5G
Bertand Parvais, imec

The advent of 5G will not only bring great new opportunities but also new challenges for the technologies enabling this next-generation of mobile communications. Not only innovations in the overall network infrastructure will be needed, but also in the technologies for the mobile devices themselves. The tutorial introduces how to connect the specifications of RF circuits to device and technology elements. The objective is twofold: on one hand, to help circuit designers to better understand technologies; on the other hand, to guide technology developments based on the key challenges of the next radio generations. Specific methodologies for analog, RF, and mmWave will be presented, and compared to a device-technology co-optimization (DTCO) flow for logic applications. In this context, modelling the parasitics of transistors is crucial. Therefore, modelling techniques based on both experimental characterization and TCAD will be covered. Key features of advanced Silicon and III-V transistors for high-speed applications will be reviewed.

Tutorial 5: STT-MRAM Design and Device Requirement
Shinichiro Shiratake, Toshiba Memory

MRAM is one of the most promising emerging memories with characteristics of fast access speed, non-volatility and good endurance, though there has been strong desire for lower power consumption and smaller cell size. In comparison with old magnetic field writing, the spin transfer torque (STT) MRAM reduced its power consumption dramatically. Moreover, the p-(perpendicular) STT technology was proved to have much smaller cell size and less power consumption than horizontal type. After periods of many studies in embedded technologies and CPU cache applications, the gigabit class MRAM was finally reported at ISSCC2017. This tutorial will be provided by a memory design engineer and it will cover basic operation principle and the chip design of STT-MRAM. After comparing MRAM to conventional memories such as DRAM and Flash, as well as other kind of emerging memories, it will summarize the recent discovery of physics and related technology development which realized STT-MRAM operation. Then the overview of actual MRAM chip design is followed by the discussion of device requirements of which difference will be studied among applications such as embedded, logic-in memory, on-chip cache and stand-alone large scale MRAMs.

Tutorial 6: Power Transistors in Integrated BCD Technologies
Hal Edwards, Texas Instruments

Power transistors such as laterally-diffused metal-oxide-semiconductor (LDMOS) transistors are integrated with bipolar and complementary metal-oxide-semiconductor (CMOS) transistors in a bipolar-CMOS-DMOS (BCD) technology. This tutorial will cover the construction of an LDMOS power transistor integrated into a BCD technology. It will also cover key figures of merit (FOM) in the context of the most common power conversion circuit the half-bridge buck converter. Power transistor robustness issues such as hot-carrier reliability, electrical safe operating area (SOA), and thermal SOA will be introduced. Future directions for BCD technology research will be sketched as well.

2018 IEDM SHORT COURSE

Scaling Survival Guide in the More-than-Moore Era
Sunday, December 2, 2018
9:00 a.m. – 5:30 p.m.
Continental Ballroom 1-5
Course Organizer: Jin Cai, TSMC

CMOS scaling is facing ever increasing challenges as 7nm technology enters volume production this year. Extending the historical trend of power-performance-area-cost benefit requires concerted efforts from all aspects of CMOS technology development. This short course brings together six world-class experts from key areas of CMOS technology to share their view on how to survive the CMOS scaling challenges.

Anthony Yen will give the first lecture on extreme UV lithography and discuss its readiness for high volume manufacturing. It's critical to achieve the high pattern fidelity required for post-7nm nodes while reducing the number of lithography levels and process cost. Continued gate pitch scaling and power efficiency requirement will drive the evolution of new transistor architectures and channel materials beyond silicon FinFET. Witek Maszara's next lecture on MOSFET scaling will start from performance knobs for FinFET. He will proceed to discuss negative capacitance FET, gate-all-around devices, alternative channel materials and beyond CMOS devices. With continued CMOS scaling, variability is expected to increase and eventually constrain scaling. Siva Mudanai will give us the next lecture on how to overcome variation challenges. He will start with a primer on sources of variations and then review mitigation techniques used in recent generations. He will then discuss variation limiters in current generations and ongoing research to overcome them. He will conclude with an outlook for variation challenges in novel technologies. At system level, embedded on-chip memory plays an increasingly important role to improve the speed and energy efficiency in the era of big data and AI. Eric Wang's lecture on embedded memory technology will start with a review of scaling challenges of SRAM in advanced nodes and eFlash in mature nodes. He will then discuss new memory architectures for AI applications and emerging memory solutions such as STT-MRAM and RRAM. Scaling into the third dimension provides a new path for density scaling and increased functionality. Julien Ryckaet will give a lecture on latest 3D integration technology which can be implemented at various granularities from transistor level to system level. The lecture will cover 3D device architecture, standard cell and SRAM design in 3D, as well as 3D systems. Finally, Suburamanian Iyer will conclude the short course with a lecture on advanced packaging. High bandwidth interconnect is indispensable for high performance multi-chip solutions. After reviewing the history and current status of packaging technology, he will discuss two new technologies including silicon interconnect fabric and fan-out wafer level packaging which can offer chip-to-chip interconnects with a density that can rival that of on-chip interconnects.

Introduction and Overview
Organizer: Jin Cai, TSMC

Extreme UV Lithography: The Road to HVM and Beyond
Instructor: Anthony Yen, VP and Head of Technology Development Centers, ASML
- History of EUV lithography
- Optical physics of EUV lithography
- High volume manufacturing
- Continual improvement and high NA development

MOSFET Scaling Knobs and Future Alternatives
Instructor: Witek Maszara

- Scaling pressures
- FinFET performance knobs
- Gate-all-around devices (horizontal and vertical GAA)
- Negative capacitance FET
- Alternative channel materials (Ge, III-V, 2D-TMD, 1D-CNT)
- 3D monolithic stacking
- Tunnel FET and spin-based devices
- Device roadmap

Overcoming Variation Challenges
Instructor: Siva Mudanai, Principle Engineer, Intel

- Sources of variation
- Classification of variation based on their impact on circuits
- Variation limiters and innovations in recent generations
- Modeling systematic variation
- Interconnect variation
- Outlook for variation challenges in novel technologies

Embedded Memory: Present Status, Emerging Architecture and Technology for Future Applications
Instructor: Eric Wang, Director, TSMC

- Present Status and challenges (SRAM, eDRAM, eFlash, OTP)
- Emerging memory technologies (STT-MRAM and RRAM)

3D Integration for Density and Functionality
Instructor: Julien Ryckaert, Distinguished Member of the Technical Staff, IMEC

- Scaling to the third dimension: from devices to systems
- 3D device architectures: Vertical FET and CFET
- Circuit design in 3D: standard cells, SRAMs and sequential 3D
- 3D systems and system-technology co-optimization
- New 3D logic paradigms

Advanced Packaging: The Next Frontier for Moore's "Law"
Instructor: Subramanian Iyer, Distinguished Professor, UCLA

- Imbalance between packaging and silicon technology scaling
- Evolution of packaging in the last six decades
- Silicon interconnect fabric
- Case studies - Fan-out wafer level packaging, silicon as a packaging material, flexible hybrid electronics

2018 IEDM SHORT COURSE

It's all about memory, not logic!!!
Sunday, December 2, 2018
9:00 a.m. – 5:30 p.m.
Continental Ballroom 6-9
Course Organizer: Nirmal Ramaswamy, Micron

Memory technology is a defining component of modern computing and has a strong impact on performance, power and cost of computing systems. For example, the dollars spent on memory content in a smartphone is comparable to that of the CPU and approximately 300 billion gigabytes of memory will be produced in 2018. Rapid performance improvements on the CPU such as multicore CPUs and GPUs have strained memory performance and highlighted several performance issues with today's memory systems. In this memory centric short course, we are going to highlight several key topics in the memory landscape, elaborate on key challenges and identify opportunities for development.

DRAM scaling challenges, access device and capacitor requirements, retention and sensing challenges will be addressed by Don Soo Woo from Samsung. An overview of 3D NAND FLASH memory and its scaling challenges will be addressed by Makoto Fujiwara from Toshiba. Having discussed today's memories, the next speaker, Kiran Pangal from Intel will follow through with a detailed discussion of 3D X point technology. He will address various challenges and opportunities in the emerging memory systems. Next, Nick Kim from Hynix will deliver a lecture on how to circumvent the memory wall through HBM and the various challenges associated with packaging technologies for HBM. Reliability of a key aspect of the memory technology and Todd Marquart from Micron Technology will discuss this topic. Lastly, we will finish the short course with a look at the future of Processing in Memory delivered by Mircea Stan from University of Virginia. He will discuss the various advantages and possibilities as well as his view on overcoming the memory wall through PIM.

Introduction and Overview
Organizer: Nirmal Ramaswamy, Micron

DRAM: its challenging history and future
Instructor: Dong Soo Woo, Samsung

- DRAM Chip Architecture
- DRAM Cell structure
- Transistors in DRAM
- Evolution of DRAM Device Technology
- Scaling Challenges for DRAM into 1xnm

3D Flash Memories: Overview of Cell Structures, Operations and Scaling Challenges
Instructor: Makoto Fujiwara, Toshiba Memory

- Cell structures and key process steps of 3D flash memories
- Program and erase operations of charge trap cells
- Program disturb
- Scaling challenges in 3D charge trap cell design

Emerging Memories including Cross-Point, Opportunities and Challenges
Instructor: Kiran Pangal, Intel

- Memory/storage hierarchy
- Overview of cross-point memories
- Intel® 3D XPoint™ Technology and Products

Future of the Packaging Technologies for HBM
Instructor: Nick (Namseog) Kim, SK Hynix

- Introduction on High Bandwidth Memory
- HBM Packaging Technologies
- Key Processes and Challenges

- HBM Quality and Reliability
- Ecosystem and System in Package
- Future Challenges in HBM

Memory Reliability, Qualification and their Relation to System Level Reliability Strategies
Instructor: Todd Marquart, Micron

- Connecting reliability and qualification to reality
- Introduction to reliability statistics
- Memory stressing strategy
- Defectivity mitigation

Processing in memory (PIM): performance and thermal challenges and opportunities
Instructor: Mircea Stan, University of Virginia

- Motivation: the memory wall, memory latency, bandwidth
- PIM taxonomy
- History of PIM
- Recent PIM examples
- Thermal/Power delivery challenges for PIM
- Solutions that alleviate the Thermal/Power challenges

IEDM Panel
Tuesday, December 4, 8:00 PM
Continental 1-5

Moderator: Sanjay Natarajan, Applied Materials

The Next 25 Years in Electronics

Description: 25 years ago, few of us could have thought that advances in chip technology will allow us to have a tiny device in our pocket that connects us to everyone, provides us with instant access to the world's information, translate foreign languages instantly for us, and tracks our health. Our panelists will debate, discuss, and predict how semiconductor technology will evolve and what new life-changing technologies it will enable in 25 years from today (circa 2045). Given the ambitious scope of this topic, we have assembled an esteemed group of panelists who have had a front-row seat for most of the past 25 years and are in a position to look out over the next 25 years. The group includes industry CEO's and CTO's, long-tenured professors, and government participants from the early days of DARPA for this 25-year look back and 25-year look forward.

Panelists:

Jim Handy, Objective Analysis
Jay Lewis, DARPA
Mark Lundstrom, Purdue
Gurtej Sandhu, Micron
H.S. Philip Wong, TSMC
Jeff Welser, IBM

Session 1: Plenary
Monday, December 3, 9:00 AM
Grand Ballroom B

Welcome and Awards
General Chair: Ken Rim, Qualcomm

Plenary Papers
Technical Program Chair: Mariko Takayanagi, Toshiba

1.1 4th Industrial Revolution and Foundry: Challenges and Opportunities (Invited), *E. S. Jung, Foundry Business, Samsung Electronics,*

Semiconductor has been the key enabler in the advancement of electronics for the past 50 years. With the coming of 4th industrial revolution, semiconductor will continue to play an even greater role as we invite a wide variety of new applications into our lives, including smart cars, smart factories, artificial intelligence, data centers, robots, etc. Such importance of semiconductor is attributed to its unique ability to copy and create everything human beings imagine. In this paper, the roles of foundry in the 4th industrial revolution, as the entity to turn ideas into reality along with electronic design automation (EDA), intellectual property (IP) vendor, and outsourced semiconductor assembly and test (OSAT) companies, as well as the need for global open innovation to overcome imminent challenges will be discussed.

1.2 Venturing Electronics into Unknown Grounds (Invited), *G. Fettweis, K. Leo, B. Voit, U. Schneider, L. Scheuvens, Center for Advancing Electronics Dresden (cfaed), Technische Universität Dresden*

Electronics is a huge driver for economic success of today's societies. cfaed, the German Cluster of Excellence located in Dresden (Germany), aims at pushing the boundaries of electronics into unknown grounds. This includes not only current electronics but also scientist's and engineer's projection of how the electronics landscape will look like in the future. We pursue an approach that connects all layers from new materials to new system design (vertical) as well as across our Research Routes (horizontal) and ensure coherence through adequate measures. cfaed is centered at one location which, combined with our unique approach, places it above the highly funded Competitive Landscape.

1.3 Future Computing Hardware for AI (Invited), *J. Welser, J. W. Pitera, C. Goldberg, IBM Research*

Hardware has taken on a supporting role in the maturation and proliferation of narrow AI, but will take a leading role to enable the innovation and adoption of broad AI. The concurrent evolution of broad AI with purpose-built hardware will shift traditional balances between cloud and edge, structured and unstructured data, and training and inference. Heterogeneous system architectures are already being delivered where varied compute resources, including high-bandwidth CPUs, specialized AI accelerators, and high-performance networking are infused in each node to yield significant performance improvements. Looking to the future, we envision a roadmap of specialized technologies to accelerate AI, starting with heterogeneous digital von Neumann machines, exploring reduced-precision accelerator approaches, finding the limits of conventional device power-performance with analog AI devices, and finishing with quantum computing for AI.

Session 2: Memory Technology - Charge Based Memories
Monday, December 3, 1:30 PM

Grand Ballroom A
Co- Chairs: M. Kobayashi, The University of Tokyo
J. Lee, Samsung Electronics

1:35 PM – 2:00 PM
2.1 Scaling Trends in NAND Flash (Invited), *K. Parat and A. Goda*, Intel Corporation, *Micron Technology*

As the 2D NAND Flash scaling plateaued, 3D NAND Flash emerged as a strong successor to continue the scaling trend. Improved cell characteristics of 3D NAND have enabled 4bits/cell capability, allowing for additional scaling. This paper describes recent innovations in 3D NAND technology and key challenges ahead for continued scaling.

2:00 PM - 2:25 PM
2.2 Analysis and Realization of TLC or even QLC Operation with a High Performance Multi-times Verify Scheme in 3D NAND Flash memory, *C.C. Lu, C.C. Cheng, H.P. Chiu, W.L. Lin,T.W. Chen, S.H. Ku, Wen-Jer Tsai, T.C. Lu*, K.C. Chen, Tahui Wang*, C.-Y. Lu*, *Macronix International Co., Ltd., *National Chiao-Tung University*

Feasibility of multi-times verify (MTV) scheme on triple-level cell (TLC) and quad-level cell (QLC) operations of charge-trap storage 3D NAND memories is investigated comprehensively. Results reveal that random telegraph noise (RTN) and program noise are the major factors affecting lower (LB) and upper boundaries (HB) of Vt distribution, respectively. Enlargement of operation window and reduction of ECC usage with MTV scheme to mitigate RTN-induced LB tail are demonstrated on TLC and QLC operations. In addition, the impact of program noise on HB Vt under various process conditions and ISPP steps is studied experimentally and also explained by our Monte Carlo simulator. Finally, program performance and reserved margin with and without MTV scheme applied on TLC and QLC operation are demonstrated.

2:25 PM - 2:50 PM
2.3 Implementing Spike-Timing-Dependent Plasticity and Unsupervised Learning in a Mainstream NOR Flash Memory Array, *G. Malavena, A. S. Spinelli, and C. Monzio Compagnoni, Politecnico di Milano*

In this work, we present the first implementation of spike-timing-dependent plasticity (STDP) and unsupervised learning in a mainstream NOR Flash memory array based on floating-gate cells. A simple yet effective word-line and bit-line pulse scheme is proposed to make a common-ground double-polysilicon NOR array in 40 nm embedded technology work as an artificial synaptic array in a spiking neural network learning according to the STDP rule, with no change required either to the array or to the cell design. With this scheme, long-term potentiation and long-term depression of the synaptic weights are achieved, respectively, by hot-hole injection and channel hot-electron injection at the drain side of the cells. Unsupervised learning is experimentally demonstrated in the array, paving the way for the development of large-scale and high-density neuromorphic systems based on mainstream nonvolatile memory technologies.

2:50 PM Coffee Break

3:15 PM - 3:40 PM
2.4 A Novel Voltage-Accumulation Vector-Matrix Multiplication Architecture Using Resistor-shunted Floating Gate Flash Memory Device for Low-power and High-density Neural Network Applications, *Y.-Y. Lin, F.-M. Lee, M.-H. Lee, W.-C. Chen, H.-L. Lung, K.-C. Wang, and C.-Y. Lu, Macronix International Co., Ltd.*

We propose a novel processing-in-memory (PIM) architecture based on the voltage summation concept to accelerate the vector-matrix multiplication for neural network (NN) applications. The core device is formed by adding a buried shunt resistor to a floating gate Flash memory device. The NN string is constructed the same way as in NAND Flash by connecting the core devices in series. In perceptron operation the weighting factors are stored in the floating gate device and the sum-of-product is readily obtained by summing the voltage drop of the cells in each NN string. The energy consumption for 128 multiply-and-sum operations within a string can be as low as 0.2pJ. Finally, with the weight values stored in the non-volatile memory there is no need to move data around and this greatly improves the performance and energy efficiency for neural network applications.

3:40 PM - 4:05 PM

2.5 Vertical Ferroelectric HfO2 FET based on 3-D NAND Architecture: Towards Dense Low-Power Memory, *K. Florent, M. Pesic*, A. Subirats, K. Banerjee, S. Lavizzari, A. Arreghini, L. Di Piazza, G. Potoms, F. Sebaai, S. R. C. McMitchell, M. Popovici, G. Groeseneken, and J. Van Houdt, imec, also with ESAT- KU Leuven, *MDLSoft Inc.*

A vertical ferroelectric HfO2 field effect transistor based on 3-D macaroni NAND architecture is reported for the first time. Up to 2 V memory window was obtained after the application of 100 ns program/erase pulses. Flash-like endurance of 1E4 cycles is reported and first reliability assessments were performed.

4:05 PM - 4:30 PM

2.6 Hybrid 1T e-DRAM and e-NVM Realized in One 10 nm node Ferro FinFET device with Charge Trapping and Domain Switching Effects, Q. Luo, T. Gong, Y. Cheng**, *Q. Zhang, H. Yu, J. Yu, H. Ma, X. Xu, K. Huang, X. Zhu, D. Dong, J. Yin, P. Yuan, L. Tai, J. Gao, J. F. Li, H. Yin, S. Long, Q. Liu, H. Lv, M. Liu, Chinese Academy of Sciences, *University of the Chinese Academy of Sciences, **East China Normal University*

For the first time, we experimentally demonstrated a 10 nm node HfZrO based FE-FinFET device with both Charge Trapping and Domain Switching memory effect. Extreme high endurance ($>10^{12}$), high operation speed (< 20ns), good data retention (104@85°C), low operation voltage (<3 V) were identified in charge trapping mode, which is quite promising for e-DRAM application. As the device working in domain switching mode, even more robust retention (>10 years) and read disturbance immunity were achieved, showing great potential for e-NVM application.

4:30 PM - 4:55 PM

2.7 High-performance (EOT<0.4nm, Jg~10-7A/cm2) ALD-deposited RuSrTiO3 stack for next generations DRAM pillar capacitor (Late News), *M. Popovici, A. Belmonte, H. Oh, G. Potoms, J.Meersschaut, O. Richard, H. Hodi, S. Van Elshocht, R. Delhougne, L. Goux, and G. Sankar Kar, imec*

We demonstrate the fabrication of strontium titanate (STO) based metal-insulator-metal (MIM) capaci tors with very-high dielectric constant (k~118) and low leakage of 10-7 A/cm2 at +/-1V for a ~11nm thick dielectric using Ru as bottom electrode (BE) and top electrode (TE). The k enhancement is attributed to the formation of an ultrathin cubic SrRuO3 phase at the RuSTO bottom interface, acting as a template optimizing the STO crystal quality from the interface to the bulk. This interface quality is evidenced by the same k~118 extracted from STO thickness series and relating to the bulk-k value. This achievement opens up an alternative integration roadmap for DRAM capacitors, moving from the current cup-shape to a denser pillar-shape design.

Session 3: Circuit and Device Interaction - Device and Algorithm Co-design for Neuromorphic and In-memory Computing

Monday, December 3, 1:30 PM

Grand Ballroom B

Co- Chairs: R. Tetzlaff, TU Dresden
T-H Hou, National Chiao Tung University

1:35 PM - 2:00 PM

3.1 Exploiting Hybrid Precision for Training and Inference: A 2T-1FeFET Based Analog Synaptic Weight Cell, *X. Sun, P. Wang, K. Ni*, S. Datta*, and S. Yu**, Arizona State University, *University of Notre Dame, **Georgia Institute of Technology*

In-memory computing with analog non-volatile memories (NVMs) can accelerate both the in-situ training and inference of deep neural networks (DNNs) by parallelizing multiply-accumulate (MAC) operations in the analog domain. However, the in-situ training accuracy suffers from unacceptable degradation due to undesired weight-update asymmetry/nonlinearity and limited bit precision. In this work, we overcome this challenge by introducing a compact Ferroelectric FET (FeFET) based synaptic cell that exploits hybrid precision for in-situ training and inference. We propose a novel hybrid approach where we use modulated "volatile" gate voltage of FeFET to represent the least significant bits (LSBs) for symmetric/linear update during training only, and use "non-volatile" polarization states of FeFET to hold the information of most significant bits (MSBs) for inference. This design is demonstrated by the experimentally validated FeFET SPICE model and co-simulation with the TensorFlow framework. The results show that with the proposed 6-bit and 7-bit synapse design, the in-situ training accuracy can achieve ~97.3% on MNIST dataset and ~87% on CIFAR-10 dataset, respectively, approaching the ideal software based training.

2:00 PM - 2:25 PM

3.2 Analog Computing for Deep Learning: Algorithms, Materials & Architectures (Invited), *W. Haensch, IBM Research*

Analog, or neuromorphic, computing for Deep Learning (DL) utilizes the fact that matrix manipulations that are inherent in the back-propagation algorithm, can be performed at constant time, in parallel, on arrays with nonvolatile memory (NVM) elements in which the weights are encoded. We discuss the NVM material requirements that need to be met to achieve a classification accuracy on par with the conventional digital approaches, discuss advantages and drawbacks, and highlight opportunities that can take advantage using analog arrays.

2:25 PM - 2:50 PM

3.3 Hardware Acceleration of Simulated Annealing of Spin Glass by RRAM Crossbar Array, *J. H. Shin, Y. Jeong, M. A. Zidan, Q. Wang, and W. D. Lu, University of Michigan*

Simulated annealing was successfully accelerated by in-memory computing hardware/software package using RRAM crossbar arrays to solve spin glass problems. Ta_2O_5-based RRAM array and stochastic Cu-based CBRAMs were utilized for calculation of the Hamiltonian and decision of spin-flip events, respectively. A parallel spin-flip strategy was demonstrated to further accelerate simulated annealing.

2:50 PM Coffee Break

3:15 PM - 3:40 PM

3.4 Demontration of Generative Adversarial Network by Intrinsic Random Noises of Analog RRAM Devices, *Y. Lin, H. Wu, B. Gao, P. Yao, W. Wu, Q. Zhang, X. Zhang, X. Li, F. Li*, J. Lu*, G. Li**, S. Yu***, and H. Qian, Tsinghua University, *Hunan University, **Huawei Technologies Co., LTD., ***Georgia Institute of Technology*

For the first time, Generative Adversarial Network (GAN) is experimentally demonstrated on 1kb analog RRAM array. After online training, the network can generate different patterns of digital numbers. The intrinsic random noises of analog RRAM device are utilized as the input of the neural network to improve the diversity of the generated numbers. The impacts of read and write noises on the performance of GAN are analyzed. Optimized methodology is developed to mitigate the excessive noise effect on RRAM based GAN. This work proves that RRAM is suitable for the application of GAN. It also paves a new way to take advantage of the non-ideal effects of RRAM devices.

3:40 PM - 4:05 PM
3.5 Error-Resilient Analog Image Storage and Compression with Analog-Valued RRAM Arrays: An Adaptive Joint Source-Channel Coding Approach, *X. Zheng, R. Zarcone*, D. Paiton*, J. Sohn, W. Wan, B. Olshausen* and H. -S. Philip Wong, Stanford University, *University of California, Berkeley*

We demonstrate by experiment an image storage and compression task by directly storing analog image data onto an analog-valued RRAM array. A joint source-channel coding algorithm is developed with a neural network to encode and retrieve natural images. The encoder and decoder adapt jointly to the statistics of the images and the statistics of the RRAM array in order to minimize distortion. This adaptive joint source-channel coding method is resilient to RRAM array non-idealities such as cycle-to-cycle and device-to-device variations, time-dependent variability, and non-functional storage cells, while achieving a reasonable reconstruction performance of ~ 20 dB using only 0.1 devices/pixel for the analog image.

Session 4: Sensors, MEMS, and BioMEMS - Micro and Nano Electromechanical Systems
Monday, December 3, 1:30 PM
Continental Ballroom 1-3
Co- Chairs: F. Perez-Murano, IMB-CNM
J-B Yoon, KAIST

1:35 PM - 2:00 PM
4.1 Demonstration of 50-mV Digital Integrated Circuits with Microelectromechanical Relays, *Z. A. Ye, S. Almeida, M. Rusch, A. Perlas, W. Zhang, U. Sikder, J. Jeon, V. Stojanović, and T.-J. K. Liu University of California, Berkeley*

50-mV operation of digital integrated circuits at room temperature is demonstrated using body-biased microelectromechanical relays. An improved relay design and self-assembled molecular coating reduce contact adhesion and hysteretic switching behavior, allowing relays to operate reliably with sub-50-mV gate voltage, enabling ultra-low active power consumption and zero static power consumption.

2:00 PM - 2:25 PM
4.2 Highly sensitive spintronic strain-gauge sensor based on magnetic tunnel junction and its application to MEMS microphone (Invited), *Y. Fuji, Y. Higashi, S. Kaji, K. Masunishi, A. Yuzawa, T. Nagata, K. Okamoto, S. Baba, T. Ono, and M. Hara, Toshiba Corporation*

We describe spintronic strain-gauge sensors based on magnetic tunnel junctions that exhibit extremely high gauge factors exceeding 5000. This high gauge factor was realized by using a novel amorphous magnetostrictive sensing layer. We also introduce a Spin-MEMS microphone in which these highly sensitive strain-gauge sensors are integrated on a diaphragm.

2:25 PM - 2:50 PM
4.3 Intermixing of motional currents in suspended CNT-FET based resonators, *L. Kumar, L. Vera Jenni, M. Haluska, C. Roman and C. Hierold, ETH ZURICH*

Here, we report the intermixing of piezoresistive and conduction modulation current in a carbon nanotube field effect transistor (CNT-FET) based resonator. We show that due to static displacement of the nanotube as a result of electrostatic actuation, the motional current at the resonance frequency consist of both current components. For instance at a gate DC bias of 1.3 V, 3/4 of motional current is conduction modulation current while the rest arises from piezoresistive effects. The intermixing effect due to asymmetry influences the fundamental harmonic response as well as the physical nature of the electrical signal being sensed; both of which are important for understanding frequency harmonics in nanoresonators and developing efficient readout schemes for nanoscale sensors.

2:50 PM - 3:15 PM
4.4 Glowing Graphene Nanoelectromechanical Resonators at Ultrahigh Temperature up to 2650K, *F. Ye, J. Lee, and P. X.-L. Feng, Case Western Reserve University*

We report on the first experimental demonstration of electrothermally tuned few-layer graphene resonant nanoelectromechanical systems (NEMS) operating at high frequency (HF) simultaneously with strong visible light emission. In tri-layer graphene resonators with carefully controlled Joule heating, we have demonstrated ultra-wide frequency tuning up to $\Delta f/f0 \approx 1300\%$, which is the highest frequency tuning range known to date among reported 2D materials resonators. Simultaneously, device temperature variations imposed by Joule heating are monitored using Raman spectroscopy and emission spectrum; and we find that the device temperature increases from 300 K up to 2650 K, which is the highest operating temperature known to date for electromechanical resonators. When device temperature is above 1800K, the graphene vibrating NEMS starts glowing and emitting visible light with robust mechanical resonance. These results show that electromechanical resonance modes can be robustly sustained and read out at glowing temperatures with incandescent emissions in graphene NEMS, suggesting new perspectives for integrating and configuring timing functions in light emitting graphene devices for harsh and extreme environment applications.

3:15 PM Coffee Break

3:40 PM - 4:05 PM
4.5 Monolithic Integration of Micron-scale Piezoelectric Materials with CMOS for Biomedical Applications, *C. Shi, T. Costa, J. Elloian, and K. L. Shepard, Columbia University*

We present the monolithic integration of piezoelectric micromachined ultrasonic transducers (PMUT) in both polyvinylidene difluoride (PVDF) and lead zirconate titanate (PZT) with complementary metal–oxide–semiconductor (CMOS) technology. Characterization results of micro-fabricated devices reveal the preservation of the piezoelectric properties of PVDF/PZT and PMUT functionality with co-designed CMOS ICs.

4:05 PM - 4:30 PM
4.6 A Nano-Mechanical Resonator with 10nm Hafnium-Zirconium Oxide Ferroelectric Transducer, *M. Ghatge, G. Walters, T. Nishida and R. Tabrizian, University of Florida*

This paper reports, for the first time, on a 10nm hafnium-zirconium oxide (HZO) piezoelectric transducer for nano-electromechanical systems. The developed 10nm HZO transducer is used for excitation of a silicon-based multi-morph nano-mechanical resonator, with an overall thickness of ~350nm, at ~4MHz. Benefiting from large piezoelectric coefficient, fully conformal deposition, and CMOS-compatibility, ALD-deposited 10nm HZO transducer paves the way for realization of truly monolithic cm- and mm-wave RF front-ends for the emerging 5G wireless communication systems.

4:30 PM - 4:55 PM

4.7 Comprehensive optical losses investigation of VLSI Silicon optomechanical ring resonator sensors, *L. Schwab, P.E. Allain*, L. Banniard**, A. Fafin**, M. Gely**, O. Lemonnier**, P. ** M. Hermouet3** S. Hentz**, I. Favero*, B. Legrand and G. Jourdan **, Université de Toulouse, *Univ. Paris Diderot, **Univ. Grenoble Alpes, CEA LETI*

Cavity optomechanics devices are leading edge candidates for a new generation of sensors both in the quantum and classical realms. Several single devices have been demonstrated in numerous labs, however large-scale integration capability necessary for industrial deployment is still an issue. In this paper, we present very-large-scale integrated (VLSI) optomechanical sensors fabricated from standard 200 mm Silicon-On-Insulator (SOI) wafers. Optical properties over a statistically significant sample size have been systematically investigated and show an excellent modeling to experiment agreement, a coupling parameter dispersion of 7% and a manufacturing yield larger than 98%. Controlled versatile sensors, such as these, could easily be embedded in any chip where mass or force sensing is needed.

Session 5 (Focus): Characterization, Reliability, and Yield - Interconnects to Enable Continued Scaling
Monday, December 3, 1:30 PM
Continental Ballroom 4
Co- Chairs: T. Oates, TSMC
T. Nigam, GLOBALFOUNDRIES

1:35 PM - 2:00 PM
5.1 Interconnect Design and Technology Optimization for Conventional and Emerging Nanoscale Devices: A Physical Design Perspective (Invited), *D. Prasad, A. Naeemi*, Arm Inc., *Georgia Instiute of Technology*

Interconnect parasitics severely limit the performance and power dissipation in modern circuits at the advanced process technology nodes. Hence, device-level advances must be complemented with appropriate interconnect technology and design innovations for effective enablement at the circuit and system levels. This paper highlights the impact of device technologies on the optimal interconnect design. The studies for FinFET and Tunnel-FETs are conducted on fully placed-and-routed physical designs. The impact of device and interconnect technology co-optimization on circuit performance, power, and variability is shown for a range of emerging devices.

2:00 PM - 2:25 PM
5.2 Mechanisms of Electromigration Damage in Cu Interconnects (Invited), *C.-K. Hu, L. Gignac*, G. Lian**, C. Cabral*, K. Motoyama, H. Shobha, J. Demarest, Y. Ostrovski, C. M. Breslin*, M. Ali**, J. Benedict**, P. S. McLaughlin, J. Ni, X. H. Liu, IBM Research at Albany, *IBM T. J. Watson Research Center, **IBM Systems*

Mechanisms of electromigration (EM) damage in Cu interconnects through various CMOS nodes are reviewed. Pure Cu and Cu alloy interconnects that were used down to 14 nm node can no longer satisfy the electrical current used for 10 nm node and beyond in high-performance ICs. Cu interconnects with a metal cap should be used. Cu interface diffusivity with EM activation energy of 1.6 eV was found to be the dominate EM factor in Cu lines with a Co liner and cap. The median lifetime of 7 or 10 nm node Cu with TaN/Co liner and Co cap is predicted to be over ten thousand years at 140oC with 1.5x10^7A/cm^2. However, the resistivity size effect and the difficulty of scaling barrier/liner layer without defects can limit the Cu BEOL roadmap below the 7 nm node.

2:25 PM - 2:50 PM

5.3 Interconnect metals beyond copper: reliability challenges and opportunities (Invited), *K. Croes, Ch. Adelmann, C.J. Wilson, H. Zahedmanesh, O. Varela Pedreira, C. Wu, A. Lesniewsak, H. Oprins, S. Beyne, I. Ciofi, D. Kocaay, M. Stucchi and Zs. Tokei, imec*

Reliability challenges of candidate metal systems to replace traditional Cu wiring in future interconnects are discussed. From a reliability perspective, a key opportunity is electromigration improvement: due to their high melting point and slower self-diffusion kinetics, higher current carrying capabilities are possible. Also, the higher cohesive energy and better resistance to oxidation of some metals potentially allows for barrierless integration, although adhesion properties must be carefully optimized. Besides avoiding small grain pinning and enabling high aspect ratio trench fill, the main processing challenges are identified to be a) avoiding seam voids, b) adhesion, c) CMP and d) disruptive metal etch. Main reliability challenges are related to higher mechanical stresses and higher joule heating which could lead to delamination during further processing and packaging and to enhanced electromigration in nearby metal lines.

2:50 PM - 3:15 PM

5.4 Microstructure Evolution and Effect on Resistivity for Cu Nanointerconnects and Beyond (Invited), *S. Hu, P. S. Ho, Unversity of Texas at Austin*

In this paper, we investigate the microstructure evolution in Cu, Co and Ru nanointerconnects and the scaling effect on resistivity. The scaling effect on microstructure of Cu interconnects was analyzed to the 24 nm linewidth for the 14 nm node using a high-resolution TEM precession microdiffraction technique. The TEM study was supplemented by a Monte Carlo simulation to investigate grain growth in nanointerconnects based on local energy minimization. The scaling effect on electrical resistivity was analyzed for Cu, Ru and Co nanointerconnects, taking into account the contributions from surface and grain boundary scatterings. The results for Cu and Co are consistent with recent experiments.

3:15 PM Coffee Break

3:40 PM - 4:05 PM

5.5 Integrating Graphene into Future Generations of Interconnect Wires (Invited), *L Li, H.-S. Philip Wong, Stanford University*

The escalating RC delay and diminishing reliability of Cu interconnect present immense challenges for integrated circuits performance improvement. This paper reviews the use of single-layer graphene as the diffusion barrier and capping layer to extend scaling of Cu into future generations of interconnects. With graphene barrier/capping layer, processor core simulations predict an 8% speed boost or 12% energy saving, plus higher tolerance for process variations. Single-layer graphene (3.35 Å thick) provides 3.3× longer barrier lifetime than 2 nm TaN. Barrier reliability is expected to further improve with transfer-free and single-crystalline graphene. In-situ low-temperature grown graphene (<0.7 nm thick) improves Cu electromigration lifetime by 10× than Cu with 2 nm CoWP. For interconnect scaling beyond Cu, we discuss the potential benefits and challenges of employing multilayer graphene as a Cu replacement. Multi-layer graphene shows better resistivity scaling trend with $FeCl_3$ doping and higher immunity to electromigration. Replacing Cu with multi-layer graphene, processor cores achieve 9% higher speed or 16% less energy consumption. Spin-on-glass encapsulated multi-layer graphene shows two times longer electromigration lifetime than CoWP capped Cu.

4:05 PM - 4:30 PM

5.6 Interconnect Trend for Single Digit Nodes (Invited), *M. Naik, Applied Materials Inc.*

Transistor performance continues to improve with density scaling and move to FinFET architectures. However, feature size reduction increases parasitic contact and interconnect resistance. This degrades the power-performance equation. To address the resistance bottleneck; new materials, new fill technologies and new integration schemes are in play. This paper reviews metallization trends for contact and interconnect as the industry prepares for 7nm node production and looks towards developing 5 and 3nm nodes.

Session 6 (Focus): Nano Device Technology - Quantum Computing Devices
Monday, December 3, 1:30 PM
Continental Ballroom 5
Co- Chairs: I. Radu, imec
W. Taylor, GLOBALFOUNDRIES

1:35 PM - 2:00 PM
6.1 Device challenges for near term superconducting quantum processors: frequency collisions (Invited), *M. Brink, J. M. Chow, J. Hertzberg, E. Magesan, S. Rosenblatt, IBM T.J. Watson Research Center*

The outstanding progress in experimental quantum computing with superconducting Josephson-junction based qubits over the past few decades has pushed coherence times many orders of magnitude above that of the first measured. We are also in the midst of scaling towards complex architectures of multi-qubit processors where maintaining very low gate error rates at the limits supported by coherence times is extremely important. Here we will review some of the critical materials and device challenges for superconducting qubits from the perspective of improved coherence and improved error rates. In particular we will focus on the problem of frequency allocations in order to target multi-qubit lattices for fixed-frequency microwave-based gates.

2:00 PM - 2:25 PM
6.2 Scalable quantum computing with ion-implanted dopant atoms in silicon (Invited), *A. Morello, G. Tosi, F.A. Mohiyaddin, V. Schmitt, V. Mourik, T. Botzem, A. Laucht, J.J. Pla, S. Tenberg, R. Savytskyy, M. Madzik, F. Hudson, A.S. Dzurak, K.M. Itoh*, A.M. Jakob**, B.C. Johnson**, J.C. McCallum** and D.N. Jamieson**, UNSW Sydney, *Keio University, ** University of Melbourne,*

We present a scalable strategy to manufacture quantum computer devices, by encoding quantum information in the combined electron-nuclear spin state of individual ion-implanted phosphorus dopant atoms in silicon. Our strategy allows a typical pitch between quantum bits of order 200 nm, and retains compatibility with the standard fabrication processes adopted in classical CMOS nanoelectronic devices. We theoretically predict fast and high-fidelity quantum logic operations, and present preliminary experimental progress towards the realization of a “flip-flop” qubit system.

2:25 PM - 2:50 PM
6.3 Qubit Device Integration Using Advanced Semiconductor Manufacturing Process Technology (Invited), *R. Pillarisetty, N. Thomas, H.C. George, K. Singh, J. Roberts, L. Lampert, P. Amin, T.F. Watson, G. Zheng, J. Torres, M. Metz, R. Kotlyar, P. Keys, J.M. Boter*, J.P. Dehollain*, G. Droulers*, G. Eenink*, R. Li*, L. Massa*, D. Sabbagh*, N. Samkharadze*, C. Volk*, B. P. Wuetz*, A.-M. Zwerver*, M. Veldhorst*, G. Scappucci*, L.M.K. Vandersypen*, J.S. Clarke Intel Corporation, *TU Delft*

Quantum computing’s value proposition of an exponential speedup in computing power for certain applications has propelled a vast array of research across the globe. While several different physical implementations of device level qubits are being investigated, semiconductor spin qubits have many similarities to scaled transistors. In this article, we discuss the device/integration of full 300mm based spin

qubit devices. This includes the development of (i) a 28Si epitaxial module ecosystem for growing isotopically pure substrates with among the best Hall mobility at these oxide thicknesses, (ii) a custom 300mm qubit testchip and integration/device line, and (iii) a novel dual nested gate integration process for creating quantum dots

2:50 PM *Coffee Break*

3:15 PM - 3:40 PM
6.4 Silicon Isotope Technology for Quantum Computing (Invited), *S. Miyamoto, K. Itoh, Keio University*

We present isotopically engineered Si-28/SiGe heterostructures for development of silicon-based quantum computers using a standard silicon CMOS integration technology. Our Si-28 quantum-wells are well-strained and demonstrate high electron mobility and large valley-splitting. These properties provide promising platforms for realization of highly integrated spin qubits working together with silicon CMOS circuits.

3:40 PM - 4:05 PM
6.5 Towards scalable silicon quantum computing (Invited), *M. Vinet, L. Hutin, B. Bertrand, S. Barraud, J.-M. Hartmann, Y.-J. Kim, V. Mazzocchi, A. Amisse, H. Bohuslavskyi, L. Bourdet*, A. Crippa*, X. Jehl*, R. Maurand*, Y.-M. Niquet*, M. Sanquer*, B. Venitucci*, B. Jado**, E. Chanrion**,P.-A. Mortemousque**, C. Spence**, M. Urdampilleta**, S. De Franceschi* and T. Meunier**, Université Grenoble Alpes, *CEA, LETI, **CNRS*

We report the efforts and challenges dedicated towards building a scalable quantum computer based on Si spin qubits. We review the advantages of relying on devices fabricated in a thin film technology as their properties can be in situ tuned by the back gate voltage, which prefigures tuning capabilities in scalable qubits architectures.

4:05 PM - 4:30 PM
6.6 Majorana QuBits (Invited), *L. Kouwenhoven, Delft University of Technology*

Abstract- We present an overview of Majorana qubits based on one-dimensional semiconducting nanowires partially covered with a conventional superconductor. Majorana zero modes emerge at the wire ends when this hybrid system transitions from a conventional superconducting phase to a topological phase, in general occurring on increasing a magnetic field. For sufficiently long wires different Majoranas are fully independent and Majorana-based qubit states become topologically protected, which make them insensitive to local sources of noise. We present qubit designs, materials and device development and ongoing experimental efforts.

Session 7: Process and Manufacturing Technology - 3D Integration and Memory Technologies
Monday, December 3, 1:30 PM
Continental Ballroom 6
Co- Chairs: P. Baars, GLOBALFOUNDRIES
T. Ando, IBM

1:35 PM - 2:00 PM
7.1 First Demonstration of 3D stacked Finfets at a 45nm fin pitch and 110nm gate pitch technology on 300mm wafers., *A. Vandooren, J. Franco, Z. Wu*, B. Parvai**, W. Li, L. Witters, A. Walke, L. Peng, V. Deshpande, N. Rassoul, G. Hellings,G. Jamieson, F. Inoue, K. Devriendt, L. Teugels, N. Heylen, E. Vecchio, T. Zheng, E. Rosseel, W. Vanherle, A. Hikavyy, G. Mannaert, B. T. Chan, R. Ritzenthaler, J.*

*Mitard, L. Ragnarsson, N. Waldron, V. De Heyn, S. Demuynck, J. Boemmels, D. Mocuta, J. Ryckaert and N. Collaert, imec, *also with KULeuven, Leuven, Belgium, **also with VUB, Brussels, Belgium*

3D stacking using a sequential integration approach is demonstrated for finfet devices on 300mm wafers at a 45nm fin pitch and 110nm poly pitch technology. This demonstrates the compatibility of the 3D sequential approach for aggressive device density stacking at advanced nodes thanks to the tight alignment precision of the first processed top layer to the last processed bottom layer through the top silicon channel and bonding stack during 193nm immersion lithography. The top devices are junction-less devices fabricated at low temperature (T≤525°C) in a top Si layer transferred by wafer-to-wafer bonding with a bonding dielectric stack down to 170nm. The top devices offer similar performance as the high temperature bulk finfet technology for LSTP applications. The use of TiN/TiAl/TiN/HfO2 gate stack provides the proper threshold voltage adjustment while the insertion of the LaSiOx dipole improves device performance and brings the BTI reliability within specification at low temperature.

2:00 PM - 2:25 PM

7.2 Breakthroughs in 3D Sequential Technology, *L. Brunet, C. Fenouillet-Beranger, P. Batude, S. Beaurepaire, F. Ponthenier,2, N. Rambal,2, V. Mazzocchi, J-B. Pin**, P. Acosta-Alba, S. Kerdiles, P. Besson*, H. Fontaine, T. Lardin, F. Fournel, V. Larrey, F. Mazen, V. Balan, C. Morales, C. Guerin, V. Jousseaume, X. Federspiel*, D. Ney*, X. Garros, A. Roman,2, D. Scevola,2, P. Perreau, F. Kouemeni-Tchouake, L. Arnaud, C. Scibetta, S. Chevalliez, F. Aussenac, J. Aubin***, S. Reboh, F. Andrieu, S. Maitrejean, M. Vinet, CEA-LETI, *STMicroelectronics, **Applied Materials Inc., *** SCREEN LASSE*

In this paper, we present technological levers to bring 3D sequential integration compatible with industrial requirements. First, in term of low temperature challenges, low resistance gate stack have been achieved using nanosecond laser and results of a full 500°C raised source & drain (RSD) epitaxy are also presented. Then, integration of intermediate Back End Of Lines (iBEOL) levels is studied from the contamination management to the thermal stability in terms of reliability and low-k morphology. Finally, a Smart CutTM process above a CMOS wafer is presented for the first time.

2:25 PM - 2:50 PM

7.3 Hybrid bonding for 3D stacked image sensors: impact of pitch shrinkage on interconnect robustness, *J. Jourdon,, S. Lhostis, S. Moreau**, J. Chossat, M. Arnoux***, C. Sart, Y. Henrion, P. Lamontagne, L. Arnaud**, N. Bresson**, V. Balan**, C. Euvrard**, Y. Exbrayat**, D. Scevola, E. Deloffre, S. Mermoz, A. Martin***, H. Bilgen, F. Andre, C. Charles, D. Bouchu**, A. Farcy, S. Guillaumet, A. Jouve**, H. Fremont*, and S. Cheramy**, STMicroelectronics, *University of Bordeaux, **CEA-LETI, ***STMicroelectronics*

We present the first 3D-stacked CMOS Image Sensor with a bonding pitch of 1.44 µm. The influence of the hybrid bonding pitch shrinkage (8.8 to 1.44 µm) from the process point of view to a functional device via the robustness aspect is studied. Smaller bonding pads do not lead to any specific failure

2:50 PM - 3:15 PM

7.4 Embedded Select in Trench Memory (eSTM), best in class 40nm floating gate based cell: a process integration challenge (Invited), *S. Niel, F. La Rosa, A. Regnier , M. Mantelli, F. Trenteseaux, G. Ghezzi, A. Marzaki, Q. Hubert, J. Delalleau, T. Cabout ,F. Maugain, E. Lepape, L. Baron, A. Champenois, D. Galpin, N. Cherault, S. Audran, L. Parmigiani, P. Gouraud, B. Duclaux, Y. Escarabajal, F. Baudin, E. Beche, B. Saidi, V. Arnal, STMicroelectronics*

This paper discusses an innovative architecture of charge storage NVM cell, which outpaces state-of-the-art in term of bit-cell area. This new concept of memory cell is used today in production for

microcontrollers. After cell architecture and activation description, we will present process flow integration challenges, process optimizations and single cell characterizations.

3:15 PM Coffee Break

3:40 PM - 4:05 PM

7.5 Highly Reliable Ferroelectric Hf0.5Zr0.5O2 Film with Al Nanoclusters Embedded by Novel Sub-Monolayer Doping Technique, *T. Yamaguchi, T. Zhang, K. Omori, Y. Shimada*, Y. Kunimune*, T. Ide*, M. Inoue, and M. Matsuura, Renesas Electronics Corp., Renesas Electronics Corporation, *Renesas Semiconductor Manufacturing Co.*

Highly reliable ferroelectric (FE) Hf0.5Zr0.5O2 (HZO) film with Al nanoclusters embedded by sub-monolayer doping technique is demonstrated for the first time. Al nanoclusters increase the remnant polarization (Pr) and reduce the voltage necessary for polarization switching. Furthermore, the program and erase endurance at the cycle of more than 250k and the Pr retention at 85ºC for 10 years are achieved. Al nanoclusters are formed by the partial oxidation of sub-monolayer metallic Al embedded in HZO films. Al nanoclusters enhance the large grain growth of the orthorhombic-phase HZO during FE-HZO crystallization annealing. The reduction of grain boundaries caused by the large grain growth with Al nanoclusters effectively reduces the leakage current. As a result, the reliability of the FE HZO film is significantly improved.

4:05 PM - 4:30 PM

7.6 Interface Dipole Modulation Memory based on Multi-stacked HfO2/SiO2 MOS Structure, *N. Miyata, J. Nara*, T. Yamasaki*, K. Sumita, R. Sano**, and H. Nohira**, AIST, *NIMS, **Tokyo City University*

We report an interface dipole modulation (IDM) in HfO2-based MOS stack structures. Experimental evidence for IDM was exhibited, and rearrangement of interfacial Ti-O configuration was theoretically demonstrated to cause IDM. Multi-stack HfO2/SiO2 IDM structures are promising in terms of a low temperature process, practical memory window, and stable potential switching.

4:30 PM - 4:55 PM

7.7 Ge-based Non-Volatile Logic-Memory Hybrid Devices for NAND Memory Application, *N. Wei, B. Chen, Z. Zheng, Z. Cai, R. Zhang, R. Cheng, S-W Lee, Y. Zhao, Zhejiang University*

In this work, novel Ge-on-Insulator (GeOI) MOSFETs with resistive-switchable gate stacks, named RFETs, are proposed and experimentally realized. The junctionless GeOI RFET and typical inversion-mode GeOI RFET are fabricated and both types of RFETs exhibit decent transistor behaviors and RRAM characteristics at the same time. Furthermore, by utilizing these two types of RFETs, a new GeOI RFET-based NAND memory is constructed and the memory functions of the arrays are experimentally demonstrated. This RFET-based NAND memory has a simple cell structure and very simplified I/O circuit in comparison with the conventional flash memory and non-volatile memory such as RRAM and MRAM. Therefore, RFETs should be promising for the applications of next-generation high density, low power memory and in-memory computing and neuromorphic computing.

Session 8: Power Devices - Advances in Silicon Carbide and Gallium Oxide Silicon Power Devices

Monday, December 3, 1:30 PM

Continental Ballroom 7-9

Co- Chairs: S. Ekkanath Madathil, University of Sheffield

S. Harada, AIST

1:35 PM - 2:00 PM

8.1 0.63 mΩcm^2 / 1170 V 4H-SiC Super Junction V-groove trench MOSFET, *T. Masuda, Y. Saito, T. Kumazawa, T. Hatayama, and S. Harada, National Institute of Advanced Industrial Science and Technology*

4H-SiC super junction, 0.63 mΩcm^2 and 1170 V, V-groove trench MOSFETs (SJ-VMOSFET) were demonstrated. The specific on-resistance (Ron, sp) of the SJ-VMOSFET is the lowest ever among all the reported SiC-MOSFETs with the blocking voltage (Bv) over 600 V. Superior electrical properties were realized with the structural combination of the V-groove MOS channel and the charge balance at super junction area. The $R_{on, sp}$ analysis of SJ-VMOSFET was carried out after mounted on a TO-268 5pin package having a Kelvin source terminal. The V-groove {03 8} channels could keep a high inversion mobility even in increasing doping concentration over $1x10^{18}$ cm-3. The excellent-static and –dynamic performances of SJ-VMOSFET were allowed to realize the ultra-low loss switching applications.

2:00 PM - 2:25 PM

8.2 First Demonstration of Dynamic Characteristics for SiC Superjunction MOSFET Realized using Multi-epitaxial Growth Method*, S. Harada, Y. Kobayashi, S. Kyogoku, T. Morimoto, T. Tanaka, M. Takei, and H. Okumur, AIST*

A 1.2 kV-class superjunction (SJ) UMOSFET was realized using a multi-epitaxial growth method. The dynamic characteristics were characterized, and the potential of a product level device was identified for the first time. The switching characteristics with Schottky barrier diode showed no degradation in spite of the large drain-source capacitance (CDS). The reverse recovery characteristics of the body diode exhibited a soft recovery which may originate from the large CDS and the short lifetime of minority carrier. A high short circuit capability comparable to a non-SJ device was demonstrated.

2:25 PM - 2:50 PM

8.3 Channel engineering of 4H-SiC MOSFETs using sulphur as a deep level donor, *M. Noguchi, T. Iwamatsu, H. Amishiro, H. Watanabe, K. Kita* and N. Miura Mitsubishi Electric Corporation, *The University of Tokyo*

We demonstrated Si-face 4H-SiC MOSFETs using sulphur as a deep level donor in channel region, for the first time. The natures of sulphur in 4H-SiC, that is a donor with large ionization energy, realized lower channel resistance and higher threshold voltage compared with the channels using conventional shallow level donors.

2:50 PM Coffee Break

3:15 PM - 3:40 PM

8.4 Demonstration of 1200V Scaled IGBTs Driven by 5V Gate Voltage with Superiorly Low Switching Loss, *T. Saraya, K. Itou, T. Takakura, M. Fukui, S. Suzuki, K. Takeuchi, M. Tsukud*, Y. Numasawa**, K. Satoh***, T. Matsudai#, W. Saito#, K. Kakushima^, T. Hoshii^, K. Furukawa^, M. Watanabe^, N. Shigyo^, K. Tsutsui^, H. Iwai^, A. Ogura**, S. Nishizawa^^, I. Omura^^, H. Ohashi#, and T. Hiramoto, The University of Tokyo, *Green Electronics Research Institute, **Meiji University, ***Mitsubishi Electric Corp., #Toshiba Electronic Devices & Storage Corp., ^Tokyo Institute of Technology, ^^Kyushu University*

Functional trench-gated 1200V-10A class Si-IGBTs, designed based on a three dimensional (3D) scaling concept, were fabricated, and 5V gate voltage switching operation has been demonstrated for the first time. 33% reduction of turn-off loss and 100mV improvement of onstate voltage were achieved, while keeping 1.2kV forward blocking voltage.

3:40 PM - 4:05 PM

8.5 2.44 kV Ga2O3 vertical trench Schottky barrier diodes with very low reverse leakage current,
W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu**, K. Sasaki**, A. Kuramata**, D. Jena and H. Grace Xing, Cornell University, *Kyoto University, **Novel Crystal Technology, Inc.*

High-performance beta-Ga2O3 vertical trench Schottky barrier diodes (SBDs) are demonstrated on bulk Ga2O3 substrates with a halide vapor phase epitaxial layer. A breakdown voltage (BV) of 2.44 kV, Baliga's figure-of-merit (BV2/Ron) of 0.39 GW/cm2 from DC measurements and 0.45 GW/cm2 from pulsed measurements are achieved, all of which are the highest among beta-Ga2O3-based power devices. A lowest reverse leakage current density below 1 uA/cm2 until breakdown is observed on devices with a fin width of 1-2 um, thanks to the reduced surface field (RESURF) effect provided by the trench SBD structure. The specific on-resistance is found to reduce with increasing area ratio of the fin-channels following a simple relationship. The reverse leakage current agrees well with simulated results considering the barrier tunneling and barrier height lowering effects. The breakdown of the devices is identified to happen at the trench bottom corner, where a maximum electric field over 5 MV/cm could be sustained. This work marks a significant step toward reaching the promise of a high figure-of-merit in beta-Ga2O3.

Session 9: Modeling and Simulation - Modeling and Simulation of Negative Capacitance Transistors
Monday, December 3, 1:30 PM
Plaza A
Co- Chairs: L. Smith, Synopsys
N. Xu, Samsung

1:35 PM - 2:00 PM

9.1 Multi-Domain Dynamics of Ferroelectric Polarization and its Coherency-Breaking in Negative Capacitance Field-Effect Transistors, *H. Ota, T. Ikegami, K. Fukuda, J. Hattori, H. Asai, K. Endo, S. Migita and A. Toriumi*, National Institute of Advanced Industrial Sceince and Technology (AIST) *The University of Tokyo*

In this paper, we, for the first time, clarified the multidomain dynamics of ferroelectric polarization in the Negative Capacitance Field-Effect Transistors (NCFETs) by an in-house Technology Computer-Aided Design (TCAD) module. It enables self-consistent simulations among the time-dependent Landau-Khalatnikov equation and the other equations that govern operation of FETs. Our simulation reveals that domain-wall thickness Tdw, which reflects a correlation strength between domains predominates coherency of the NC polarization. In a strong correlation (large Tdw) case, a coherent NC polarization is realized at least to a degree of Tdw. On the other hand, in a weak correlation (small Tdw) case, perturbation from peripherals easily leads to incoherence of polarization, where a uniform polarization is split into multiple spontaneous polarization domains. This coherency breaking found to give rise to deteriorated voltage amplification of NC. Design methodology to maintain the NC coherency is also proposed.

2:00 PM - 2:25 PM

9.2 Modeling of Multi-domain Switching in Ferroelectric Materials: Application to Negative Capacitance FETs, *A. Dasgupta, P. Rastogi*, D. Saha*, A. Gaidhane*, A. Agarwal* and Y. S. Chauhan*, Univ. of California, Berkeley, *IIT Kanpur*

We present a new multi-domain model for polarization switching in ferroelectric materials. The computationally efficient model captures the time evolution of multi-domain ferroelectrics with good accuracy along with the frequency dependent switching behavior. We have fabricated (PVDF) and measured P-E characteristics of PZT and PVDF capacitors and have validated the model with measurements. The model allows the visualization of time dependent domain switching allowing further

physical insights. We have also proposed a method to extract the distribution of domain orientations experimentally.

2:25 PM - 2:50 PM
9.3 On the Microscopic Origin of Negative Capacitance in Ferroelectric Materials: A Toy Model (Invited), *A. Khan, Georgia Institute of Technology*

We present a simple, physical explanation of underlying microscopic mechanisms that lead to the emergence of the negative phenomena in ferroelectric materials. The material presented herein is inspired by the pedagogical treatment of ferroelectricity by Feynman and Kittel. In a toy model consisting of a linear one dimensional chain of polarizable units (i.e., atoms or unit cells of a crystal structure), we show how simple electrostatic interactions can create a microscopic, positive feedback action that leads to negative capacitance phenomena. We point out that the unstable negative capacitance effect has its origin in the so called "polarization catastrophe" phenomenon which is essential to explain displacement type ferroelectrics. Furthermore, the fact that even in the negative capacitance state, the individual dipole always align along the direction of the local electrical field not opposite is made clear through the toy model. Finally, how the "S"-shaped polarization vs. applied electric field curve emerges out of the electrostatic interactions in an ordered set of polarizable units is shown.

2:50 PM Coffee Break

3:15 PM - 3:40 PM
9.4 Effect of Polycrystallinity and Presence of Dielectric Phases on NC-FinFET Variability, *Y.-K. Lin, M.-Y. Kao, H. Agarwal, Y-H Liao, P. Kushwaha, K. Chatterjee, J. Pablo Duarte, H-L Chang, S. Salahuddin, and C. Hu University of California, Berkeley*

A Monte Carlo TCAD simulation study of the impact of polycrystallinity and dielectric phases of the ferroelectric film on an 8/7 nm node NC-FinFET is presented. The study considers the random variation of ferroelectric remnant polarization (Pr) and the presence of dielectric phases. In order to keep the ferroelectric-film induced device variability less than those induced by other sources (RDF, GER, FER, and MGG), we found that the DE content must be less than 20%, which is theoretically possible, and the grain to grain Pr variations less than 27%. While uniform single-crystalline ferroelectric film would provide the least device variation, we found 4 nm grains to produce less device variability than 5.3 nm grains due to the larger number of grains in the channel area.

3:40 PM - 4:05 PM
9.5 A simulation based study of NC-FETs design: off-state versus on-state perspective, *T. Rollo, H. Wang, G. Han*, D. Esseni, Università degli Studi di Udine, *Xidian University*

Analytical and numerical models are presented for a better insight of physics and design of Ferroelectric-NCFETs. A steep-slope hysteresis-free design is difficult to obtain, while on-state enhancement is more feasible and improves both SS and on-current. NC-FETs reduce temperature sensitivity compared to baseline FETs, but magnify the sensitivity to thicknesses.

Session 10: Optoelectronics, Displays, and Imagers - Image Sensors
Monday, December 3, 1:30 PM
Plaza B
Co- Chairs: T. Sakai, NHK
L. Grant, OmniVision

1:35 PM - 2:00 PM

10.1 1.5µm dual conversion gain, backside illuminated image sensor using stacked pixel level connections with 13ke- full-well capacitance and 0.8e- noise, *V. C. Venezia, A. C-W Hsiung, K. Ai, X. Zhao, Zhiqiang Lin, Duli Mao, Armin Yazdani, Eric A. G. Webster, L. A. Grant, OmniVision Technologies*

A 1.5µm pixel size, 8 mega pixel density, dual conversion gain (DCG), back side illuminated CMOS image sensor (CIS) is described having a linear full-well capacity (FWC) of 13ke- and total noise of 0.8e- RMS at 8x gain. The sensor adopts a world smallest 1.5µm pitch, stacked pixel-level connection (SPLC) technology with greater than 8M connections, maximizing fill-factor of the photodiode and dimensions of the associated transistor dimensions to achieve a large FWC and low noise performance at the same time. In addition, by allocating transistors into two different layers, the DCG function can be realized with 1.5µm pixel size.

2:00 PM - 2:25 PM
10.2 A 0.68e-rms Random-Noise 121dB Dynamic-Range Sub-pixel architecture CMOS Image Sensor with LED Flicker Mitigation, *S. Iida, Y. Sakano, T. Asatsuma, M. Takami, I. Yoshiba, N. Ohba, H. Mizuno, T. Oka, K. Yamaguchi, A. Suzuki, K. Suzuki, M. Yamada, M. Takizawa, Y. Tateshita, and K. Ohno, Sony Semiconductor*

This is a report of a CMOS image sensor with a sub-pixel architecture having a pixel pitch of 3 um. The aforementioned sensor achieves both ultra-low random noise of 0.68e-rms and high dynamic range of 121 dB in a single exposure, further realizing LED flicker mitigation.

2:25 PM - 2:50 PM
10.3 A 24.3Me- Full Well Capacity CMOS Image Sensor with Lateral Overflow Integration Trench Capacitor for High Precision Near Infrared Absorption Imaging, *M. Murata, R. Kuroda, Y. Fujihara, Y. Aoyagi, H. Shibata*, T. Shibaguchi*, Y. Kamata*, N. Miura*, N. Kuriyama*and S. Sugawa, Tohoku University, *LAPIS Semiconductor Miyagi Co., Ltd.*

This paper presents a 16um pixel pitch CMOS image sensor exhibiting 24.3Me- full well capacity with a record spatial efficiency of 95ke-/um2 and high quantum efficiency in near infrared waveband by the introduction of lateral overflow integration trench capacitor on a very low dopant concentration p-type Si substrate. A diffusion of 5mg/dl concentration glucose was clearly visualized by an over 71dB SNR absorption imaging at 1050nm.

2:50 PM Coffee Break

3:15 PM - 3:40 PM
10.4 A HDR 98dB 3.2µm Charge Domain Global Shutter CMOS Image Sensor (Invited), *A. Tournier, F. Roy, Y. Cazaux*, F. Lalanne, P. Malinge, M. Mcdonald, G. Monnot**, N. Roux**, STMicroelectronics, **CEA Leti, **STMicroelectronics*

We developed a High Dynamic Range (HDR) Global Shutter (GS) pixel for automotive applications working in the charge domain with dual high-density storage node using Capacitive Deep Trench Isolation (CDTI). With a pixel size of 3.2µm, this is the smallest reported GS pixel achieving linear dynamic range of 98dB with a noise floor of 2.8e-. The pinned memory isolated by CDTI can store 2 x 8000e- with dark current lower than 5e-/s at 60°C. A shutter efficiency of 99.97% at 505nm and a Modulation Transfer Function (MTF) at 940nm better than 0.5 at Nyquist frequency is also reported.

3:40 PM - 4:05 PM
10.5 High Performance 2.5um Global Shutter Pixel with New Designed Light-Pipe Structure, *T. Yokoyama, M. Tsutsui,Y. Nishi, I. Mizuno, V. Dmitry, A. Lahav TowerJazz*

We developed a 2.5um global shutter (GS) CMOS image sensor pixel using an advanced Light-Pipe (LP) structure designed with novel guidelines. To the best of our knowledge, it is the smallest reported GS pixel in the world. The developed pixel shows an excellent Quantum Efficiency (QE), Angular Responses (AR) and very low Parasitic Light Sensitivity (PLS). Also, even in oblique light condition of 10 degrees, the 1/PLS is maintained to about half value. These key characteristics allow development of ultra-high resolution sensors, industrial cameras with wide aperture lenses and low form factors optical modules for GS mobile applications.

4:05 PM - 4:30 PM

10.6 Back-Illuminated 2.74 µm-Pixel-Pitch Global Shutter CMOS Image Sensor with Charge-Domain Memory Achieving 10k e- Saturation Signal, *Y. Kumagai, R. Yoshita, N. Osawa, H. Ikeda, K.Yamashita, T. Abe, S. Kudo, J. Yamane, T. Idekoba, S. Noudo, Y. Ono, S.Kunitake, M. Sato, N. Sato, T. Enomoto, K. Nakazawa, H. Mori, Y. Tateshita, and K. Ohno, Sony Semiconductor*

A 3208×2184 global shutter image sensor with back-illuminated architecture is implemented in a 90 nm/65 nm imaging process. The sensor, having 2.74 µm-pitch-pixels, achieves 10000 electrons full-well capacity and -80 dB parasitic light sensitivity. Furthermore, 13.8 e-/s dark current at 60°C and 1.85 erms random noise are obtained. In this paper, the structure of a pixel with memory along with saturation enhancement technology is described.

Session 11: Process and Manufacturing Technology - Material and Processes for Advanced Silicon Technologies

Tuesday, December 4, 9:00 AM
Grand Ballroom A
Co- Chairs: S. Maitrejean, CEA-LETI
S. Ecoffey, University of Sherbrooke

9:05 AM - 9:30 AM

11.1 Conformal, Wafer-Scale and Controlled Nanoscale Doping of Semiconductors Via the iCVD Process, *J. H. Kim, H. K. Park, K. Y. Pak, A. Yoon*, Y. S. Kim*, S. G. Im, W. S. Hwang** and B. J. Cho, KAIST, *Lam Research Corporation, **Korea Aerospace University*

For the first time, a novel doping technique using an initiated CVD (iCVD) process was developed, facilitating the conformal, wafer-scale and controlled nanoscale doping of semiconductors at a high concentration. iCVD poly(boron allyloxide) (pBAO) and poly(triallyl phosphate) (pTAP) were used as a p-type and n-type dopant diffusion source, respectively. In detail, an optimized integration process was developed involving copolymer p(BAO-co-V3D3) passivation for pBAO and double-step deposition for pTAP. It was found that a dopant-containing polymer layer with a sub-10-nm thickness provided a high doping concentration at a shallow junction depth (10 nm) for both the p-type (10^{20} cm-3) and the n-type (10^{21} cm-3). Furthermore, the conformality and dopant distribution of the iCVD polymer layer were investigated using a high-aspect-ratio Si fin (5:1). The SOI nFET with iCVD doping at the source/drain regions exhibited better subthreshold swing and on-current values than a SOI nFET with conventional ion-implantation doping. Compared to other diffusion doping methods, the iCVD process could achieve lower sheet resistance.

9:30 AM - 9:55 AM

11.2 Low Temperature Sputtered Graphenic Carbon Enables Highly Reliable Contacts to Silicon, *M. Stelzer, M. Jung, U. Wurstbauer, A.W. Holleitner, and F. Kreupl, Technical University of* Munich

Titanium silicide (TiSi) contacts are commonly used metal-silicon contacts but are known to diffuse into the active region under high current stress. Recently we demonstrated that graphenic carbon (GC) deposited by CVD has the same low Schottky barrier on silicon as TiSi, but a much improved reliability against high current stress. The drawback of the CVD-GC is the required deposition temperature of ~ 900 °C. In this paper we demonstrate now that the deposition of graphenic carbon is possible at 100 - 400°C by a modified sputter process. We show that the sputtered carbon-silicon (SC-Si) contact is over 1 billion times more stable against high current stress pulses than the conventionally used TiSi-Si junction, while it has the same or even a lower Schottky barrier. Doping SC by nitrogen (CN) leads to an even lower resistivity and improved stability. The finding that there is a low temperature approach for using the superb carbon properties has important consequences for the reliability of contacts to silicon and opens up the use of GC in a plethora of other applications.

9:55 AM - 10:20 AM

11.3 Location-controlled-grain technique for monolithic 3D BEOL FinFET Circuits, *C-C Yang, T-Y Hsieh***, P-T Huang*, K-N Chen *, W-V Wu*, S-W Chen, C-H Chang, C-H Shen, J-M Shieh, C. Hu**, Meng-C Wu***, W-K Yeh, National Nano Device Laboratories, *National Chiao Tung University, **also with University of California, Berkeley, ***National Tsing Hua University*

A location-controlled-grain technique is presented for fabricating BEOL monolithic 3D FinFET ICs over SiO2. The grain-boundary free Si FinFETs thus fabricated exhibit steep sub-threshold swing (<70mV/dec.), high driving currents (n-type: 363 uA/um and p-type: 385 uA/um), and high Ion/Ioff (>10^6). According to simulation, the thickness of interlayer dielectric layer plays an important role and shall be thicker than 250nm for sequential pulse laser crystallization process to keep bottom device and interconnect at less than 400ºC

10:20 AM - 10:45 AM

11.4 Novel Materials and Processes in Replacement Metal Gate for Advanced CMOS Technology, *R. Bao, S. Hung*, M. Wang, K. Chung, S. Barman*, S. A Krishnan*, Y. Yang*, W. Tang*, L. Li*, Y. Lin*, M. S Chan*, Z. Chen*, X. Miao, M. Hopstaken, R. A Conti, H. Jagannathan, M. P Chudzik*, D. McHerron, B. S Haran, S. Natarajan*, IBM, *Applied Materials*

This paper addresses novel approaches at material and integration fronts for gate applications. Material wise, new n work function metal (WFM) material is explored to address the need for reducing gate resistance and maintaining proper Vt at 20Å or less WFM thickness. Integration wise, next generation dipole is tested with various process sequences to address the need in lowering overall thermal budget at the gate level for advanced architectures, such as scaled FinFET and Nanosheets.

10:45 AM Coffee Break

11:10 AM - 11:35 AM

11.5 Why GeO_2 growth on Ge is suppressed and GeO_2/Ge stack is much improved in high pressure O_2 oxidation?, *X. Wang and A. Toriumi, The University of Tokyo*

This paper reports for the first time a new kinetic model of thermal oxidation of Ge that considers both O-vacancy and atomic O diffusion as a function of O2 pressure. The model is based on newly obtained results that Ge oxidation is described by kinetics completely different from the Deal-Grove model and that it exhibits anomalous O2 pressure dependence. Furthermore, new experimental results have been obtained in the oxidation of SiO2/GeO2/Ge, GeO2/SiO2/Si and GeO2/SiO2/Ge stacks. They support new kinetic model of Ge oxidation as well. This is critically important for high quality Ge gate stacks, as the Deal-Grove model have played a considerable role in Si technology.

11:35 AM - 12:00 PM

11.6 EUV Lithography at Threshold of High-Volume Manufacturing (Invited), *A. Yen, ASML*

A throughput of >140 wph has been achieved on NXE:3400B EUV scanners at a source power of 250W. Power degradation rate has been concurrently driven down so that high system throughput can be maintained. Improvement in mask-area cleanliness has resulted in over 1,500 exposures per fall-on particle, and solid progress on the pellicle has been made.

12:00 PM - 12:25 PM

11.7 Half pitch 14 nm direct pattering with Nanoimprint lithography, *T. Nakasugi, T. Kono, K. Fukuhara, M. Hatano, H. Tokue, M. Komori, H. Tsuda,T. Komukai, K. Takahata, H. Kato, K. Kobayashi, A. Mitra, S. Kobayashi, S. Inoue, T. Higashiki, T. Motokawa*, M. Saito*, S. Kanamitsu*, M. Itoh*, T. Imamura**, K. Matasunaga**, K. Hashimoto**, Y. Kim***, J. Cho***, and W. Jung***, Toshiba Memory Corp, *Kawasaki, **Yokkaichi, Japan, ***SK hynix Inc.*

A half pitch 14 nm direct pattering is demonstrated by Nano-imprint lithography (NIL). A template, fabricated by a self-aligned double patterning on a mask-blanks-template, provides a resist pattern with smooth vertical sidewalls. It enables a 14 nm etched pattern. A NIL system NZ2C used for this experiment shows good performance.

Session 12: Sensors, MEMS, and BioMEMS - Integrated Ion and Gas Sensors

Tuesday, December 4, 9:00 AM

Continental Ballroom 1-3

Co- Chairs: J-W Han, NASA

X. Wang, Tsinghua University

9:05 AM - 9:30 AM

12.1 All CMOS Integrated 3D-Extended Metal Gate ISFETs for pH and Multi-Ion (Na+, K+, Ca2+) Sensing, *J.-R. Zhang, M. Rupakula, F. Bellando, E. Garcia Cordero, J. Longo*, F. Wildhaber*, G. Herment, H. Guérin*, A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne, *Xsensio S.A., EPFL*

This paper reports for the first time, smart 3D-Extended-Metal-Gate Ion-Sensitive-Field-Effect-Transistors (3D-EMG-ISFETs), with unique figures of merit: (i) extremely-low-power (down to a record value of 2 pW per sensor under excellent linearity), (ii) all CMOS integrated, (iii) high performance pH and multi-ion (Na+, K+, Ca2+) sensing, and, (iv) uniquely low cross sensitivity experimentally proven. Detailed electrical DC and dynamic characterizations show excellent sensitivities (56.8 mV/pH, -58mV/dec for Na+, -49.5 mV/dec for K+, and -21.9 mV/dec for Ca2+) and high selectivity of each ion sensor against 4 different ions that usually coexist in biofluids, all achieved on same CMOS die. Furthermore, unprecedented results show that the threshold voltage (Vth) variability of such CMOS ISFET is reduced by 78 times. We report a Vth drift rate in liquid conditions of 0.67 mV/h, decreased by one order of magnitude compared to other state of the art CMOS ISFETs. Overall, the reported experimental achievements, supported by SPICE calibrated behavioral model simulations results shown in this paper, are expected to greatly enhance the predictability of high performance multi-analyte ISFETs, which is a big step towards ISFET sensor system mass production.

9:30 AM - 9:55 AM

12.2 High Resolution Ion Detector (HRID) by 16nm FinFET CMOS Technology, *P-C Liou, T-H Lee*, C-P Wang, Y-L Chueh*, Y-D Chih**, J. Chang**, C J Lin, Y-C King, Institute of Electronics Engineering, National Tsing Hua University, *National Tsing Hua University, **Taiwan Semiconductor Manufacturing Company*

A novel approach for the ion-sensing of electrolyte solution, using specially designed CMOS FinFET process compatible floating-gate (FG) device is proposed. With the self-balancing readout scheme, the floating gate based pH sensor shows a maximum pH readout sensitivity of 115 mV/pH. Through a laterally coupling structure to the metal floating gate of a FinFET, its channel potential can be controlled both by the read gate as well as the sensing gate. In additional, this novel scheme also enables high linearity pH sensing in the target sensing range, readily adjusted by coupling ratios and biasing levels.

9:55 AM - 10:20 AM

12.3 Highly Performant Integrated pH-Sensor Using the Gate Protection Diode in the BEOL of Industrial FDSOI, *G. T. Ayele, S. Monfray, S. Ecoffey**, F. Boeuf, J-P. Cloarec*, D. Drouin**, and A. Souifi*, STMicroelectronics, *INL-Université de Lyon, **LN2, **IT-Université de Sherbrooke*

This is the first demonstration of a CMOS pH-sensor using the gate protection diode of standard FDSOI transistors in the BEOL. The extremely steep switching of the drain current induced by an exploitation of the DIBL effect is used for fabrication of extremely sensitive pH-sensors. The back gate voltage at which the abrupt switching of drain current occurs depends on the potential at the gate protection diode. Integrating the pH sensing film on this diode BEOL metal, the shift depends on the pH value of the liquid which creates a proportional potential. The abrupt switching (as small as 9 mV/decade) of the drain current can give a theoretical maximum sensitivity of 6.6 decade of drain current change per unit pH. In this paper, we report an experimental sensitivity of 1.25 decade/pH which is superior to state-of-the-art CMOS pH sensors which have a maximum sensitivity of 0.9 decade/pH.

10:20 AM Coffee Break

10:45 AM - 11:10 AM

12.4 Very Large Scale Integration Optomechanics: a cure for loneliness of NEMS resonators*?* (Invited)*, M. Hermouet, M. Sansa, M. Martial Defoort, L. Banniard, S. Dominguez-Medina*, S. Fostner, U. Palanchoke, A. Fafin, M. Gely, L. Hutin, C. Plantier, E. Rolland, C. Tabone, G. Usai, T. Ernst, P. Villard, G. Billiot, P. Mattei, G. Nonglaton, C. Fontelaye, C. Barrois, O. Castany, E. Gil Santos***, P. E. Allain***, E. Vernhes#, P. Boulanger#, A. Brenac##, C. Masselon*, I. Favero***, T. Alava, G. Jourdan and S. Hentz*, Univ. Grenoble Alpes, CEA LETI, *CEA, BIG, **Inserm, ***Université Paris Diderot, #Université Paris-Saclay, ##Univ. Grenoble Alpes*

The first Very Large Scale Integration process with variable shape beam lithography for optomechanical devices is presented. State of the art performance was obtained with silicon microdisk resonators showing 1 million optical quality factors and 10-17m.Hz(-1/2) displacement resolution. Single-particle mass spectrometry could be performed with these optomechanical resonators in vacuum. The devices retained high performance when directly immersed in liquid media, allowing for biosensing experiments. These results open the door to large, dense arrays of optomechanical sensors.

11:10 AM - 11:35 AM

12.5 SiC-FET-type NOx Sensor for High-Temperature Exhaust Gas, *Y. Sasago, H. Nakamura, T. Odaka, A. Isobe, S. Komatsu, Y. Nakamura, T. Yamawaki, C. Yorita, N. Ushifusa, K. Yoshikawa, K. Ono, Y. Anzai, S. Machida, M. Kinoshita, K. Fujisaki, T. Usagawa, K. Okishiro*, and Y. Sugiyama*, Hitachi, Ltd., *Hitachi Metals, Ltd.*

We have developed a SiC-FET-type gas sensor that enables highly sensitive NO detection in high-temperature exhaust gas. The gate of the FET is a gas detection layer consisting of yttria-stabilized zirconia, nickel oxide, and platinum, which are deposited on the SiC substrate. The threshold voltage of the FET depends on the NO concentration. Experimental results demonstrate that the FET-type sensor can detect

NO concentration less than 1 ppm, thus meeting the specifications required to satisfy the strict regulations for exhaust gas in the next generation.

11:35 AM - 12:00 PM
12.6 A Si FET-type Gas Sensor with Pulse-driven Localized Micro-heater for Low Power Consumption, *Y. Hong, S. Hong, D. Jang, Y. Jeong, M. Wu, G. Jung, J-H Bae, J. S. Kim, K. S. Chang*, C. B. Jeong*, C. S. Hwang, B.-G. Park, and J-H Lee, Seoul National University, *Korea Basic Science Institute*

A poly-Si localized micro-heater for Si FET-type gas sensor is proposed in this paper. The fabricated gas sensor has an air gap under the heater to prevent the heat dissipation. It is found that the micro-heater itself can read the temperature by applying a read bias of less than 0.5 V. The heating and cooling times of the heater are ~200 μs and ~100 μs, respectively. Measured temperatures are verified by infrared thermal microscopy. The NO2- and H2S-sensing tests with the heater are successfully performed by using a pulse scheme.

Session 13: Nano Device Technology - Nano-Devices for Low-Power Technologies
Tuesday, December 4, 9:00 AM
Continental Ballroom 4
Co- Chairs: L-E Wernersson, Lund University
W. Zhu, University of Illinois at Urbana-Champaign

9:05 AM - 9:30 AM
13.1 ECRAM as Scalable Synaptic Cell for High-Speed, Low-Power Neuromorphic Computing, *J. Tang, D. Bishop, S. Kim, M. Copel, T. Gokmen, T. Todorov, S Shin, K-T Lee, P. Solomon, K. Chan, W. Haensch, J. Rozen IBM TJ WatsonResearch*

We have demonstrated a nonvolatile ECRAM that relies on electrochemically driven Li-ion intercalation for neuromorphic computing. It shows near-ideal switching symmetry and linearity, large dynamic range, up to 1000 discrete conductance states, and excellent endurance. Most importantly, sub-10 ns programming and sub-micron devices are both demonstrated for the first time.

9:30 AM - 9:55 AM
13.2 SoC Logic Compatible Multi-Bit FeMFET Weight Cell for Neuromorphic Applications, *K. Ni, J. A. Smith, B. Grisafe, T. Rakshit*, B. Obradovic*, J. A. Kittl*, M. Rodder* and S. Datta*
*University of Notre Dame, Notre Dame, *Samsung Advanced Logic Lab*

We demonstrate an SoC logic compatible ferroelectric-metal field effect transistor (FeMFET) digital 2-bit weight cell by monolithic BEOL integration of a ferroelectric (FE) capacitor with the gate of a conventional Si HK/MG MOSFET. Through optimization of the area ratio between the FE capacitor and the MOSFET, we show: 1) program/erase write voltages can be scaled down to logic compatible level, ±1.8 V, simplifying write circuitry; 2) write speed of 100ns; 3) write endurance $>10^{10}$ cycles without degradation due to elimination of charge trapping in FE; 4) 2 bits/cell achieving software levels of accuracy for inference on MNIST training database; 5) state retention approaching 10^4 s for a depolarization field of 0.3 MV/cm; 6) Multi-port (independent read and write) operations.

9:55 AM - 10:20 AM
13.3 Experimental Demonstration of Ferroelectric Spiking Neurons for Unsupervised Clustering, *Z. Wang, B Crafton, J. Gomez*, R. Xu**, A. Luo**, Z. Krivokapic***, L. Martin**, S. Datta*, A. Raychowdhury, A. Islam Khan, Georgia Institute of Technology, *University of Notre Dame, **University of California, ***Lawrence Berkeley National Laboratory*

We report the first experimental demonstration of ferroelectric field-effect transistor (FEFET) based spiking neurons. A unique feature of the ferroelectric (FE) neuron demonstrated herein is the availability of both excitatory and inhibitory input connections in the compact 1T-1FEFET structure, which is also reported for the first time for any neuron implementations. Such dual neuron functionality is a key requirement for bio-mimetic neural networks and represents a breakthrough for implementation of the third generation spiking neural networks (SNNs)—also reported herein for unsupervised learning and clustering on real world data for the first time. The key to our demonstration is the careful design of two important device level features: (1) abrupt hysteretic transitions of the FEFET with no stable states therein, and (2) the dynamic tunability of the FEFET hysteresis by bias conditions which allows for the inhibition functionality. Experimentally calibrated, multi-domain Preisach based FEFET models were used to accurately simulate the FE neurons and project their performance at scaled nodes. We also implement an SNN for unsupervised clustering and benchmark the network performance across analog CMOS and emerging technologies and observe (1) unification of excitatory and inhibitory neural connections, (2) STDP based learning, (3) lowest reported power (3.6nW) during classification, and (4) a classification accuracy of 93%.

10:20 AM - 10:45 AM

13.4 Near Hysteresis-Free Negative Capacitance InGaAs Tunnel FETs with Enhanced Digital and Analog Figures of Merit below VDD=400mV, *A. Saeidi, A. S. Verhulst*, I. Stolichnov, A. Alian*, H. Iwai**, N. Collaert*, and A. M. Ionescu, EPFL, *imec, **Tokyo Institute of Technology*

We report the universal boosting impact of a true negative capacitance (NC) effect on digital and analog performances of Tunnel FETs (TFETs), mirrored for the first time in near hysteresis-free experiments and exploiting the S-shaped polarization characteristics. Well behaved InGaAs planar TFETs with a minimum swing of 55 mV/dec at room temperature are combined with high-quality single crystalline PZT capacitors, placed in series with the gate. When fully satisfying the exact NC matching conditions by a single crystalline ferroelectric that can perform a mono-domain state, a hysteresis-free (sub-10 mV over 4 decades of current) NC-TFET with a sub-thermionic swing and an SSmin of 40 mV/dec is demonstrated for the first time. In other devices, improvement in the subthreshold swing, down to 30 mV/dec, and analog current efficiency factor, up to 150 V-1, are achieved in NC-TFETs with a hysteresis as small as 30 mV. Importantly, the I60 FoM of the TFET is improved up to 2 orders of magnitude. The supply voltage is thereby reduced by 50%, down to 300 mV, providing the same drive current. Our results show that NC can open a new direction as a universal performance booster in the FET design by significantly improving the low I60 and low overdrive of TFETs.

10:45 AM Coffee Break

11:10 AM - 11:35 AM

13.5 An Experimental Study of Heterostructure Tunnel FET Nanowire Arrays: Digital and Analog Figures of Merit from 300K to 10K, *T. Rosca, A. Saeidi, E. Memisevic*, L-E. Wernersson* and A.M.Ionescu, EPF Lausanne, *Lund University*

In this work, we experimentally report the figures of merit of state-of-the-art heterostructure Tunnel Field-Effect-Transistor (TFET) arrays from room (300K) down to cryogenic temperature (10K) at supply voltages below 400mV. We demonstrate here, for the first time, that InAs/InGaAsSb/GaSb Nanowire (NW) TFETs are robust enough to maintain excellent figures of merit over a large temperature range even in devices with a large number arrayed nanowires (here, from 4 to 184 nanowires per device), accounting for technological variability. The investigated Tunnel FETs have temperature-independent min and average subthreshold swings of 45mV/dec/67mV/dec in large NW arrays, versus ~36/45mV/dec in smaller arrays, once the trap-assisted tunneling is removed (from 150K down to 10K). In all NW arrays we observe improvement of the on-current and of maximum transconductance, gmax, at cryogenic temperatures, with very little

dependence of temperature, from 150K to 10K. The paper reports that in the range 150K to 10K only band-to-band-tunneling dominates the analog figures of merit of Tunnel FETs; we measured transconductance efficiencincies higher than 60V-1 for small arrays (breaking the limit of CMOS at RT) and close to 42V-1 for large arrays, for supply volrages smaller than 100mV, offering the possibility to design future energy efficient readouts and analog-to-digital converters. In contrast with cryogenic MOSFETs, Tunnel FETs show almost no hysteresis (<24mV), steep transfer characteristics, are free of kinks in output characteristics, with a unique stability of the swing drift with T, and negligible threshold voltage drift in all arrays configurations.

11:35 AM - 12:00 PM

13.6 High thermal tolerance of 25-nm c-axis aligned crystalline In-Ga-Zn oxide FET, H. Kunitake, *K. Ohshima, K. Tsuda, N. Matsumoto, H. Sawai, Y. Yanagisawa, S. Saga, R. Arasawa, T. Seki, R. Tokumaru, T. Atsumi, K. Kato and S. Yamazaki, Semiconductor Energy Laboratory*

We developed FETs having gate lengths of 25 and 60 nm that are suited for high-temperature operation, using c-axis aligned crystalline In-Ga-Zn oxide (CAAC-IGZO) as its channel material. The FETs with a gate length of 60 nm achieved off-state leakage currents of 10 zA at 150°C. Furthermore, cutoff frequency the FETs with a gate length of 25 nm was 33 GHz at room temperature and changing the temperature from room temperature to 150°C changed the cutoff frequency by only -13% against -36% in Si FET. The CAAC-IGZO FET enables integrated circuits that consume little power even under high-temperature environments.

Session 14 (Focus): Compound Semiconductor and High Speed Devices - Future Technologies Towards Wireless Communications: 5G and Beyond

Tuesday, December 4, 9:00 AM

Continental Ballroom 5

Co- Chairs: K. Makiyama, Fujitsu Laboratories, Ltd.

S-C Shen, Georgia Tech

9:05 AM - 9:30 AM

14.1 Intel 22nm FinFET (22FFL) Process Technology for RF and mmWave Applications and Circuit Design Optimization for FinFET Technology (Invited), *H.-J. Lee, S. Rami, S. Ravikumar, V. Neeli, K. Phoa, B. Sell, and Y. Zhang, Intel Corporation*

Intel 22FFL is a unique FinFET process technology optimized for RF and mmWave applications supporting superior RF performance to planar technologies with both f_t and f_max of NMOS above 300 GHz and 450 GHz respectively. Flicker noise improvement over planar technologies and excellent gain-power efficiency enabling low-power wireless applications are demonstrated.

9:30 AM - 9:55 AM

14.2 GaN HEMTs for 5G Base Station Applications (Invited), *S. Nakajima, Sumitomo Electric Ind., Ltd.*

Many challenges have been overcome in developing highly reliable, cost effective and excellent performance GaN HEMTs. We have focused on GaN HEMT on SiC, and have been shipping commercial GaN HEMTs for the base station market since 2005. The state of the art GaN HEMT has penetrated into the 4G/LTE base station. The efficiency advantage, based on its material properties will also attract 5G power amplifier designers. This paper explains our development history, and overviews the GaN HEMT power amplifiers in the 5G era.

9:55 AM - 10:20 AM

14.3 100-340GHz Systems: Transistors and Applications (Invited), *M.J.W. Rodwell, Y. Fang, J. Rode, J. Wu, B. Markman, S. T. Suran Brunelli, J. Klamkin, M Urteaga*, University of California, Santa Barbara, *Teledyne Scientific Company*

We examine potential 100-340 GHz wireless applications in communications and imaging, and examine the prospects of developing the mm-wave transistors needed to support these applications.

10:20 AM Coffee Break

10:45 AM - 11:10 AM
14.4 Considerations on Design of Highly-Integrated Millimeter-Wave Transceivers in SiGe HBT (Invited), *V. Issakov and S. Trotta, Infineon Technologies AG*

This paper addresses considerations on design of highly-integrated transceivers at mm-wave frequencies. Some aspects are discussed such as SiGe HBT scaling and co-design optimization. A highly-integrated chip operating at V-band for backhaul communication is provided as an example.

11:10 AM - 11:35 AM
14.5 BAW Filters for 5G Bands (Invited), *R. Aigner, G. Fattinger, M. Schaefer, K. Karnati, R. Rothemund, F. Dumont, Qorvo Inc.*

The number of frequency bands requiring BAW filters is expected to grow significantly with the launch of 5G mobile applications. BAW is in particular well suited to address the new radio bands below 6 GHz also referred to as nr-1. RF integration is the only path forward to achieve full connectivity in LTE + 5G wireless due to the complexity of the antenna systems and the resulting coexistence challenges. The article gives an overview and describes recent trends regarding BAW for high frequency bands, wide bandwidth filters, miniaturization and thermal management. Evolution of RF content and the challenges of developing complex RF modules are discussed.

11:35 AM - 12:00 PM
14.6 Tunable Filter Technologies for 5G Communications (Invited)*, D. Peroulis, Purdue University*

This paper presents an overview of available technologies for manufacturing three-dimensional front-end tunable filters for 5G systems. Specifically, we discuss three main technologies: a) RF MEMS, b) Printed Circuit Board (PCB), and c) injection molding. The advantages and drawbacks of each technology are discussed along with relevant proof-of-concept demonstrations. Future directions and improvements are also presented.

Session 15: Circuit and Device Interaction - Emerging Devices for Neural Network and IoT
Tuesday, December 4, 9:00 AM
Continental Ballroom 6
Co- Chairs: C-H Shen, National Nano Device Laboratories
J. Deng, Qualcomm

9:05 AM - 9:30 AM
15.1 Ultra-Low Power 3D NC-FinFET-based Monolithic 3D+-IC with Computing-in-Memory for Intelligent IoT Devices, *F-K Hsueh, W-H Chen*, K-S Li, C-H Shen*, J-M Shieh*, C Y Lee*, B-Y Chen, H-C Chen, C-C Yang, W-H Huang, K-M Chen, G-W Huang, P. Chen*, Y-N Tu*, S. Srinivasa**, V. Narayanan**, M-F Chang*, and W-K Yeh, National Nano Device Laboratories, *National Tsing Hua University, **Pennsylvania State University*

For the first time, ultra-low power ferroelectric FinFET-based monolithic 3D+-IC technology was demonstrated for near memory computing (NMC) circuit. Key enablers are ICP-SiO2 interfacial layer, doped hafnia ferroelectric gate dielectric layer (HfZrO2), and far-infrared laser activation. The proposed stackable 3D NC-FinFETs thus fabricated exhibit record-low sub-threshold swing (NC-nFinFET: 45mV/dec and NC-pFinFET: 50mV/dec) and high Ion/Ioff (>10^6) that enable ultra-low power operation (Vdd=100mV) of CMOS inverter and SRAM. Moreover, above mentioned features of NC-FinFETs and the differential output of SRAM readout enable 50+% area reduction in the near-memory computing circuitry.

9:30 AM - 9:55 AM

15.2 First Demonstration of Ge Ferroelectric Nanowire FET as Synaptic Device for Online Learning in Neural Network with High Number of Conductance State and Gmax/Gmin, *W. Chung, M. Si, and P. D. Ye, Purdue University*

In this paper, optimum weight update scheme for improved linearity and asymmetry of channel conductance potentiation and depression in a Germanium ferroelectric (FE) nanowire FET (NWFET) was experimentally demonstrated and simulated for the first time. It was found that -5 V, 320 pulses and +5 V, 256 pulses both with 50 ns pulse width were the optimum pulsing conditions for potentiation and depression process, respectively. With the optimized scheme, non-linearity for potentiation and depression were extracted to be α_p= 1.22 and α_d= -1.75, respectively resulting in asymmetry ($|\alpha_p - \alpha_d|$) of 2.97 based on models embedded in MLP simulator and NeuroSim [1]. Gmax/Gmin ratio (few hundreds) and number of conductance states (> 256) are both very large. 9 alternating consecutive conductance updates (potentiation followed by depression) were executed to observe variability in conductance profiles. Multilayer perceptron neural network was simulated over 1 million MNIST images with extracted experimental parameters which yielded in online learning accuracy of ~ 88 %.

9:55 AM - 10:20 AM

15.3 STT-MRAM Design Technology Co-optimization for Hardware Neural Networks, *N. Xu,*, Y. Lu, W. Qi, Z. Jiang, X. Peng*, F. Chen, J. Wang, W. Choi, S. Yu*, D. Sin Kim**, Samsung Semiconductor Inc., *Georgia Institute of Technology, **Samsung Electronics,*

The potential of embedded STT-MRAM technology for designing large-scale multiply-and-accumulation (MAC) array circuits are evaluated by comprehensive and holistic design-technology co-optimizations. After careful calibrations with experimental data, post-layout circuit simulations together with GPU-enabled massively parallel Monte Carlo evaluations are conducted to guarantee the designs at rare failure rates. With all critical device and design non-idealities included, architectural emulations are performed to examine the hardware neural network (HNN)'s accuracies and estimate system-level power, performance and area specs. Results indicate the amount of process variation, parasites and error levels to control in order to achieve a feasible solution for STT-MRAM based HNNs.

10:20 AM Coffee Break

10:45 AM - 11:10 AM

15.4 A 68 Parallel Row Access Neuromorphic Core with 22K Multi-Level Synapses Based on Logic-Compatible Embedded Flash Memory Technology, *M. Kim, J. Kim, G. Park, L. Everson, H. Kim, S. Song,**, S. Lee**, and C. H. Kim, University of Minnesota, **Anaflash Inc*

A neuromorphic core utilizing logic-compatible embedded flash cells as non-volatile multi-level synapses is demonstrated in a 65nm CMOS process. A carefully-designed program-verify sequence and bitline voltage regulation scheme allow a record high number of rows to be activated in parallel without compromising the accuracy of the handwritten digital recognition application.

11:10 AM - 11:35 AM

15.5 Interchangeable Hebbian and Anti-Hebbian STDP Applied to Supervised Learning in Spiking Neural Network, *C-C Chang, P-C Chen, B. Hudec, P-T Liu, and T-H Hou National Chiao Tung University*

This work provides a complete framework, including device, architecture, and algorithm, for implementing bio-inspired supervised spiking neural networks (SNNs) on hardware. An analog synapse with atypical dual bipolar resistive-switching (D-BRS) modes demonstrates interchangeable Hebbian spiking-timing-dependent plasticity (STDP) and anti-Hebbian STDP, and it is capable of implementing supervised ReSuMe SNNs in crossbar arrays. By using an "exchange" update scheme, accurate supervised learning (~96% for MNIST) is achieved in a compact network.

11:35 AM - 12:00 PM

15.6 Stochastic Inference and Learning Enabled by Magnetic Tunnel Junctions (Invited), *A. Sengupta, G. Srinivasan, D. Roy and K. Roy, Purdue University*

Neuromorphic computational paradigms that exploit the stochastic switching behavior of devices in the presence of thermal noise is bringing about a wave of change in the way we perceive brain-inspired computing. In this article, we present proposals of spintronics enabled neuromorphic computing systems that perform probabilistic inference and online learning. Such stochastic neuromimetic hardware has the potential of enabling a new generation of state-compressed, low-power computing platforms, which can be significantly more efficient and scalable than their deterministic counterparts.

Session 16: Modeling and Simulation - Advanced Modeling of Ferroelectric Materials and Devices

Tuesday, December 4, 9:00 AM
Plaza A
Co- Chairs: R. Clerc, Institute d'Optique
Y. Chauhan, IIT Kanpur

9:05 AM - 9:30 AM

16.1 In-Memory Computing Primitive for Sensor Data Fusion in 28 nm HKMG FeFET Technology, *K. Ni, B. Grisafe, W. Chakraborty, A. K. Saha**, S. Dutta, M. Jerry, J. A. Smith, S. Gupta**, and S. Datta, University of Notre Dame, *Purdue University*

In this work, we exploit the spatio-temporal switching dynamics of ferroelectric polarization to realize an energy-efficient, and massively-parallel in-memory computational primitive for at-node sensor data fusion and analytics based on an industrial 28nm HKMG FeFET technology [1]. We demonstrate:(i) the spatio-temporal dynamics of polarization switching in HfO2-based ferroelectrics under the stimuli of sub-coercive voltage pulses using experiments and phase-field modeling; (ii) an inherent rectifying conductance accumulation characteristic in FeFET with a large dynamic range of Gmax/Gmin> 100 in the case of 3.0V, 50ns gate pulses; (iii) transition to more abrupt accumulation characteristics due to single/few domain polarization switching in scaled FeFET (34nm LG); and (iv) successful detection of physiological anomalies from real- world multi-modal sensor data streams.

9:30 AM - 9:55 AM

16.2 Experimentally Validated, Predictive Monte Carlo Modeling of Ferroelectric Dynamics and Variability, *C. Alessandri, P. Pandey, and A. C. Seabaugh, University of Notre Dame*

A physics based, predictive, circuit compatible Monte Carlo simulation framework for ferroelectric dynamics is developed. Polarization reversal data is used to extract the statistical distribution of the

ferroelectric grains. With these parameters, the ferroelectric response to any arbitrary waveform, its scaling behavior, and variability are predicted without further calibration.

9:55 AM - 10:20 AM

16.3 Scalability Study on Ferroelectric-HfO2 Tunnel Junction Memory Based on Non-eqilibrium Green Function Method with Self-consistent Potential, *F. Mo, Y. Tagawa, T. Saraya, T. Hiramoto, M. Kobayashi, The University of Tokyo*

We have investigated scalability and design guideline of HfO2-based Ferroelectric Tunnel Junction (FTJ) memory by employing numerical simulation which is based on Non-Equilibrium Green Function (NEGF) method and self-consistent potential, and calibrated by our experimental FTJ data, for the first time. Metal-Ferroelectric-Insulator-semiconductor (MFIS) FTJ shows a higher TER than Metal-Ferroelectric-Insulator-Metal (MFIM) FTJ with almost the same read current because of the large asymmetry of dielectric screening property in top and bottom electrodes. High read current can be obtained by thinner layers while high TER and low depolarizing field area maintained by adjusting bottom semiconductor electrode property. Based on these results, a guideline for designing MFIS structure FTJ to achieve high read current and high TER has been proposed. We have shown a potential for scaling the FTJ down to sub-20 nm diameter.

10:20 AM Coffee Break

10:45 AM - 11:10 AM

16.4 Role of Oxygen Vacancies in Electric Field Cycling Behaviors of Ferroelectric Hafnium Oxide, *C. Liu, F. Liu, Q. Luo**, P. Huang*, X. X. Xu**, H. B. Lv**, Y. D. Zhao, X.Y. Liu and J. F. Kang, Peking University, **Chinese Academy of Sciences, ***University of Hong Kong*

Based on first principle calculations, a new mechanism of the oxygen vacancies(Vo) in the HfO2-based ferroelectric devices is presented. In this mechanism, the Vo in m-phase HfO2 not only serve as the electron traps but also emerge ferroelectricity besides the known o-phase HfO2. And the increased remanent polarization during the “wake-up” process is mainly attributed to this part of Vo-m-phase HfO2 ferroelectric cells. Based on the new mechanism, a Kinetic Monte Carlo (KMC) simulator is developed to quantify the typical electric cycling behaviors observed in the HfO2-based ferroelectric devices, including the wake-up, fatigue, split-up, and breakdown effects. This new understanding establishes relationship between the Vo and the cycling behaviors, and further shows the connection between the dopant and the wake-up characteristics of HfO2-based ferroelectric device.

11:10 AM - 11:35 AM

16.5 First-Principles Perspective on Poling Mechanisms and Ferroelectric/ Antiferroelectric Behavior of Hf1-xZrxO2 for FEFET Applications, *S. Clima, S.R.C. McMitchell, K. Florent*, L. Nyns, M. Popovici, N. Ronchi, L. Di Piazza, J. Van Houdt, G. Pourtois,imec, *University of Leuven, PLASMANT, University of Antwerp*

We investigate at the atomic level the most probable phase transformations under strain, that are responsible for the ferroelectric/ antiferroelectric behavior in Hf1-xZrxO2 materials. Four different crystalline phase transformations exhibit a polar/ non-polar transition: monoclinic-to-orthorhombic requires a gliding strain tensor, orthorhombic-to-orthorhombic transformation does not need strain to polarize the material, whereas tetragonal-to-cubic cell compression and tetragonal-to-orthorhombic cell elongation destabilizes the non-polar tetragonal phase, facilitating the transition towards a polar atomic configuration, therefore changing the polarization-electric field loop from antiferroelectric to ferroelectric. Oxygen vacancies can reduce drastically the polarization reversal barriers.

Session 17: Characterization, Reliability, and Yield - Innovative Characterizations

Tuesday, December 4, 9:00 AM
Plaza B
Co- Chairs: K. Okada, TowerJazz Panasonic Semiconductor
K. P. Cheung, NIST

9:05 AM - 9:30 AM
17.1 Characterization Methodology and Physical Compact Modeling of in-Wafer Global and Local Variability, *K. Pradeep, T. Poiroux**, P. Scheer, A. Juge, G. Gouget, and G. Ghibaudo*, STMicroelectronics, *IMEP-LAHC, MINATEC Campus, **CEA-LETI*

A unified, industrially compatible methodology to characterize and model in-wafer variability at different spatial scales, with addressable array test structures is proposed. Using a physics-based compact model, a single statistical model for both local and global variability is developed for the first time. The proposed method and model are validated using 28 nm FD-SOI devices and the dependence of dominant sources of variability on bias and device geometry is evaluated.

9:30 AM - 9:55 AM
17.2 Too Noisy at the Bottom? -Random Telegraph Noise (RTN) in Advanced Logic Devices and Circuits (Invited), *R. Wang*, S. Guo, Z. Zhang, Q. Wang*, D. Wu*, J. Wang*, R. Huang, Peking University, *Synopsys, Inc.*

In this paper, the recent advances of our studies on RTN are presented from device, circuit, and EDA perspectives. RTN characteristics in FinFETs are investigated and compared with planar devices. The AC RTN effect is discussed for understanding RTN impacts in practical circuit applications. Then, a new and efficient circuit simulation platform for RTN is presented for the first time, which has been implemented in HSPICE using OMI/TMI. In addition, some open questions related to RTN are discussed with outlooks.

9:55 AM - 10:20 AM
17.3 Comprehensive Study on the "Anomalous" Complex RTN in Advanced Multi-Fin Bulk FinFET Technology, *J. Zhang, Z. Zhang, R. Wang, Z. Sun**, Z. Zhang, S. Guo, R. Huang, Peking University, *National Key Laboratory of Science and Technology on Micro/Nano Fabrication, **Fuzhou University*

In this paper, random telegraph noise (RTN) in advanced multi-Fin bulk FinFETs are comprehensively studied for the first time. Based on the statistical experiments, the complete categories of simple and complex RTNs are identified and analyzed in details. Especially, the anomalous ""reversal RTN"" induced by 2 metastable states in single oxide trap, are found not rare, but appears at a certain percentage, which provides a unique opportunity for statistically studying the metastable states directly from RTN measurements. In addition, anomalous layout dependence of RTN amplitudes are observed, with respects to Fin number. The results are helpful for deep understanding of reliability physics and robust circuit design against RTN.

10:20 AM - 10:45 AM
17.4 An Unique Methodology to Estimate The Thermal Time Constant and Dynamic Self Heating Impact for Accurate Reliability Evaluation in Advanced FinFET Technologies, *S. Mukhopadhyay, A. Kundu, Y.W. Lee, H. D. Hsieh, D.S.Huang, J.J.Horng, T.H.Chen, J.H. Lee, Y.S. Tsai, C.K.Lin, R. Lu, and J. He, Taiwan Semiconductor Manufacturing Company Limited*

The increasing impact of self-heating effect (SHE) in complex FinFET structure is a serious reliability concern. Although the evaluation of SHE has become extremely arduous; this work proposes an in-situ layout based experimental solution to find out the precise thermal time constant (TTH) due to SHE on

advanced FinFET devices, even with the application of very pragmatic ‘circuit-like’ gate and drain input waveforms. Using this precise TTH, the accurate dynamic thermal profile is found out from SPICE simulations. Finally, the true degradations due to different reliability mechanisms are evaluated including SHE impact and successfully compared with measured FinFET silicon data.

10:45 AM Coffee Break

11:10 AM - 11:35 AM
17.5 7nm FinFET Plasma Charge Recording Device, *Y.-P. Tsai, J-R Shih*, Y-C King and C. J. Lin, National Tsing Hua University (NTHU), *Taiwan Semiconductor Manufacturing Company*

A new wafer-level coupling plasma charge recorder fabricated with 7nm FinFET CMOS logic process is presented in this paper. This plasma ion charge recording device provides the historic and quantitative plasma ion charges of damascene metallization steps in advanced 7nm FinFET COMS logic processes. The high-resolution plasma ion recorder is formed by an accurate FinFET coupling structure to store the plasma ion level and distribution of the whole wafer. By a simple wafer-level WAT measurement, the promising plasma charge recording device can efficiently collect the accumulated ion charges, ion polarization, and tiny plasma fluctuation of each metallization process step in 7nm FinFET CMOS logic technologies, which definitely provides a superior device and method in developing a reliable and non-latent plasma damage process for 7nm FinFET technology and beyond.

11:35 AM - 12:00 PM
17.6 Development of X-ray Photoelectron Spectroscopy under bias and its application to determine band-energies and dipoles in the HKMG stack, *P. Kumar, C. Leroux*, F. Domengie, E. Martinez*, V. Loup*, D. Guiheux, Y. Morand*, J-M Pedini*, C Tabone*, F. Gaillard*, G. Ghibaudo**, STMicroelectronics, *Univ. Grenoble Alpes, CEA, LETI, **IMEP-LAHC, Minatec/INPG*

In this paper, we present for the first time specific methodology and test structures authorizing an accurate analysis of XPS under bias measurements. Such analysis which identifies effective biasing across the device, allows to determine the absolute energy levels of the different layers in the HKMG stack at any bias. This enables an accurate band diagram identification and it is applied to analyze the physical mechanisms at work in the threshold voltage (VT) engineering of HKMG stacks. We demonstrate that VT shift induced by La and Al additives or metal gate thickness variations originates by the modifications of the dipole at SiO2/high-k interface.

12:00 PM - 12:25 PM
17.7 In-situ investigation of the impact of externally applied vertical stress on III-V bipolar transistor, *Y. Liu, G. Hiblot, M. Gonzalez, K. Vanstreels, D. Velenis, M. Badaroglu**, G. Van der Plas, I. De Wolf, imec, *KU Leuven, **Qualcomm Inc.*

This work presents a new methodology to investigate in-situ the impact of vertical stress on the electrical characteristics of semiconductor devices. It is applied for the first time on III-V Heterojunction Bipolar Transistors (HBT). It combines a nanoindenter, which is used to apply controlled vertical forces on the sample surface, with in-situ electrical measurements using micro probes. The HBT devices are shown to be significantly affected by vertical stress: both the current and the capacitance show a reduction with increasing compressive vertical stress. The observations are confirmed by TCAD simulations. This method can be employed to extract the sensitivity of advanced devices to vertical (out-of-plane stress) which is a growing concern in packaging and 3D integration.

Career Luncheon

Tuesday, December 4, 12:25– 2:15 PM
Grand Ballroom B
Speakers:
John Chen, VP of Technology and Foundry Management, nVidia
Veena Misra, Distinguished Professor, North Carolina State University

In this inaugural IEDM Career Luncheon, the IEDM Executive Committee invites student conference attendees, aspiring professionals, and the IEDM community at-large to join several industry and academic veterans in a casual, buffet lunch setting to discuss topics related to building their careers in the semiconductor industry. To facilitate this dialog, two distinguished members of the semiconductor community, Dr. John Chen and Prof. Veena Misra, will share their industrial and academic perspectives on skill sets needed in the future of the semiconductor industry. We encourage the audience to engage with their peers and industry/academic leaders seated at their dining table, and with the distinguished speakers to seek answers to their career development questions.

Session 18: Circuit and Device Interaction - Embedded Memory at Advanced CMOS Nodes
Tuesday, December 4, 2:15 PM
Grand Ballroom A
Co- Chairs: R. Waser, RWTH Aachen
A. Mocuta, imec

2:20 PM - 2:45 PM
18.1 MRAM as Embedded Non-Volatile Memory Solution for 22FFL FinFET Technology, *O. Golonzka, J.-G. Alzate, U. Arslan, M. Bohr, P. Bai, J. Brockman, B. Buford, C. Connor, N. Das, B. Doyle, T. Ghani, F. Hamzaoglu, P. Heil, P. Hentges, R. Jahan, D. Kencke, B. Lin, M. Lu, M. Mainuddin, M. Meterelliyoz, P. Nguyen, D. Nikonov, K. O'brien, J. ODonnell, K. Oguz, D. Ouellette, J. Park, J. Pellegren, C. Puls, P. Quintero, T. Rahman, A. Romang, M. Sekhar, A. Selarka, M. Seth, A. J. Smith, A. K. Smith, L. Wei, C. Wiegand, Z. Zhang and K. Fischer, Intel Corporation*

This paper presents key features of MRAM-based non-volatile memory embedded into Intel 22FFL technology. 22FFL is a high performance, ultra low power FinFET technology for mobile and RF applications with extensive high voltage and analog support, and a high level of design flexibility at low cost. Embedded NVM technology presented here achieves 200°C 10-year retention capability combined with >1E6 cycle endurance and high die yield. Technology data retention, endurance and yield capabilities are demonstrated on 7.2Mbit arrays. We describe device-level MTJ characteristics, key integration features, cell characteristics, array operation specifics, as well as key yield milestones.

2:45 PM - 3:10 PM
18.2 Demonstration of Highly Manufacturable STT-MRAM Embedded in 28nm Logic, *Y. J. Song, J. H. Lee, S. H. Han, H. C. Shin, K. H. Lee, K. Suh, D. E. Jeong, G. H. Koh, S. C. Oh, J. H. Park, S. O. Park, B. J. Bae, O. I. Kwon, K. H. Hwang, B.Y. Seo, Y.K. Lee, S. H. Hwang, D. S. Lee, Y. Ji , K.C. Park, G. T. Jeong, H. S. Hong, K. P. Lee, H. K. Kang, and E. S. Jung, Samsung Electronics*

We successfully demonstrated the manufacturability of 8Mb STT-MRAM embedded in 28nm FDSOI logic platform by achieving stable functionality and robust package level reliability. Read margin were greatly improved by increasing TMR value and also reducing distribution of cell resistance using advanced MTJ stack and patterning technology. Write margin was also increased by improving the efficiency using novel integration process. Its product reliability was confirmed in package level with passing HTOL 1000 hours tests, 10^6 endurance test, and retention test. For a wider application, we also demonstrated the feasibility of high density 128Mb STT-MRAM. Based on these results, we clearly verified the product manufacturability of embedded STT-MRAM.

3:10 PM - 3:35 PM

18.3 Enablement of STT-MRAM as last level cache for the high performance computing domain at the 5nm node, *S. Sakhare*, M. Perumkunnil, T. Huynh Bao, S. Rao, W. Kim, D. Crotti, F. Yasin, S. Couet, J. Swerts, S. Kundu, D., Yakimets, R. Baert, HR. Oh, A. Spessot, A. Mocuta, G. Sankar Kar, A. Furnemont, imec*

The increased complexity of CMOS transistor processing has led to limited scaling of high density SRAM cell at advanced technology nodes. STT-MRAM appears to be a promising candidate for replacing last level caches (LLC). This paper addresses design technology co-optimization (DTCO) of STT-MRAM technology and analyzes its viability as a LLC (compared to SRAM) for the high performance computing (HPC) domain (while maintaining a constraint of occupying merely 43.3% of SRAM macro area at identical capacities). This is the first study that breaks down a power, performance and area (PPA) comparison between SRAM and STT-MRAM based LLCs at the 5nm node. The STT-MRAM design and analysis is based on a silicon verified compact model and can be realized using 193i single patterning at the 5nm node. Our STT-MRAM design manages to achieve a nominal access latency <2.5ns and <7.1ns for read and write operations respectively. We also observe a clear and significant trend of increasing energy gains with respect to SRAM for increasing LLC sizes with the crossover points for STT-MRAM read and write operations at 0.4MB and 5MB respectively.

3:35 PM Coffee Break

4:00 PM - 4:25 PM

18.4 Truly Innovative 28nm FDSOI Technology for Automotive Micro-Controller Applications embedding 16MB Phase Change Memory, *F. Arnaud, P. Zuliani, M.P. Reynard, A. Gandolfo, F. Diesgni, P. Mattavelli, E. Gomiero, G. Samanni, C. Jahan, R. Berthelon, O. Bewer, E. Richard, V. Barral, A. Villaret, S. Kohler, J.C. Grenier, R. Ranica, C. Gallon, A. Souhaite, D. Ristoiu, L. Favennec, V. Caubet, S. Delmedico, N. Cherault, R. Beneyton, S. Chouteau, P.O. Sassoulas, A. Vernhet, Y. Le Friec, F. Domengie, L. Scotti, D. Pacelli, J. L. Ogier, F. Boucard, S. Lagrasta, D. Benoit, L. Clement, P. Boivin, P. Ferreira, R. Annuniziata, P. Cappelletti, STMicroelectronics*

For the first time we propose a 28nm FDSOI e-NVM solution for automotive micro-controller applications using a Phase Change Memory (PCM) based on chalcogenide ternary material. A complete array organization is described exploiting body biasing capability of Fully Depleted Silicon On Insulator (FDSOI) transistors. Leveraging triple gate oxide integration with high-k metal gate (HKMG) stack, a true 5V transistor with high analog performance has been demonstrated. Reliable PCM 0,036um2 analytical cell with 2 decades programming window after 1 Million of cycles has been demonstrated. Finally, current distributions based on a fully integrated 16MB macro-cell is presented achieving Bit Error Rate (BER) < 10-8 after multiple bakes at 150°C and 10k cycling of code storage memory.

4:25 PM - 4:50 PM

18.5 A cost-efficient 28nm split-gate eFLASH memory featuring a HKMG hybrid bit cell and HV device, *R. Richter, M. Trentzsch, S. Dünkel, J. Müller, P. Moll, B. Bayha, K. Mothes, A. Henke, M. Mazur, J. Paul, P. Krottenthaler, J. Poth, S. Jansen, R. Hüselitz, H. Kim, A. Zaka, T. Herrmann, E.M. Bazizi, S. Beyer, P. Ghazavi*, H. Om'mani*, S. Lemke*, Y. Tkachev*, F. Zhou*, J. Kim*, X. Liu*, V. Tiwari*, and N. Do*, GLOBALFOUNDRIES, *Silicon Storage Technology, Inc.*

We demonstrate for the first time the integration of the proven SuperFlash® bit cell into 28 nm High-K Metal Gate (HKMG) technology, incorporating logic HKMG into the flash cell. Flash cell and high-voltage (HV) devices are implemented into a cost-optimized process flow saving seven masks compared to other 28nm eFLASH technologies. Comparable program/erase (P/E) endurance of up to one million cycles at

125°C is shown and program disturb characteristics meets array operation requirements. The Wordline transistor exhibits no degradation in sub-threshold slope of the post 100k P/E cycling, demonstrating robust reliability despite the introduction of HKMG into the flash cell. Additionally, the HKMG based HV devices demonstrate performance similar to platforms without HKMG material.

4:50 PM - 5:15 PM
18.6 A Bi-stable 1- /2-Transistor SRAM in 14 nm FinFET Technology for High Density / High Performance Embedded Applications, *Y. Widjaja, J. Wilson, T. Nguyen, J-W Han, C. Norwood, D. Maheshwari, S. Lai, P. Vorenkamp, Z. Or-Bach, Y. Nishi*, Zeno Semiconductor Inc., *Stanford University*

1-transistor and 2-transistor (1T/2T) SRAM are fabricated using 14 nm baseline foundry process without any process modifications. A bi-stable self-latch mechanism is established in a single transistor where its p-type body becomes electrically floating by reverse biased, buried depletion regions from adjacent n-wells. The bit cell operation and the disturb immunity are verified. A unit cell size of 0.039 µm2 is achieved, offering >2x area reduction over 6T-SRAM and providing comparable power and performance.

Session 19 (Focus): Power Devices - Challenges for Wide Bandgap Device Adoption in Power Electronics
Tuesday, December 4, 2:15 PM
Continental Ballroom 1-3
Co- Chairs: D.S. Lee, Texas Instruments
G. Meneghesso, University of Padova

2:20 PM - 2:45 PM
19.1 SiC Devices for Mainstream Adoption (Invited), *P. Friedrichs, Infineon Technologies AG*

SiC power devices enter more and more applications today. This process is supported by a couple of factors. Maturity levels and cost/performance of diodes and transistors are interesting enough for many users to consider the new components. Furthermore, devices are more and more fine-tuned to target application requirements which make it easier to enter the most promising target applications. The contribution will sketch on various examples how this philosophy can be rolled out. A new generation of power didoes will be discussed as well as corresponding more powerful package technologies. Finally, a similar assessment for SiC power MOSFETs will be presented.

2:45 PM - 3:10 PM
19.2 The current status and future prospects of SiC high voltage technology (Invited), *A. Mihaila, L. Knoll, E. Bianda, M. Bellini, S. Wirths, G. Alfieri, L. Kranz, F. Canales, and M. Rahimo, ABB Switzerland, Ltd.*

This paper reviews the recent progress of SiC MOSFETs rated above 3.3kV. The static and dynamic performance of 3.3 and 6.5kV-rated MOSFETs will be evaluated and benchmarked against similarly rated state-of-the-art Si IGBTs. A numerical comparison between high voltage (15kV) SiC MOSFETs and IGBTs will also be provided. The paper will also attempt to comment on the future challenges facing high voltage (HV) devices in SiC technology.

3:10 PM - 3:35 PM
19.3 Progress in High and Ultrahigh Voltage Silicon Carbide Device Technology (Invited), *Y. Yonezawa, K. Nakayama, R. Kosugi, S. Harada, K. Koseki, K. Sakamoto, T. Kimoto*, H. Okumura, Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology (AIST), *Kyoto University*

The current developments in silicon carbide (SiC) device technology in various voltage ranges are introduced. These developments correspond to, in particular, next-generation high to ultrahigh-voltage devices, SiC super-junction metal oxide semiconductor field effect transistors, SiC insulated gate bipolar transistors, and the fundamental bipolar degradation suppression technology. We expect that these next generation devices will trigger a paradigm shift in power electronics.

3:35 PM - 4:00 PM

19.4 Effects of Basal Plane Dislocations on SiC Power Device Reliability (Invited), *R. E. Stahlbush, K. N. A. Mahakik, A. J. Lelis* and R. Green*, U.S. Naval Research Laboratory, *U.S. Army Research Laboratory*

As silicon carbide power devices enter the commercial power electronics market there is a strong interest in all aspects of their reliability. This work discusses the degradation of MOSFETs due to basal plane dislocations (BPDs). During the forward bias of the MOSFET body diode, electron-hole recombination causes BPDs to fault and the resulting stacking faults in the drift layer degrade the MOSFET. As the stacking faults grow, the on-state conductivity of the MOSFET drift layer decreases, the off-state leakage of the drift layer increases, and the forward voltage of the body diode increases. Commercial 1200 V MOSFETs were stressed with a body current of 5 A or 10 A. The first generation of commercial MOSFETs showed significant degradation within minutes of stress time, whereas more recent MOSFETs did not show degradation for over 5 hours of stress time.

4:00 PM Coffee Break

4:25 PM - 4:50 PM

19.5 GaN devices for automotive application and their challenges in adoption (Invited), *T. Kachi, Nagoya University*

Currently, electrification of automobiles is an urgent task. Electrification requires high performance power devices to achieve high efficiency. Wide bandgap semiconductors are powerful candidates for power devices used in the near future electric vehicles (EV) and fuel cell vehicles (FCV) . Recent advances in GaN power devices are prominent. Lateral GaN power devices on Si substrates are beginning to be commercialized and are moving on to the system development. Research and development of vertical GaN power devices is also accelerating, and there are reports that exceed the performance of SiC-MOSFETs. Such high-performance devices are expected to greatly contribute to the electrification of automobiles, then interest in GaN power devices is increasing.

4:50 PM - 5:15 PM

19.6 Barriers to the Adoption of Wide-Bandgap Semiconductors for Power Electronics (Invited), *I.C. Kizilyalli, E.P. Carlson*, and D.W. Cunningham, U.S. Department of Energy, *Booz Allen Hamilton*

Wide-bandgap power semiconductor devices offer enormous energy efficiency gains in a wide range of potential applications. As silicon-based semiconductors are fast approaching their performance limits for high power requirements, wide-bandgap semiconductors such as gallium nitride and silicon carbide with their superior electrical properties are likely candidates to replace silicon in the near future. Along with higher blocking voltages wide-bandgap semiconductors offer break-through relative circuit performance enabling low losses, high switching frequencies, and high temperature operation. However, even with the considerable materials advantages, a number of challenges are preventing widespread adoption of power electronics using WBG semiconductors.

5:15 PM - 5:40 PM

19.7 GaN Power Commercialization with Highest Quality-Highest Reliability 650V HEMTs-Requirements, Successes and Challenges (Invited), *P. Parikha, Y. Wua, L. Shena, R. Barra, S. Chowdhurya, J. Grittersa, S. Yea a, P. Smitha, L. McCarthya, R. Birkhahna, M. Moorea, J. McKaya, H. Clementa, U. Mishra, R. Lala, P. Zuka, T. Hosodab, K. Shonob, K. Imanishib, Y. Asaib. Transphorm Inc.*

Gallium Nitride (GaN) is now a popular choice for power conversion. High voltage (HV) GaN HEMTs (GaN FETs) in the range of 650-900 volts are emerging as the next standard for power conversion. This paper highlights key successes in efficient and compact converters/inverters ranging from high performance gaming/crypto-mining power supplies, titanium class server power, servo drives, PV inverters, and automotive OBCs, dc-dc converters, pole charges. The reasons for market success including unmatched quality & reliability, high volume GaN on Si manufacturing, robust performance in applications as well as challenges to achieve the full potential of GaN FETs are presented.

Session 20: Memory Technology - RRAM for Neuromorphic Applications
Tuesday, December 4, 2:15 PM
Continental Ballroom 4
Co- Chairs: B. Magyari-Kope, Stanford University
R. Dittmann, Forschungszentrum Juelich

2:20 PM - 2:45 PM
20.1 20x Retention Improvement by Eliminating Resistance Relaxation with High Temperature Forming in 28 nm RRAM Chip, *X. Xu, L. Tai, T. Gong, J. Yin, P. Huang***, J. Yu, D. Nian Dong, Q. Luo, J. Liu, Z. Yu, X. Zhu, X. Long Wu**, Q. Liu, H. Lv, M. Liu, Chinese Academy of Sciences, Beijing, *University of the Chinese Academy of Sciences, **Anhui University, ***Peking University*

In this work, we proposed a high temperature forming scheme for 28 nm 1Mb RRAM test chip. Compared with room temperature forming scheme, the average forming voltage performed at 125 ℃ could be greatly reduced from 2.5 V to 1.7 V. Resistance relaxation resulted from the recombination of Vo and O2- that generally occurred after programming was effectively eliminated as the residual O2-in the filament was highly decreased. Benefit from this,retention improvement of more than 20× times was successfully achieved, especially for LRS.

2:45 PM - 3:10 PM
20.2 Characterizing Endurance Degradation of Incremental Switching in Analog RRAM for Neuromorphic Systems, *M. Zhao, H. Wu, B. Gao, X. Sun*, Y. Liu, P. Yao, Y. Xi, X. Li, Q. Zhang, K. Wang**, S. Yu*, and H. Qian, Tsinghua University, *Georgia Institute of Technology, **Huawei Technologies Co., LTD.*

Resistive random access memory (RRAM) is attractive for neuromorphic computing systems as synaptic weights. In the neural network training, incremental switching occurs between the analog conductance states, thus the analog RRAM devices have unique endurance degradation behaviors compared to the convention digital memory application. In this work, a fast measurement platform is developed to characterize the endurance of incremental switching in analog RRAM. It is found that under weak weight update pulses, the incremental switching cycles of RRAM can be increased for more than 5 orders of magnitude compared with full window switching under strong programming pulses. The 1e11-cycle endurance of analog RRAM is proved to be sufficient for training neural networks online for various datasets (from MNIST to ImageNet). However, the nonlinearity and dynamic range of analog RRAM degrade during cycling, which may influence the learning accuracy of the neural network when it re-trains with new datasets.

3:10 PM - 3:35 PM

20.3 In-depth Characterization of Resistive Memory-based Ternary Content Addressable Memories, *D. R. B. Ly, B. Giraud, J-P Noel, A. Grossi, N. Castellani, G. Sassine, J-F Nodin, G. Molas, C. Fenouillet-Beranger, G. Indiveri*, E. Nowak and E. Vianello, CEA Leti, *University of Zurich and ETH Zurich*

Resistive Memory-based Ternary Content Addressable Memories (TCAMs) were developed to reduce cell area, search energy and standby power consumption beyond what can be achieved by SRAM-based TCAMs. In previous works, RRAM-based TCAMs have already been fabricated, but the impact of RRAM reliability on TCAM performance has never been proven until now. In this work, we fabricated and extensively tested a RRAM-based TCAM circuit. We show that a trade-off exists between search latency and reliability in terms of match/mismatch detection and search/read endurance. We show that a RRAM-based TCAM is an ideal building block in multi-core neuromorphic architectures. These ones would not be affected by long latency time and limited endurance, and could greatly benefit from their high-density and zero standby power consumption.

3:35 PM - 4:00 PM
20.4 Mixed-Signal Neuromorphic Inference Accelerators: Recent Results and Future Prospects (Invited), *M. Bavandpour, M.R. Mahmoodi, H. Nili, F. Merrikh, Bayat, M. Prezioso, A. Vincent, and D.B. Strukov, K.K. Likharev*, University of California, Santa Barbara, *Stony Brook University*

Recent advances in analog-grade dense nonvolatile memories now enable extremely fast, compact, and energy efficient analog circuits. Such circuits are perfectly suited for implementations of the inference operation in neuromorphic networks. Here, we review implementations mixed-signal circuits, describe recent experimental demos of mixed-signal neuromorphic networks and outline urgently needed work.

4:00 PM Coffee Break

4:25 PM - 4:50 PM
20.5 Temporal sequence learning with a history-sensitive probabilistic learning rule intrinsic to oxygen vacancy-based RRAM, *J. Doevenspeck, R. Degraeve, A. Fantini, P. Debacker, D. Verkest, R. Lauwereins, and W. Dehaene, imec, KU Leuven ESAT*

Widely spread and low value resistance distributions inhibit the use of filamentary resistive RAM (RRAM) at low currents for deep learning training and inference. An entirely different approach which employs RRAM as active computational elements is proposed. For this means, the history-sensitive probabilistic reset in Tantalum-Oxide (TaOx)-based RRAM is characterized and explained. This intrinsic RRAM effect is used as a local learning rule in a novel temporal sequence learning algorithm.

4:50 PM - 5:15 PM
20.6 In-Memory and Error-Immune Differential RRAM Implementation of Binarized Deep Neural Networks, *M. Bocquet, T. Hirztlin*, J.-O. Klein*, E. Nowak**, E. Vianello**, J.-M. Portal and D. Querlioz*, Université de Toulon, CNRS, IM2NP, *Univ Paris-Sud, **CEA, LETI*

We fabricated differential HfO2-based memory arrays and their CMOS circuitry for in-Memory Computing. Our approach reproduces the reliability benefits of error correction, but without the associated CMOS overhead. It can implement ultralow-energy Binarized Deep Neural Networks, and allows using RRAMs at low voltage, where they feature outstanding endurance.

5:15 PM - 5:40 PM

20.7 A new hardware implementation approach of BNNs based on nonlinear 2T2R synaptic cell, *Z. Zhou, P. Huang, Y. C. Xiang, W. S. Shen, Y. D. Zhao, Y. L. Feng, B. Gao*, H. Q. Wu*, H. Qian*, L. F. Liu, X. Zhang, X. Y. Liu, and J. F. Kang, Peking University, *Tsinghua University*

For the first time, we propose a new hardware implementation approach which can utilize the non-linear synaptic cells to build a Binarized-Neural-Networks (BNNs)for online training. A 2T2R-based synaptic cell is designed and demonstrated by the fabricated RRAM array to achieve the basic functions of synapse in BNNs: binary weight (sign(W)) reading and analog weight updating (W+ΔW). The performance of BNNs based on 2T2R synaptic cells is evaluated by MNIST, and the recognition accuracy of 97.4% can be achieved. A novel refresh operation is proposed to enhance the network performance.

Session 21: Process and Manufacturing Technology - Advanced Gate All Around Process
Tuesday, December 4, 2:15 PM
Continental Ballroom 5
Co-Chairs: S. Yang, Qualcomm
C.-W. Liu, Taiwan University

2:20 PM - 2:45 PM
21.1 Ge CMOS gate stack and contact development for Vertically Stacked Lateral Nanowire FETs, *M.J.H. van Dal, G. Vellianitis, G. Doornbos, B. Duriez, M.C. Holland, T. Vasen, A. Afzalian, E. Chen*, S.K. Su*, T.K. Chen*, T.M. Shen*, Z.Q. Wu*, C.H. Diaz*, TSMC Corporate Research, *TSMC*

We present (i) a novel, thermally stable Atomic Layer Deposition (ALD) high-k dielectric stack that, for the first time, has the potential to meet all gate stack requirements for both n- and p-channel Ge FETs, (ii) record low contact resistivity for n Ge/metal contacts using an implant-free contact scheme with successful implementation into a single nanowire (NW) Ge nFET baseline, (iii) single NW Ge pFETs with short-channel effect (SCE) immunity down to 24 nm physical gate length, of which electrical data show excellent agreement with calibrated models and (iv) demonstration of Ge-channel vertically stacked lateral NW FETs using a 300 mm VLSI compatible platform.

2:45 PM - 3:10 PM
21.2 Advantage of NW structure in preservation of SRB-induced strain and investigation of off-state leakage in strained stacked Ge NW pFET, *H. Arimura, G. Eneman, E. Capogreco, L. Witters, A. De Keersgieter, P. Favia, C. Porret, A. Hikavyy, R. Loo, H. Bender, L.-Å. Ragnarsson, J. Mitard, N. Collaert, D. Mocuta, N. Horiguchi, imec*

Nanowires (NW) and nanosheets (NS) are promising device architectures for future technology nodes as they can offer better electrostatics than FinFETs. In this paper, we show another advantage of strained Ge NW pFET over strained Ge FinFET, which lies in the preservation of Strain-Relaxed-Buffer (SRB)-induced strain through fin cut and S/D recess. This benefit comes from the presence of the sacrificial SiGe layers. Lowering the Ge concentration in the SiGe sacrificial layer is a way to further suppress the strain loss. Furthermore, a comparison of Ge NW pFETs integrated on Ge SRB and SiGe SRB reveals that SiGe SRB provides a huge advantage not only in the strain engineering but also in IOFF control. These are key enablers in maximizing the performance while minimizing the IOFF of strained Ge NW pFETs.

3:10 PM - 3:35 PM
21.3 Tunability of Parasitic Channel in Gate-All-Around Stacked Nanosheets, *S. Barraud, B. Previtali, V. Lapras, C. Vizioz, J.-M. Hartmann, S. Martinie, J. Lacord, M. Cassé, L. Dourthe, V. Loup, G. Romano*, N. Rambal, Z. Chalupa, N. Bernier, G. Audoit, A. Jannaud**, V. Delaye, V. Balan, O. Rozeau, T. Ernst, M. Vinet, CEA-LETI, and Univ. Grenoble Alpes, * STMicroelectronics, **SERMA Technologies*

For the first time, a comprehensive study going from the integration of 3D stacked nanosheets Gate-All-Around (GAA) MOSFET devices to SPICE modeling is proposed. Devices have been successfully fabricated on SOI substrates using a replacement high- metal gate process and self-aligned-contacts. Back-biasing is herein efficiently used to highlight a drastic improvement of electrostatics in the upper GAA Si channels. Advanced electrical characterization of these devices enabled us to calibrate a new version of physical compact model (LETI-NSP) in order to assess the performance of ring oscillators for different configurations of GAA FETs integrating up to 8 vertically stacked Si channels.

3:35 PM Coffee Break

4:00 PM - 4:25 PM

21.4 Voltage Transfer Characteristic Matching by Different Nanosheet Layer Numbers of Vertically Stacked Junctionless CMOS Inverter for SoP/3D-ICs applications, *P.-J. Sung, C.-Y. Chang*, L.-Y. Chen**, K.-H. Kao**, C.-J. Su, T.-H. Liao***, C.-C. Fang***, C.-J. Wang, T.-C. Hong*, C.-Y. Jao***, H.-S. Hsu***, S.-X. Luo**, Y.-S. Wang**, H.-F. Huang**, J.-H. Li**, Y.-C. Huang*, F.-K. Hsueh, C.-T. Wu, Y.-M. Huang, F.-J. Hou, G.-L. Luo, Y.-C. Huang, Y.-L. Shen, W. C.-Y. Ma***, K.-P. Huang+, K.-L. Lin, S. Samukawa++, Y. Li*, G.-W Huang, Y.-J. Lee,*, J. -Y. Li, W.-F. Wu, J.-M. Shieh, T.-S. Chao*, W. -K. Yeh, Y.-H. Wang**,* National Nano Device Laboratories, **National Chiao Tung University, **National Cheng Kung University, ***National Sun Yat-sen University, +Industrial Technology Research Institute, ++Tohoku University*

For the first time, CMOS inverters with different numbers of vertically stacked junctionless (JL) nanosheets (NSs) are demonstrated. All fabrication steps were below 600 °C, and 8-nm thick poly-Si NSs with smooth surface roughness were formed by a dry etching process. Compared to single channel devices, stacked n/p-channel FETs exhibit higher on-current with low leakage current. Furthermore, a common-gate process was performed for the fabrication of CMOS inverters. By adjusting the NS layer numbers for n/pFETs, respectively, the voltage transfer characteristics (VTCs) of the CMOS inverter can be matched much better to reduce the noise margin due to on-current matching without area penalty. This work experimentally demonstrates a new configuration of CMOS inverters on stacked NSs, which is promising for System-on-Panel (SoP) and 3D-ICs applications.

4:25 PM - 4:50 PM

21.5 Vertically Stacked Gate-All-Around Si Nanowire CMOS Transistors with Reduced Vertical Nanowires Separation, New Work Function Metal Gate Solutions, and DC/AC Performance Optimization, *R. Ritzenthaler, H. Mertens, V. Pena*, G. Santoro*, A. Chasin, K. Kenis, K. Devriendt, G. Mannaert, H. Dekkers, A. Dangol, Y. Lin*, S. Sun*, Z.Chen**, M. Kim*, J. Machillot*, J. Mitard, N. Yoshida*, N. Kim*, D. Mocuta, N. Horiguchi, imec, *Applied Materials*

We report on vertically stacked gate-all-around (GAA) Si nanowire (NW) MOSFETs, integrated in a CMOS dual Work Function Metal Replacement Metal Gate (RMG) flow. The integration of a lower temperature STI module and a SiN liner, designed to mitigate the oxidation-induced NW size loss and improve the width/height aspect ratio and NW controllability, is validated electrically. Additionally, Si GAA devices with reduced vertical nanowire spacing are demonstrated. The challenges in terms of Work Function Metal thickness scaling are highlighted, and a thinner nMetal process with low VTH capability and no JG/PBTI lifetime penalty is proposed. Electrically, these process innovations lead to a large improvement of ION/IOFF performance and short channel margin. Finally, a ring oscillator circuit demonstration is shown, with a improvement of gate delay from 24ps down to 10ps at matched VDD demonstrated.

Session 22: Nano Device Technology - 2D CMOS and Memory Devices

Tuesday, December 4, 2:15 PM

Continental Ballroom 6
Co-Chairs: M. Shrivastava, Indian Institute of Science
W.-C. Chien, Macronix

2:20 PM - 2:45 PM
22.1 2D materials: roadmap to CMOS integration (Invited), *C. Huyghebaert, T.Schram, Q. Smets, T. Kumar Agarwal, D.Verreck, S.Brems, A.Phommahaxay, D.Chiappe*, S. El Kazzi, C.Lockhart de la Rosa, G. Arutchelvan ,D. Cott, J. Ludwig, A. Gaur, S. Sutar, A. Leonhardt, D. Marinov, D. Lin, M. Caymax, I. Asselberghs, G. Pourtois and I.P. Radu, imec, *currently @ ASM Europe*

To keep Moore's law alive, 2D materials are considered as a replacement for Si in advanced nodes due to their atomic thickness, which offers superior performance at nm dimensions. In addition, 2D materials are natural candidates for monolithic integration which opens the door for density scaling along the 3rd dimension at reasonable cost. This paper highlights the obstacles and paths to a scaled 2D CMOS solution. The baseline requirements to challenge the advanced Si nodes are defined both with a physical compact model and TCAD analysis, which allows us to identify the most promising 2D material and device design. For different key challenges, possible integrated solutions are benchmarked and discussed. Finally we report on the learning from our first lab to fab vehicle designed to bridge the lab and IMEC's 300mm pilot line.

2:45 PM - 3:10 PM
22.2 First Demonstration of WSe_2 Based CMOS-SRAM, *C.-S. Pang, N. Thakuria1, S. K. Gupta, and Z. Chen, Purdue University*

In this work, we demonstrate a CMOS static random-access-memory (SRAM) using WSe2 as a channel material for the first time, providing comprehensive DC analyses for transition metal dichalcogenide (TMD) material-based memory applications. A tri-gate design is adopted for the n-type MOSFET, while an air-stable, oxygen plasma induced doping scheme is introduced to implement the p-type MOSFET. DC measurements of SRAM cells demonstrate a unique dynamic tunability enabled by modulating the n-FET doping level through electrostatically gating the extended source/drain regions. Furthermore, with various read/write assist techniques, SRAM operation at low VDD of 0.8V is achieved. Our low power demonstration and its 2D ultra-thin material nature suggest promising applications of WSe2 for flexible electronics and Internet of Things (IoT).

3:10 PM - 3:35 PM
22.3 Steep Slope p-type 2D WSe_2 Field-Effect Transistors with Van Der Waals Contact and Negative Capacitance, *J. Wang, X. Guo, Z. Yu*, Z. Ma**, Y. Liu, M. Chan**, Y. Zhu, X. Wang* and Y. Chai, Hong Kong Polytechnic University, *Nanjing University, **The Hong Kong University of Science and Technology*

We fabricated Steep-slope p-type 2d WSe2 NCFET using van der Waals Pt contact and HZO/Al2O3 dielectric. The van der Waals contact is free from disorder and Fermi level pinning and decreases the sub-threshold slope. The NCFET shows minimum SS of 18.2 mV/dec and negligible hysteresis in the sub-threshold region.

3:35 PM Coffee Break

4:00 PM - 4:25 PM
22.4 Toward High-mobility and Low-power 2D MoS_2 Field-effect Transistors (Invited), *Z. Yu, Y. Zhu, W. Li, Y. Shi, G. Zhang*, Y. Chai and X. Wang, Nanjing University, *The Hong Kong Polytechnic University*

2D semiconductors are promising candidates for future electronic device applications due to their immunity to short-channel effects (SCE), but many issues regarding mobility, contact, interface and power consumption still remain (Fig. 1). We develop a low-field model to calculate the mobility of monolayer MoS2 FETs. Guided by the model, high carrier mobility of 150 cm2/Vs and saturation current over 450 µm are realized in long-channel monolayer MoS2 FETs, through a series of interface optimization by high-***k*** dielectric and thiol chemical treatment. For low-power applications, we demonstrate hysteresis-free MoS2 negative capacitance FETs (NCFETs) using ferroelectric HfZrOx(HZO) as gate dielectric, achieving sub-60mV/dec subthreshold slope (SS) over 6 orders of ID, minimum SS of 24 mV/dec and 10^7 on/off ratio under Vdd=0.5V. We further study the high frequency performance and show that sub-60mV/dec is maintained at least to 10 kHz without signs of degradation. Finally, by performing different gate sweeps we conclude that the steep slope is indeed due to NC effects rather than ferroelectric switching of HZO.

4:25 PM - 4:50 PM

22.5 3D Monolithic Stacked 1T1R cells using Monolayer MoS_2 FET and hBN RRAM Fabricated at Low (150°C) Temperature, *C.-H. Wang, C. McClellan, Y. Shi*, Xin Zheng, V. Chen, M. Lanza*, E. Pop and H. -S. P. Wong, Stanford University, * Soochow University*

We demonstrate 3D monolithic integrated two-level stacked 1-transistor/1-resistor (1T1R) memory cells with processing temperature < 150 ºC. CVD monolayer MoS2 transistors are employed to switch few layer CVD hBN RRAMs with programming voltage < 1 V. The 1T1R cell resistance change linearity can be improved by controlling the gate voltage.

4:50 PM - 5:15 PM

22.6 Atomristors: Memory Effect in Atomically-thin Sheets and Record RF Switches, *R. Ge, X. Wu, M. Kim, P.-A. Chen, J. Shi**, J. Choi, X. Li, Y. Zhang**, M.-H. Chiang*, J. C. Lee and D. Akinwande, University of Texas at Austin, *National Cheng Kung University, **Peking University*

Non-volatile resistive switching (NVRS) has been recently observed with synthesized monolayer molybdenum disulfide (MoS2) as the active layer and termed atomristors [1]. In this paper, we demonstrate the fastest switching speed (<15 ns) among all crystalline two-dimensional (2D) related NVRS devices to the best of our knowledge. For the first time, ab-initio simulation results of atomristors elucidate the mechanism revealing favorable substitution of specific metal ions into sulfur vacancies during switching. This insight combined with area-scaling experimental studies indicate a local conductive-bridge-like nature. The proposed mechanism is further supported by sulfur annealing recovery phenomenon. Moreover, exfoliated MoS2 monolayer is demonstrated to have memory effect for the first time, expanding the materials beyond synthesized films. State-of-the-art non-volatile RF switches based on MoS2 atomristors were prepared, featuring 0.25 dB insertion loss, 29 dB isolation (both at 67 GHz), and 70 THz cutoff frequency, a record performance compared to emerging RF switches. Our pioneering work suggests that memory effect maybe present in dozens or 100s of 2D monolayers similar to MoS2 paving the path for new scientific studies for understanding the rich physics, and engineering research towards diverse device applications.

5:15 PM - 5:40 PM

22.7 An Ultra-fast Multi-level $MoTe_2$-based RRAM, *F. Zhang, H. Zhang*, P.R. Shrestha*, Y. Zhu, K. Maize, S. Krylyuk*, A. Shakouri, J.P. Campbell**, K.P. Cheung**, L.A. Bendersky**, A.V. Davydov** and J. Appenzeller, Purdue University, *Theiss Research, Inc., **National Institute of Standards and Technology*

We report multi-level MoTe2-based resistive random-access memory (RRAM) devices with switching speeds of less than 5 ns due to an electric-field induced 2H to 2Hd phase transition. Different from

conventional RRAM devices based on ionic migration, the MoTe2-based RRAMs offer intrinsically better reliability and control. In comparison to phase change memory (PCM)-based devices that operate based on a change between an amorphous and a crystalline structure, our MoTe2-based RRAM devices allow faster switching due to a transition between two crystalline states. Moreover, utilization of atomically thin 2D materials allows for aggressive scaling and high-performance flexible electronics applications. Multi-level stable states and synaptic devices were realized in this work, and operation of the devices in their low-resistive, high-resistive and intrinsic states was quantitatively described by a novel model.

Session 23: Optoelectronics, Displays, and Imagers - Silicon Photonics
Tuesday, December 4, 2:15 PM
Continental Ballroom 7-9
Co-Chairs: C. Doerr, Acacia Communications, Inc.
P. De Dobbelaere, Luxtera

2:20 PM - 2:45 PM
23.1 First cryogenic electro-optic switch on silicon with high bandwidth and low power tunability, *F. Eltes, J. Barreto*, D. Caimi, S. Karg, A. A. Gentile*, A. Hart*, P. Stark, N. Meier, M. G. Thompson*, J. Fompeyrine, S. Abel, IBM Research, * University of Bristol*

We demonstrate the first electro-optic switch operating at cryogenic temperatures of 4 K with a high electro-optic bandwidth of >18 GHz. Our novel technology exploits the Pockels effect in barium titanate thin films co-integrated with silicon photonics and offers low losses, pure phase modulation, and sub-pW electro-optic tuning.

2:45 PM - 3:10 PM
23.2 High Speed (*f3-dB* above 10 GHz) Photo Detection at Two-micron-wavelength Realized by GeSn/Ge Multiple-quantum-well Photodiode on a 300 mm Si Substrate, *S. Xu, W. Wang, Y.-C. Huang*, Y. Dong, S. Masudy-Panah, H. Wang**, X. Gong, and Y.-C. Yeo, National University of Singapore, *Applied Materials Inc., **Nanyang Technological University*

High speed photo detection at two-micron-wavelength has been achieved with a GeSn/Ge multiple-quantum-well (MQW) photodiode (PD), demonstrating a 3-dB bandwidth (f3-dB) above 10 GHz for the first time. The device layer stack was grown on a standard 300 mm (001) Si substrate using RPCVD, showing potential for large-scale integration. Radio frequency (RF) characterization was performed using µm RF optical measurement setup. To our knowledge, this is also the first PDs on Si with direct RF measurement to quantitatively confirm the high speed functionality at 2 µm.

3:10 PM - 3:35 PM
23.3 Quadratic electro-optical silicon-organic hybrid RF modulator in a photonic integrated circuit technology, *P. Steglich, C. Mai, A. Peczek, F. Korndörfer, C. Villringer*, B. Dietzel*, and A. Mai, IHP, *Technical University of Applied Sciences Wildau*

For the first time, an integrated electro-optical RF modulator based on the quadratic electro-optical effect with CMOS compatible sub-volt driver voltages is presented. As unique feature, this modulator provides an amplitude tuning of the modulated carrier wave. The silicon-based modulator was fabricated using process steps of an established photonic integrated circuit technology and covered by a nonlinear optical polymer in a post-process. We demonstrate a device tunability of up to 350 pm/V, surpassing state-of-the-art silicon modulators with an order of magnitude. Moreover, the ring resonator is designed to have an ultra-low per-bit energy consumption of 87 aJ/bit demonstrating the potential for high-performance photonic devices with low energy consumption.

3:35 PM Coffee Break

4:00 PM - 4:25 PM
23.4 Silicon Photonics: a Scaling Technology for Communications and Interconnects (Invited), *P. Dong, K. W. Kim, A. Melikyan, and Y. Baeyens, Nokia Bell Labs*

Silicon photonics exploits CMOS foundry processes to fabricate passive and active photonic circuits on silicon substrates. This technology offers superior scalability in terms of integration level and energy efficiency, two key metrics to obtain sustainable capacity growths in future telecom, datacom, and chip-scale interconnects. We illustrate the advantages of compactness and low power consumption by describing two novel silicon photonic based devices, namely, microring resonators and directly reflectivity modulated lasers.

4:25 PM - 4:50 PM
23.5 InAs/GaAs Quantum Dot Lasers Monolithically Integrated on Group IV Platform (Invited), *K. Li, M. Tang, M. Liao, J. Wu, S. Chen, A. Seeds, and H. Liu, University College London*

III-V quantum dot lasers monolithically integrated on silicon platform attracts intensive interests due to its advantages on providing a promising solution for reliable and efficient light source to integrated on photonics and electronics circuits. Compared to wafer bonding technique, monolithic integration its more attractive for large scale, low cost and streamline fabrication. In this paper, we give a brief review on our recent progress of III-V quantum dot lasers monolithically integrated on 4° offcut and exact (001) Si substrates for the silicon photonic integration.

4:50 PM - 5:15 PM
23.6 Heterogeneously integrated light sources on bulk-silicon platform, *D. Shin, J. Cha, Y. Shin, K. Ha, C. B. Lee, C. Shin, D. Shim, B. L. Choi, H. Hong, K. Lee, and H.-K. Kang, Samsung Electronics,*

Heterogeneously integrated single-wavelength and wavelength-tunable light sources on bulk-silicon platform are presented. Thanks to the thermal advantage of the bulk-silicon platform, the single-wavelength source showed WPE of 8% up to 70°C, feasibility of 25Gb/s direct modulation, and 70°C MTTF of ~46000h. The wavelength-tunable source showed 42.2nm tuning range. This result completes the optical device library suite for the bulk-silicon platform used in most semiconductor products.

Session 24: Modeling and Simulation - 2D Materials, Modeling, and the Optimization of Beta-Ga2O3 Power Devices
Tuesday, December 4, 2:15 PM
Plaza A
Co-Chairs: R. Williams, IBM
M. Pala, University of Paris-Saclay

2:20 PM - 2:45 PM
24.1 Interfacial Thermal Conductivity of 2D Layered Materials: An Atomistic Approach, *K. Parto, A. Pal, X. Xie, W. Cao and K. Banerjee, University of California, Santa Barbara*

This paper presents the first comprehensive modeling and analysis of thermal transport across both lateral and vertical interfaces to two-dimensional (2D) layered materials. Using an ab-initio atomistic Green's function approach that accurately accounts for the interface geometry including the van der Waals gap, as well as interatomic force constants and interface phonon scatterings, we provide estimation of crucial interfacial thermal properties including thermal conductivity that are invaluable for assessing the

performance, scaling, and reliability limits of all emerging 2D based nano-devices, interconnects, circuits and non-planar (monolithic 3D) integration schemes.

2:45 PM - 3:10 PM
24.2 Computational Design of Silicon Contacts on 2D Transition-Metal Dichalcogenides: The Roles of Crystalline Orientation, Doping Level, Passivation and Interfacial Layer, *X. Ma, Z. Fan*, J. Wu, X. Jiang*, J. Chen, University, Qingdao, *Chinese Academy of Sciences*

Systematic numerical simulations based on density functional theory (DFT) and non-equilibrium Green's function (NEGF) formalism have been carried out for comprehensive understanding of the physical properties of silicon contacts on monolayer transition metal dichalcogenides (TMDs). The effects of different contact crystalline orientations including Si (001), (110) and (111), silicon doping levels, possible surface passivation such as H- and F-, as well as interfacial layer (IL) engineering using BN and Graphene are thoroughly discussed. On the one hand, it was found that the contact properties of different crystalline orientations follow similar trend, and the doping modulation of the Schottky barrier height (SBH) remains inappreciable in a practical range of doping level. On the other hand, H- and F- passivation are found to be effective ways to diverge the intrinsic contact into n- and p- type contacts, respectively. In addition, monolayer BN as IL was found to form surprisingly good p-type contact with vanishing p-SBH.

3:10 PM - 3:35 PM
24.3 First Principles Study of Memory Selectors using Heterojunctions of 2D Layered Materials, *L. Li, B. Magyari-Köpe*, C.-H. Wang*, S. Deshmukh*, Z. Jiang*, H. Li*, Y. Yang, H. Li, H. Tian, E. Pop*, T.-L. Ren, H.-S. Philip Wong*, Tsinghua University, *Stanford University*

Two-dimensional (2D) tunnel heterojunctions with an H-shaped energy barrier could serve as ultrathin memory selectors with good symmetry, non-linearity, and high endurance. Atomically thin 2D layered materials can potentially deliver high on-state tunneling current density. We explore the design space for H-shaped memory selectors using heterojunctions of 2D layered materials, using physical modeling and first principles density functional theory (DFT) quantum transport simulations. The difference between simulations and the few existing experiments is also discussed. A selector must be designed to suit the resistive memory (1R) characteristics. We evaluate the H-shaped selector in the one-selector-one-resistor (1S1R) configuration and provide design guidelines for the heterojunction (metal/nL hBN/nL 2D material/nL hBN/metal) design to match with the 1R characteristics.

3:35 PM Coffee Break

4:00 PM - 4:25 PM
24.4 Can Kinetic Inductance in Low-Dimensional Materials Enable a New Generation of RF-Electronics?, *K. Agashiwala, A. Pal, W. Cao, J. Jiang and K. Banerjee, University of California, Santa Barbara*

Kinetic Inductance has been recently exploited at room temperature to create materials with inductance densities that exceed the traditional Faraday limit. In this work, for the first time, we develop a rigorous theoretical framework to uncover the physics and origin of kinetic inductance to identify/engineer the materials for addressing inductance-density and performance requirements in next generation passive devices for RF-ICs. Employing three different approaches (Drude model, Fermi sphere and the Boltzmann Transport Equation), we provide guidelines for optimally exploiting kinetic inductance in natural as well as engineered low-dimensional materials to simultaneously achieve maximum inductance-density and performance required for next-generation RF/wireless applications.

4:25 PM - 4:50 PM

24.5 A Surface Potential- and Physics- Based Compact Model for 2D Polycrystalline-MoS_2 FET with Resistive Switching Behavior in Neuromorphic Computing, *L. Wang, L. Wang, K.-W. Ang, A. Voon-Yew Thean, G. Liang, National University of Singapore*

For the first time, a surface potential- and physics-based compact model for two dimensional (2D) polycrystalline- molybdenum disulfide (MoS2) field effect transistors (FETs) with resistive switching (RS) behavior is developed and verified by experimental data. This model is incorporated with the theories of thermal activation transport, grain boundary (GB) barrier and space charge limited current (SCLC). Based on the GB induced disorders, the grain size, low temperature, and high electrical field dependent characteristics are studied. The predicted transfer and output characteristics have an excellent quantitative agreement with experimental results. Furthermore, considering the hopping process induced defect- (i.e., sulfur vacancy) redistribution, the GB (e.g., intersecting or bisecting GB) dependent resistive switching behavior is physically investigated. Finally, this model is implemented to simulate the synaptic activity such as short-term/long-term plasticity, which indicates the possibility of using 2D-FETs for neuromorphic computing applications.

4:50 PM - 5:15 PM

24.6 Design and Optimization of β-Ga2O3 on (h-BN layered) Sapphire for High Efficiency Power Transistors: A Device-Circuit-Package Perspective, *B. K. Mahajan, Y.-P. Chen, W. Ahn, N. Zagni and M. Ashraful Alam, Purdue University*

Despite exceeding the Baliga's Figure of Merit (BFOM) by 400% and Huang's Chip Area Manufacturing FOM (HCAFOM) by 330% [1], the performance of existing ß-Ga2O3 FETs is inferior to that of GaN, primarily due to extreme self-heating. Self-heating effect (SHE) has emerged as an important concern for device performance, output power density, run-time variability and reliability for modern logic transistors. The effects are even more severe for high-power transistor where the channel material may be a poor thermal conductor, e.g. ß-Ga2O3. Very high internal electric fields, extreme temperature and mechanical stresses associated with these transistors drive electrochemical reactions [2], influence atomic processes [3], and accelerate multiple non-equilibrium effects [4]. A device-circuit-package, multi-physics, multi-scale simulation is needed to capture these effects self-consistently, but such a model has not yet been developed. In this paper, we (i) develop the first self-consistent device (TCAD), circuit (HSPICE), and package (COMSOL) model considering SHE which predicts FET performance on variety of substrates accurately; (ii) use the model to propose a novel hexagonal-Boron Nitride (h-BN) based ß-Ga2O3 FET with 30% (cf. Sapphire substrate) and 80% (cf. SiO2 substrate) reduction in thermal resistance (R_th); (iii) demonstrate the performance of boost converter (with parameters extracted from our TCAD model) with h-BN based ß-Ga2O3 FET, which outperforms the existing ß-Ga2O3 FETs, achieving an efficiency within 10-15% of highest performing enhancement mode (E-mode) GaN FET; (iv) propose h-BN based FinFET which exceeds the ION of the existing ß-Ga2O3 FET by more than 500%; and (v) develop a Faraday-cage type novel packaging strategy for effective heat dissipation and efficient system performance in β-Ga2O3 FETs.

Session 25: Characterization, Reliability, and Yield - Emerging Memory Reliability

Tuesday, December 4, 2:15 PM

Plaza B

Co-Chairs: D. Varghese, Texas Instruments

H. Park, SK Hynix

2:20 PM - 2:45 PM

25.1 Deconvoluting charge trapping and nucleation interplay in FeFETs: Kinetics and Reliability, *M. Pesic, A. Padovani, S. Slesazeck, T. Mikolajick*, and L. Larcher**, MDLSoft Inc, *TU Dresden, **University of Modena and Reggio Emilia*

Discovery of ferroelectric (FE) behavior in HfO2 removed the compatibility roadblocks between the state-of-the-art CMOS and FE memories. Even though FE FETs (FeFETs) are scaled into 22 nm nodes and beyond, the limits of the technology as well as the physical mechanisms and reliability are still under research. In this paper we successfully developed a multiscale modeling platform to understand the interplay between the FE switching and charge trapping. Starting from the nucleation theory and rigorous charge transport modeling we present for the first time a self-consistent modeling framework we used for investigation of reliability and variability in FeFETs.

2:45 PM - 3:10 PM
25.2 Impact of self-heating on reliability predictions in STT-MRAM, *S. Van Beek*, B. J. O'Sullivan, P. J. Roussel, R. Degraeve, E. Bury, J. Swerts, S. Couet, L. Souriau, S. Kundu, S. Rao, W. Kim, F. Yasin, D. Crotti, D. Linten and G. Kar, imec, *also at KU Leuven*

At breakdown conditions, large current flows in STT-MRAM devices. We experimentally show that this large current causes significant self-heating of 200-300°C, which impacts the reliability extrapolation to operating conditions. By measuring and analyzing breakdown at various temperatures and on different MgO thickness, we successfully incorporate self-heating into the breakdown model. We find that the 10 year lifetime is underestimated by a factor 10^3 at 63-percentile, to even 10^7 when applying percentile scaling to 1 ppm.

3:10 PM - 3:35 PM
25.3 Investigating the Statistical-Physical Nature of MgO Dielectric Breakdown in STT-MRAM at Different Operating Conditions, *J.H. Lim, N. Raghavan, A. Padovani**, J.H. Kwon*, K. Yamane*, H. Yang*, V.B. Naik*, L. Larcher***, K.H. Lee* and K.L. Pey, Singapore University of Technology and Design (SUTD), *GLOBALFOUNDRIES Singapore Pte. Ltd., **MDLSoft Inc., ***Università di Modena e Reggio Emilia*

We carry out a comprehensive study on dielectric breakdown in ultra-thin MgO for STT-MRAM application. Pulse voltage, polarity dependence and temperature have been used to study the breakdown distribution in MgO, which follows defect clustering model. Field-induced mechanical strain at the MgO interface during pulsed stress affects TDDB lifetime significantly.

3:35 PM - 4:00 PM
25.4 Trap Reduction and Performances Improvements Study after High Pressure Anneal Process on Single Crystal Channel 3D NAND Devices, *A. Subirats, A. Arreghini, R. Delhougne, E. Rosseel, A. Hikavyy, L. Breuil, S. Vadakupudhu Palayam, G. Van den bosch, D. Linten and A. Furnémont, imec*

We study the impact of HPAP on SCC 3D NAND devices. We show that the process can reduce trap density but is leaving trap impact on devices VT unaffected. It is also shown, both by simulations and measurements, that further scaling could lead to the increase of single trap impact. Finally, we measure that despite largely improving devices electrical parameter, HPAP has no effect on memory performances (Program/Erase) or could slightly degrade it (Retention).

4:00 PM Coffee Break

IEDM Panel
Tuesday, December 4
Continental 1-5
Moderator: Sanjay Natarajan, Applied Materials

Title: The Next 25 years in Electronics

Description: 25 years ago, few of us could have thought that advances in chip technology will allow us to have a tiny device in our pocket that connects us to everyone, provides us with instant access to the world's information, translate foreign languages instantly for us, and tracks our health. Our panelists will debate, discuss, and predict how semiconductor technology will evolve and what new life-changing technologies it will enable in 25 years from today (circa 2045). Given the ambitious scope of this topic, we have assembled an esteemed group of panelists who have had a front-row seat for most of the past 25 years and are in a position to look out over the next 25 years. The group includes industry CEO's and CTO's, long-tenured professors, and government participants from the early days of DARPA for this 25-year look back and 25-year look forward.

Session 27: Memory Technology - MRAM & PCRAM
Wednesday, December 5, 9:00 AM
Grand Ballroom A
Co-Chairs: S. Kang, Qualcomm Technology Inc.
G. Navarro, CEA-Leti

9:05 AM - 9:30 AM
27.1 22-nm FD-SOI Embedded MRAM Technology for Low-Power Automotive-Grade-1 MCU Applications, *K. Lee, R. Chao, K. Yamane, V. B. Naik, H. Yang, J. Kwon, N. L. Chung, S. H. Jang, B. Behin-Aein, J. H. Lim, S. K, B. Liu, E. H. Toh, K. W. Gan, D. Zeng, N. Thiyagarajah, L. C. Goh, T. Ling, J. W. Ting, J. Hwang, L. Zhang, R. Low, R. Krishnan, L. Zhang, S. L Tan, Y. S. You, C. S. Seet, H. Cong, J. Wong, S. T. Woo, E. Quek, S. Y. Siah, GLOBALFOUNDRIES*

We demonstrate 22-nm FD-SOI 40Mb embedded MRAM (eMRAM) macros for automotive-grade-1 (Auto-G1) MCU applications, highlighting sub-ppm t0 bit error rate and zero failure after 1M endurance cycles across Auto-G1 operating temperature range (-40~150 °C). Read disturbance characterization with external field also reveals that 40Mb eMRAM macro is capable of active-mode magnetic immunity > 500 Oe at 150 °C. In addition, based on 22-nm eMRAM macro data, we review the effects of magnetic tunnel junction (MTJ) size on reliability and examine scalability of eMRAM technology beyond 22 nm.

9:30 AM - 9:55 AM
27.2 14ns write speed 128Mb density Embedded STT-MRAM with endurance>10^{10} and 10yrs retention @85°C using novel low damage MTJ integration process, *H. Sato, H. Honjo, T. Watanabe, M. Niwa, H. Koike, S. Miura, T. Saito, H. Inoue, T. Nasuno, T. Tanigawa, Y. Noguchi, T. Yoshiduka, M. Yasuhira, S. Ikeda, S.- Y. Kang*, T. Kubo*, K. Yamashita*, Y. Yagi*, R. Tamura**, and T. Endoh, Tohoku University, *Tokyo Electron Ltd., **Advantest Corp.*

By developed novel damage-control-integration-process technology with new low-damage unit PVD/RIE/SiN-cap process, TMR, thermal stability, and switching efficiency improved by a factor of 1.7, 9, and 9, respectively, and its endurance is over 10^10, although thermal stability drastically increased. Finally, 14ns-write speed at 1.2V-Vdd was successfully demonstrated using our 128Mb-density-STT-MRAM.

9:55 AM - 10:20 AM
27.3 STT-MRAM devices with low damping and moment optimized for LLC applications at 0x nodes, *L. Thomas, G. Jan, S. Serrano-Guisan, H. Liu, J. Zhu, Y.-J. Lee, S. Le, J. Iwata-Harms, R.-Y. Tong, S. Patel, V. Sundar, D. Shen, Y. Yang, R. He, J. Haq, Z. Teng, V. Lam, P. Liu, Y.-J. Wang, T. Zhong, H. Fukuzawa, and P.K. Wang, TDK- Headway Technologies, Inc.*

Last-Level-Cache applications at 0X technology nodes require devices switching reliably in less than 10ns at currents smaller than 50uA, while preserving data retention up to 85°C. In this paper, we show that both low Gilbert damping and low magnetic moment are the primary factors for efficient writing at nanosecond time scales. We report comprehensive device-level measurements of damping using both conventional free layer designs and an optimized free layer that combines low damping and low moment and meets LLC requirements.

10:20 AM - 10:45 AM
27.4 Microwave neural processing and broadcasting with spintronic nano-oscillators (Invited), *P. Talatchian, M. Romera, S. Tsunegi*, F. Abreu Araujo, V. Cros, P. Bortolotti, J. Trastoy, K. Yakushiji*, A. Fukushima*, H. Kubota*, S. Yuasa*, M. Ernoult, D. Vodenicarevic, T. Hirtzlin, N. Locatelli, D. Querlioz, J. Grollier, Thales, Univ. Paris-Sud, Université Paris-Saclay, *National Institute of Advanced Industrial Science and Technology (AIST)*

Can we build small neuromorphic chips capable of training deep networks with billions of parameters? This challenge requires hardware neurons and synapses with nanometric dimensions, which can be individually tuned, and densely connected. While nanosynaptic devices have been pursued actively in recent years, much less has been done on nanoscale artificial neurons. In this paper, we show that spintronic nano-oscillators are promising to implement analog hardware neurons that can be densely interconnected through electromagnetic signals. We show how spintronic oscillators maps the requirements of artificial neurons. We then show experimentally how an ensemble of four coupled oscillators can learn to classify all twelve American vowels, realizing the most complicated tasks performed by nanoscale neurons.

10:45 AM - 11:10 AM
27.5 High Endurance Phase Change Memory Chip Implemented based on Carbon-doped $Ge_2Sb_2Te_5$ in 40 nm Node for Embedded Application, *Z. T. Song, D. L. Cai, X. Li, L. Wang*, Y. F. Chen, H. P. Chen, Q. Wang, Y. P. Zhan*, M. H. Ji*, Chinese Academy of Sciences, *Semiconductor Manufacturing International Corporation*

We present the results of a highly reliable PCM based on Carbon-doped Ge2Sb2Te5 material in 40 nm node. The chip exhibits excellent data retention, endurance characteristics, and the sensing window is even larger after 260 °C soldering test. PCM is suitable for applications requiring high thermal stability and cycling endurance.

11:10 AM - 11:35 AM
27.6 A 40nm Low-Power Logic Compatible Phase Change Memory Technology, *J.Y. Wu, Y.S. Chen, W.S. Khwa, S.M. Yu, T.Y. Wang, J.C. Tseng, Y.D. Chih and Carlos H. Diaz, Taiwan Semiconductor Manufacturing Company Ltd.*

An embedded phase change memory technology in 40nm low-power logic platform is demonstrated with minimal added process complexity - two non-critical additional masks over standard logic. Specially designed hard mask and etching process was used to achieve 50% shrinkage of the memory cell bottom electrode dimension with same lithography tooling as the 40nm logic platform. Bottom electrode CD shrinkage along with optimization of the electrode materials in terms of electrical and thermal conductivity enabled significant (~4x) write current reduction attaining competitive levels of ~300 µA at 40nm BE CD. Embedded PCM cells reported in this work demonstrated over 100x memory window - (RESET/SET resistance switching ratio), over 200k cycling endurance with extrapolated 10 year retention at 120 °C. In this work not only large switching resistance ratios but also highly-controllable resistance values that are almost independent of the PCM starting resistance state are presented along with the corresponding programing pulse requirements. The switching resistance ratio and resistance value controllability are key features for neural network and compute-in-memory applications. In this work, their benefits on design

margins for energy efficient high-density binary neural network for inference applications aiming accuracy levels of well over 90% is asserted over an MNIST dataset.

11:35 AM - 12:00 PM
27.7 8-bit Precision In-Memory Multiplication with Projected Phase-Change Memory, *I. Giannopoulos*, A. Sebastian*, M. Le Gallo, V.P. Jonnalagadda, M. Sousa, M.N. Boon, and E. Eleftheriou, IBM Research – Zurich*

In-memory computing is an emerging non-von Neumann approach in which certain computational tasks such as matrix-vector multiplication are performed using resistive memory devices organized in a crossbar array. However, the conductance variations associated with the memory devices limit the precision of this computation. Here, we demonstrate that the so-called projected phase-change memory (Proj-PCM) devices can achieve 8-bit precision while performing scalar multiplication. The devices were fabricated and characterized using electrical measurements and STEM investigation. They are found to be remarkably immune to conductance variations arising from structural relaxation, 1/f noise and temperature variations. Moreover, it is possible to compensate for the temperature-dependent conductance variations in a crossbar array using a simple model. Finally, we experimentally demonstrate a neural network-based image classification task involving 30 such Proj-PCM devices.

Session 28: Circuit and Device Interaction - Advanced CMOS Technology for Computing in the Nanoscale Era
Wednesday, December 5, 9:00 AM
Grand Ballroom B
Co-Chairs: S. Rakheja, New York University
W. Hafez, Intel Corporation

9:05 AM - 9:30 AM
28.1 System Performance: From Enterprise to AI (Invited), *A. Kumar, L. Chang, G.E. Tellez, L.A. Clevenger, and J.L. Burns, IBM Research*

System performance has shown many decades of continuous improvement. After first reviewing historical trends and the current outlook, in this paper we discuss the challenges and opportunities in future computing systems due to the disruptive confluence of stalled scaling and emerging AI workloads. Heterogeneous integration is highlighted as a key means to future systems performance growth.

9:30 AM - 9:55 AM
28.2 Design-Technology Co-Optimization of Standard Cell Libraries on Intel 10nm Process, *X. Wang, R. Kumar, S. Bangalore Prakash, P. Zheng, T.-H. Wu, Q. Shi, M. Nabors, S. C. Gadigatla, S. Realov, C.-H. Chen, Y. Zhang, K. Mistry, A. Yeoh, I. Post, C. Auth, A. Madhavan, Intel Corporation*

This paper highlights the co-optimization of process technology, std. cell library offerings and block-level TFM on Intel 10nm node to enable unprecedented scaling opportunity for products ranging from high performance client/server to low power mobile/IoT segments. The 10nm short height library enables 2.7x transistor density scaling going from 14nm counterpart. The taller height libraries are optimized to meet performance and reliability requirements of Intel's leading edge client/server products. PPA trade-offs are analyzed both at std. cell level and block level on an industry standard Core IP design.

9:55 AM - 10:20 AM
28.3 An Accurate FinFET's Vmin Estimation Method for Extreme Low Operation Voltage Design, *H. W. Choi, S. K. Kim, H. Jung, D. R. Chang, S. Park and Y. Yasuda-Masuoka, and J.S. Yoon Foundry Business, Samsung Electronics Co. Ltd.*

In this paper, the minimum operating voltage (Vmin) estimation methodology for advanced FinFET technology is newly proposed with a manufacturability consideration. The experiment depicts that key factors to determine Vmin are the sum of threshold voltages of n-FET/p-FET, beta-ratio (n/p-FET strength ratio), and random variation. The new equation successfully captures the key electrical features, which is verified by both Monte-Carlo simulation and advanced 11nm/8nm FinFET experimental data. Based on the new model, the paper also provides the guideline for threshold voltage and local mismatch strategy for future advanced FinFET Vmin improvement.

10:20 AM - 10:45 AM

28.4 Tackling Fundamental Challenges of Carrier Transport and Device Variability in Advanced Si *n*FinFETs for 7nm Node and Beyond, *M.-H. Lin, V. S. Chang, J.-H. Lu, S.-H. Wang, and S.-H. Yang, Taiwan Semiconductor Manufacturing Company*

We report that the S/D long-range Coulomb interactions and gate-corner work-function roll-up can be mitigated by S/D epitaxy and HK/MG RPG optimizations, paving the way for 7nm node and beyond. These techniques feature larger Idsat enhancements than that of Idlin. Their signatures and influences on transport parameters are investigated comprehensively.

10:45 AM - 11:10 AM

28.5 Extendable and Manufacturable Volume-less Multi-Vt Solution for 7nm Technology Node and Beyond, *R. Bao, H. Zhou, M. Wang, D. Guo, B. S Haran, V. Narayanan, R. Divakaruni, IBM Semiconductor Technology Research*

We demonstrated more than 3 pairs of threshold voltage (Vt) devices by volume-less multiple Vt (multi-Vt) scheme plus dual work function metals (WFM) without performance and reliability degradation on 20nm gate length FinFET CMOS devices. Vt shifts over 200 mV were achieved for both nFET and pFET. The volume-less nature of this multi-Vt scheme relieves replacement metal gate (RMG) challenges and opens the path to offer multi-Vt solution for future highly scaled technologies.

11:10 AM - 11:35 AM

28.6 Channel Geometry Impact and Narrow Sheet Effect of Stacked Nanosheet, *C. W. Yeung, J. Zhang, R. Chao, O. Kwon*, R. Vega, G. Tsutsui, X. Miao, C. Zhang, C.-W. Sohn*, B. K. Moon**, A. Razavieh**, J. Frougier**, A. Greene, R. Galatage**, J. Li, M. Wang, N. Loubet, R. Robison, V. Basker, T. Yamashita, D. Guo, IBM, *Samsung Electronics, **GLOBALFOUNDRIES*

The characteristics of Stacked Nanosheet are investigated, focusing on channel geometry. For the first time, "narrow sheet effect" on carrier transport is observed. By comparing measured electron and hole mobilities, and the n-type/p-type opposite transconductance (gm) trends versus sheet width (Wsheet), we show that the mobility dependency on Wsheet, is attributed to reduced (100) plane conduction contribution as Wsheet shrinks.

11:35 AM - 12:00 PM

28.7 3nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications (Late News), *G. Bae, D.-I. Bae, M. Kang, S.M. Hwang, S.S. Kim, B. Seo, T.Y. Kwon, T.J. Lee, C. Moon, Y.M. Choi, K. Oikawa, S. Masuoka, K.Y. Chun, S.H. Park, H.J. Shin, J.C. Kim, K.K. Bhuwalka, D.H. Kim, W.J. Kim, J. Yoo, H.Y. Jeon, M.S. Yang, S.-J. Chung, D. Kim, B.H. Ham, K.J. Park, W.D. Kim, S.H. Park, G. Song, Y.H. Kim, M.S. Kang, K.H. Hwang, C.-H. Park, J.-H. Lee, D.-W. Kim, S-M. Jung, H.K. Kang, Samsung Electronics*

As the most feasible solution beyond FinFET is successfully technology, a gate-all-around Multi-Bridge-Channel MOSFET (MBCFET) technology demonstrated including a fully working high density SRAM. MBCFETs are fabricated using 90% or more of FinFET processes with only a few revised masks, allowing easy migration from FinFET process. Not only on-target but also multiple Vt is achieved in challengingly limited vertical spacing between channels. Also, reliability of MBCFETs is shown to be comparable to that of FinFETs. Three representative superior characteristics of MBCFET compared to FinFET have been demonstrated — better gate control with 65 mV/dec sub-threshold swing (SS) at short gate length, higher DC performance with a larger effective channel width (Weff) at reference footprint, and design flexibility with variable nanosheet (NS) widths. The optimization of the standard cell design by using variable NS width is evaluated. The usefulness of MBCFET as a multi-purpose performance provider is proven by the modulation of effective capacitance (Ceff), effective resistance (Reff) and frequency by Weff control. Finally, mass production feasibility with MBCFET is proven through a fully working high density SRAM circuit.

Session 29: Sensors, MEMS, and BioMEMS - Biosensors and Neural Interfaces
Wednesday, December 5, 9:00 AM
Continental Ballroom 1-3
Co-Chairs: D. Kuzum, University of California, San Diego
B. Boyanav, Illumina

9:05 AM - 9:30 AM
29.1 A CMOS Proximity Capacitance Image Sensor with 16µm Pixel Pitch, 0.1aF Detection Accuracy and 60 Frames Per Second, *M. Yamamoto, R. Kuroda, M. Suzuki, T. Goto, H. Hamori*, S. Murakami*, T. Yasuda*, and S. Sugawa, Tohoku University, *OHT Inc.*

A 16µm pixel pitch 60 frames per second CMOS proximity capacitance image sensor fabricated by a 0.18µm CMOS process technology is presented. By the introduction of noise cancelling operation, both fixed pattern noise and kTC noise are significantly reduced, resulting in the 0.1aF detection accuracy. Proximity capacitance imaging results using the developed sensor are also demonstrated.

9:30 AM - 9:55 AM
29.2 3D Expandable Microwire Electrode Arrays Made of Programmable Shape Memory Materials, *R. Zhao, X. Liu, Y. Lu, C. Ren, A. Mehrsa, T. Komiyama and D. Kuzum, University of California San Diego*

Nitinol is biocompatible and widely used in biomedical applications. Here we demonstrate 3D expandable nitinol microwire electrode arrays that can be programmed to conform to the brain vasculature, minimizing blood vessel damage during implantation. In in vivo experiments, our microwire arrays detect single spikes and neural potentials without tissue damage.

9:55 AM - 10:20 AM
29.3 Bio-inspired 3D neural electrodes for the peripheral nerves stimulation using shape memory polymers, *Y. Zhang, N. Zheng*, Y. Ma, T. Xie* and X. Feng, Tsinghua University, *Zhejiang University*

To minimize the mechanical mismatch and facilitate the surgical implantation, bio-inspired 3D neural electrodes that fabricated based on traditional planar processing are proposed, which can be introduced into the body in planar state and self-climb to the 3D peripheral nerves. In vivo animal experiments has demonstrated the potential clinical utility.

10:20 AM - 10:45 AM

29.4 Fabrication and Characterization of 3D Multi-Electrode Array on Flexible Substrate for *In Vivo* EMG Recording from Expiratory Muscle of Songbird, *M. Zia, B. Chung, S. J. Sober*, and M. S. Bakir, Georgia Institute of Technology,*Emory University*

This work presents fabrication and characterization of flexible three-dimensional (3D) multi-electrode arrays (MEAs) capable of high signal-to-noise (SNR) electromyogram (EMG) recordings from the expiratory muscle of a songbird. The fabrication utilizes a photoresist reflow process to obtain 3D structures to serve as the electrodes. A polyimide base with a PDMS top insulation was utilized to ensure flexibility and biocompatibility of the fabricated 3D MEA devices. SNR measurements from the fabricated 3D electrode show up to a 7x improvement as compared to the 2D MEAs.

10:45 AM - 11:10 AM

29.5 Bioelectronics at the Single Molecule Level (Invited), *O. Tolga Gul, K. M. Pugliese*, Y. Choi*, A. J. Rajapakse*, C. J. Lau*, N. Kumar*, K. N. Gabriel*, D. Marushchak*, T. J. Olsen*, D. Pan*, G. A. Weiss*, and P. G. Collins*, Ankara Hacı Bayram Veli University, *University of California at Irvine*

Bioelectronic devices built with single molecules of a protein, enzyme, or aptamer represent a new class of hybrid electronics. When biofunctionalization of nanoscale conductors is reduced to one molecule, that molecule's dynamic activity can be transduced into a large amplitude, high bandwidth electronic output. The resulting single-molecule devices bridge solid state electronics with the world of chemical activity and biological complexity, and they represent a far-reaching, transformative opportunity for molecular electronics. For example, they can capture the dynamic signals generated as target molecules arrive, activate, or bind; and quantitatively reveal the timing, thermodynamics, and rate distributions of complex chemical events like protein-protein recognition, enzymatic activation, or pharmaceutical inhibition. Here, we review recent progress making single-molecule bioelectronic devices using carbon nanotubes as the connective wiring to DNA polymerase I, an example enzyme having complex functionality. The results show how single-molecule bioelectronics can reveal biochemical activity with bond-by-bond resolution.

11:10 AM - 11:35 AM

29.6 Si Nanowire Biosensors Using a FinFET Fabrication Process for Real Time Monitoring Cellular Ion Actitivies, *Q. Zhang, H. Tu, H. Yin*, F. Wei, H. Zhao, C. Xue**, Q. Wei, Z. Zhang*, X. Zhang, S. Zhang, Q. Han**, Y. Li*, R. C. Zhao**, J. Yan***, J. Li*, and W. Wang*, General Research Institute for Nonferrous Metals, *Institute of Microelectronics, CAS, **School of Basic Medicine Peking Union Medical College, ***North China University of Technology*

In this paper, a biocompatible biosensor based on horizontal Si nanowire (NW) array field-effect transistor (FET) has been fabricated by the feasible spacer image transfer (SIT) process. The Si NW FET as biosensor is proposed for the real-time cellular Ca2+ monitoring for mesenchymal stem cells (MSCs), which presents fast-responded and high-sensitive characteristics. Compared with the conventional sensing techniques, the Si NW biosensor exhibits non-invasive, biocompatible and reliable advantages. This will help us to further understand the mechanism of cellular ion activities and provides a promising method for the cell-level diagnose and therapy.

11:35 AM - 12:00 PM

29.7 A Flexible, Heterogeneously Integrated Wireless Powered System for Bio-Implantable Applications using Fan-Out Wafer-Level Packaging, *G. Ezhilarasu, A. Hanna, R. Irwin, A. Alam, and S. S. Iyer, University of California*

Fan-Out Wafer-Level Packaging (FOWLP) is used to fabricate a near field wireless implantable system on an ultra-flexible (~5mm bending radius) & biocompatible elastomeric substrate. A µLED is powered

wirelessly with an efficiency > 15% @ 1cm transmit distance. The implantable system is only ~535µm thick with a diameter <2cm.

Session 30: Power Devices - GaN Power Devices
Wednesday, December 5, 9:00 AM
Continental Ballroom 4
Co-Chairs: E. Morvan, CEA-Leti
T. Narita, Toyota Central R&D Labs, Inc.

9:05 AM - 9:30 AM
30.1 Parallel-Plane Breakdown Fields of 2.8-3.5 MV/cm in GaN-on-GaN p-n Junction Diodes with Double-Side-Depleted Shallow Bevel Termination, *T. Maeda, T. Narita*, H. Ueda*, M. Kanechika*, T. Uesugi*, T. Kachi**, T. Kimoto, M. Horita, and J. Suda, Kyoto University, *Toyota Central R&D Labs., Inc., **Nagoya University*

We report homoepitaxial GaN p-n junction diodes with novel beveled-mesa structures. The n-layers and p-layers, the doping concentrations of which are comparable, were prepared. We found that electric field crowding does not occur in the structure using TCAD simulation. The fabricated devices showed the breakdown voltages of 180-480 V, small leakage currents, and excellent avalanche capabilities. The breakdown voltages increased at elevated temperature. At the breakdown, nearly uniform luminescence in the entire p-n junctions was observed in all the devices. These results are strong evidences that the uniform avalanche breakdowns occurred in the devices. We carefully characterized the depletion layer width at the breakdown, and the parallel-plane breakdown electric fields of 2.8–3.5 MV/cm were obtained, which are among the best of the reported non-punch-through GaN vertical devices.

9:30 AM - 9:55 AM
30.2 Demonstration of avalanche capability in polarization-doped vertical GaN pn diodes: study of walkout due to residual carbon concentration, *C. De Santi, E. Fabris, K. Nomoto*, Z. Hu*, W. Li*, X. Gao**, D. Jena*, H. G. Xing**, G. Meneghesso, M. Meneghini, and E. Zanoni, University of Padova, *Cornell University, **IQE*

We demonstrate and investigate the avalanche capability in vertical GaN-on-GaN pn diodes with polarization doping. We describe the dependence of breakdown voltage on temperature and monochromatic illumination and demonstrate the presence of avalanche walkout, caused by charge trapping due to residual carbon. We develop a model to explain the data.

9:55 AM - 10:20 AM
30.3 Suppressed Hole-Induced Degradation in E-mode GaN MIS-FETs with Crystalline GaO_xN_{1-x} Channel, *M. Hua, X. Cai, S. Yang, Z. Zhang, Z. Zheng, J. Wei, N. Wang, and K. J. Chen, The Hong Kong University of Science and Technology*

Under reverse-bias stress with a high drain voltage, hole-induced gate dielectric degradation in the E-mode GaN MIS-FETs could lead to non-recoverable VTH shifts and devastating time-dependent breakdown. Such a degradation can be effectively suppressed by converting the GaN channel into a crystalline GaO_xN_{1-x} channel in the gated region. The valence band offset between GaOxN1-x and the surrounding GaN creates a hole-blocking ring around the gate dielectric, preventing holes from flowing to the gate dielectric and therefore mitigating the hole-induced degradation.

10:20 AM - 10:45 AM

30.4 Recent advancement of GaN HEMT with InAlGaN barrier layer and future prospects of AlN-based electron devices (Invited), *J. Kotani, A. Yamada, T. Ohki, Y. Minoura, S. Ozaki, N. Okamoto, K. Makiyama, and N. Nakamura, Fujitsu Ltd.*

We have successfully achieved high-power operation of InAlGaN/GaN HEMTs in the wide-frequency range from S-band to W-band. A re-grown n+-GaN contact layer and an InGaN back-barrier layer was employed for the W-band GaN HEMTs. For the S-band GaN HEMTs, 2DEG mobility was improved using the atomically flat AlGaN spacer layers. This technology allows us to reduce the 2DEG densities while maintaining the low access resistance, which contributes to the lower electric-field concentration at the edge of the gate electrodes i.e. enables high voltage operation. Furthermore, we must pay more attention on the thermal-related issues for the S-band, as the increased heat generation hinders stable operation of GaN HEMTs and seriously degrades long-term reliability. In addition to the re-grown n+-GaN layer and the InGaN back-barrier layer used for W-band GaN HEMTs, we employed a single-crystal diamond substrate as a heat spreader and successfully confirmed the further output power density improvement. Finally, we investigated the possibility of AlN- or high Al composition AlGaN-based electron devices as a possible candidate for the next generation devices. In order to break the trade-off between maximum drain current and breakdown voltage, an asymmetric 2DEG channel was investigated. It was found that the thin AlGaN barriers with high Al composition are suitable for high-power devices with asymmetric 2DEG density as the strain effectively applied to the AlGaN/GaN interfaces. To estimate the potential of AlN-based electron devices from a viewpoint of thermal-related issues, we compared the thermal resistance of the AlN devices on AlN substrates with the conventional GaN HEMTs on SiC substrates. It is expected that AlN/AlN structures can reduce the thermal resistance by 26% compared to the conventional GaN on SiC structures. It is believed that the lower thermal resistance will be a large advantage for future high-power devices.

10:45 AM - 11:10 AM

30.5 Power GaN HEMT degradation: from time-dependent breakdown to hot-electron effects (Invited), *M. Meneghini, A. Barbato, M. Borga, C. De Santi, M. Barbato, S. Stoffels*, M. Zhao*, N. Posthuma*, S. Decoutere*, O. Haeberlen**, T. Detzel**, G. Meneghesso, E. Zanoni, University of Padova, *imec, **Infineon*

This paper describes our most advanced results in the field of GaN-HEMT degradation, with focus on power devices. We discuss three main aspects: (i) the dependence of breakdown voltage on substrate and buffer properties; (ii) the existence of time-dependent breakdown of GaN buffer submitted to high vertical stress;(iii) the role of hot-electrons in limiting the dynamic performance of the devices.

Session 31: Nano Device Technology - NCFET Physics and Devices

Wednesday, December 5, 9:00 AM

Continental Ballroom 5

Co-Chairs: K.-L. Cheng, TSMC

T. Yamashita, Renesas Electronics

9:05 AM - 9:30 AM

31.1 New Insights into the Physical Origin of Negative Capacitance and Hysteresis in NCFETs, *H. Wang, M. Yang, Q. Huang, K. Zhu, Y. Zhao, Z. Liang, C. Chen, Z. Wang, Y. Zhong, X. Zhang, R. Huang, Peking University*

In this paper, direct experimental observation of negative capacitance (NC) in a standalone ferroelectric (FE) capacitor is reported for the first time, which proves that the physical origin of NC is the domain switching dynamics rather than the stabilized switching. Based on this origin, the “dynamic polarization (DP) matching”, different from the traditional capacitance matching, is rigorously derived and verified to be the prerequisite for sub-60mV/dec subthreshold swing (SS) in NCFET. The proposed DP matching can

accurately describe and predict the features of NCFET based on our developed device model, showing that the SS and hysteresis are highly sensitive to the input sweeping voltage and FE switching dynamics, as well as other device parameters. Moreover, an intrinsic conflict is found between hysteresis and SS optimization. This work provides new understanding for the NCFET mechanism.

9:30 AM - 9:55 AM

31.2 A Critical Examination of 'Quasi-Static Negative Capacitance' (QSNC) theory, *Z. Liu, A. Bhuiyan, and T. P. Ma, Yale University*

Recent years have seen a boom in the interest of using the alleged ferroelectric 'negative capacitance' to realize low subthreshold swing of MOSFETs. According to the "quasistatic negative capacitance' (QSNC) theory, a ferroelectric (FE) capacitor has an intrinsic but unstable 'negative capacitance' (NC) region. By adding a matching linear dielectric (DE) capacitor in series, it is possible to 'stabilize' the NC region. In this work, we examined the validity of the QSNC theory, and performed several key experiments to verify that experimental results are consistent with our theoretical assessment. Unfortunately, our overall results do not support the QSNC theory.

9:55 AM - 10:20 AM

31.3 Direct relationship between sub-60 mV/dec subthreshold swing and internal potential instability in MOSFET externally connected to ferroelectric capacitor, *X. Li, A. Toriumi, The University of Tokyo*

Negative-capacitance effect on subthreshold-swing (SS) improvement in ferroelectric-FETs is still under debate. We demonstrate the direct correlation between sub-60 mV/dec SS and internal-potential enhancement in MOSFET externally connected to ferroelectric-capacitor. The results support that reported steep SS are tightly related to ferroelectric domain switching rather than the ideal negative-capacitance effect.

10:20 AM - 10:45 AM

31.4 Assessment of Steep-Subthreshold Swing Behaviors in Ferroelectric-Gate Field-Effect Transistors Caused by Positive Feedback of Polarization Reversal, *S. Migita, H. Ota, and A. Toriumi*, National Institute of Advanced Industrial Science and Technology (AIST), *The University of Tokyo*

Steep-subthreshold swing (SS) behaviors in ferroelectric-gate field-effect transistors (Fe-FETs) are investigated using the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) gates stack structures with different area ratios between MIS and MFM capacitors. It is analyzed that the capacitance matching between them by adjusting the area ratio is significant to efficiently utilize the polarization reversal behavior in the ferroelectric layer. In this work we explain the steep-SS behavior from viewpoint of positive feedback of polarization reversal. Furthermore it is discussed why steep-SS is observable in recent Fe-FETs.

10:45 AM - 11:10 AM

31.5 Experimental Study on The Role of Polarization Switching in Subthreshold Characteristics of HfO_2-based Ferroelectric and Anti-ferroelectric FET, *C. Jin, K. Jang, T. Saraya, T. Hiramoto, and M. Kobayashi, The University of Tokyo*

We have experimentally studied and revealed the direct relationship between polarization switching and steep subthreshold slope (SS) characteristics of HfO2-based ferroelectric FET (FeFET) and Anti-FeFET (A-FeFET) by systematically designing and fabricating devices, and monitoring Ig with high resolution, for the first time. In the circumstances that charge injection prevents polarization switching from occurring in subthreshold region of FeFET, we have obtained two major findings: (1) Sub-60 SS as low as 23.5 mV/dec is observed by adjusting Vg bias sequence, which is attributed to charge injection assisted by

polarization switching. (2) Anti-ferroelectric facilitates to align polarization switching in subthreshold region and SS can be improved in A-FeFET as a consequence, which is directly observed by monitoring I_g.

11:10 AM - 11:35 AM

31.6 Demonstration of High-speed Hysteresis-free Negative Capacitance in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$, *M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, NaMLab gGmbH*

We report the experimental observation of hysteresis-free negative capacitance (NC) in thin ferroelectric Hf0.5Zr0.5O2 (HZO) films through high-speed pulsed charge-voltage measurements. Hysteretic switching is suppressed by the addition of thin Al2O3 layers on top of the HZO to prevent the screening of the polarization. We observe an S-shaped polarization-electric field dependence without hysteresis in agreement with Landau theory, which enables direct extraction of NC modeling parameters for ferroelectric HZO. Hysteresis-free NC is demonstrated down to 100 ns pulse widths limited only by our measurement setup. These results give critical insights into the physics of ferroelectric NC and practical NC device design using ferroelectric HZO.

11:35 AM - 12:00 PM

31.7 Negative-Capacitance FinFET Inverter, Ring Oscillator, SRAM Cell, and Ft, *K.-S. Li, Y.-J. Wei, Y.-J. Chen, W.-C. Chiu, H.-C. Chen, M.-H. Lee*, Y.-F. Chiu, F.-K. Hsueh, B.-W.Wu, P.-G. Chen, T.-Y. Lai, C.-C. Chen, J.-M. Shieh, W.-K. Yeh, S. Salahuddin***, C. Hu**, National Applied Research Laboratories, *National Taiwan Normal University, **National Chiao Tung University, ***University of California, Berkeley*

In this work, we use thermal-ALD to prepare ferroelectric HfZrO2 (HZO) thin film with thickness from 3 to 7 nm for the NC-FinFET's gate stack. The subthreshold swing (SS) was as low as 5 mV/dec (SSmin) over 4 orders of ID. Lower thermal budget process, CO2 far-infrared laser activation and 400 oC Ni silicide were employed in the 2-level metal backend integration for maintaining orthorhombic phase in HZO thin film and minimizing the hysteresis in IV. NC-FinFET inverter has 77% higher voltage gain compared to FinFET-inverter employing HfO2 gate dielectric. NC-FinFET ring oscillator exhibited small speed and power advantages over FinFET oscillator. For the first time, NC-FET cut-off frequency (Ft) frequency is measured, 23.08 GHz for NC-FniFET versus 18.85 GHz for the control FinFET and NC-FinFET SRAM was observed to exhibit excellent noise margin.

12:00 PM - 12:25 PM

31.8 Extremely Steep Switch of Negative-Capacitance Nanosheet GAA-FETs and FinFETs, *M. H. Lee, K.-T. Chen, C.-Y. Liao, S.-S. Gu, G.-Y. Siang, Y.-C. Chou, H.-Y. Chen, J. Le, R.-C. Hong, Z.-Y. Wang, S.-Y. Chen, P.-G. Chen*, M. Tang**, Y.-D. Lin***, H.-Y. Lee***, K.-S. Li*, and C. W. Liu+, National Taiwan Normal University, *National Nano Device Laboratories, ** PTEK Technology Co., Ltd, ***Industrial Technology Research Institute, +National Taiwan University*

Extremely steep switch of NC Nanosheet (NS) GAA-FETs and FinFETs are experimentally presented with SSavg/SSmin=22/14mV/dec and SSavg/SSmin=38/21mV/dec, respectively. The sub-60mV/dec current magnitude of sub-60mV/dec is >4 and ~5 decades for NC-NSGAA and NC-FinFET, respectively, as well as apparent N-DIBL and NDR. The SS depends on WFin/L ratio, and WFin < L is the solution to achieve sub-60mV/dec. The uniform size of each NS for stacked NC-NSGAA is an important issue to optimize the NC effect with SS=19mV/dec.

Session 32: Optoelectronics, Displays, and Imagers - CMOS Photodetectors

Wednesday, December 5, 9:00 AM

Continental Ballroom 7-9

Co-Chairs: S. Pellegrini, STMicroelectronics
P. Malinowski, imec

9:05 AM - 9:30 AM
32.1 Optocoupling in CMOS, *V. Agarwal, S. Dutta, A. J. Annema, R. J. E. Hueting, J. Schmitz, M.-J. Lee*, E. Charbon* and B. Nauta, University of Twente, *EPFL*

This is the first experimental demonstration of data communication using a monolithically integrated optocoupler realized in a standard CMOS technology without any post-processing. The proposed optocoupler occupies very low area, can achieve data rate of a few Mbps and is very attractive for intra-chip communication and smart power applications.

9:30 AM - 9:55 AM
32.2 High Voltage Generation Using Deep Trench Isolated Photodiodes in a Back Side Illuminated Process, *F. Kaklin, J. M. Raynor*, R. K. Henderson, The University of Edinburgh, *STMicroelectronics Imaging Division*

We demonstrate passive high voltage generation using photodiodes biased in the photovoltaic region of operation. The photodiodes are integrated in a 90nm back side illuminated (BSI) deep trench isolation (DTI) capable imaging process technology. Four equal area, DTI separated arrays of photodiodes are implemented on a single die and connected using on-chip transmission gates (TG). The TGs control interconnects between the four arrays, connecting them in series or in parallel. A series configuration successfully generates an open-circuit voltage of 1.98V at 1klux. The full array generates 423nW/mm2 at 1klux of white LED illumination in series mode and 425nW/mm2 in parallel mode. Peak conversion efficiency is estimated at 16.1%, at 5.7klux white LED illumination.

9:55 AM - 10:20 AM
32.3 Through-silicon-trench in back-side-illuminated CMOS image sensors for the improvement of gate oxide long term performance, *A. Vici, F. Russo*, N. Lovisi*, L. Latessa*, A. Marchioni*, A. Casella*, F. Irrera, Sapienza University of Rome, *LFoundry, a SMIC Company*

To improve the gate oxide long term performance of MOSFETs in back side illuminated CMOS image sensors the wafer back is patterned with suitable through-silicon-trenches. We demonstrate that the reliability improvement is due to the annealing of the gate oxide border traps thanks to passivating chemical species carried by trenches.

10:20 AM - 10:45 AM
32.4 High-Performance Germanium-on-Silicon Lock-in Pixels for Indirect Time-of-Flight Applications, *N. Na, S.-L. Cheng, H.-D. Liu, M.-J. Yang, C.-Y. Chen, H.-W. Chen, Y.-T. Chou, C.-T. Lin, W.-H. Liu, C.-F. Liang, C.-L. Chen, S.-W. Chu, B.-J. Chen, Y.-F. Lyu, and S.-L. Chen, Artilux Inc.*

We investigate and demonstrate the first Ge-on-Si lock-in pixels for indirect time-of-flight measurements. Compared to conventional Si lock-in pixels, such novel Ge-on-Si lock-in pixels simultaneously maintain a high quantum efficiency and a high demodulation contrast at a higher operation frequency, which enable consistently superior depth accuracies for both indoor and outdoor scenarios. System performances are evaluated, and pixel quantum efficiencies are measured to be >85% and >46% at 940nm and 1550nm wavelengths, respectively, along with demodulation contrasts measured to be >0.81 at 300MHz. Our work may open up new routes to high-performance indirect time-of-flight sensors and imagers, as well as potential adoptions of eye-safe lasers (e.g. wavelengths > 1.4μm) for consumer electronics and photonics.

10:45 AM - 11:10 AM

32.5 CMOS-Integrated Single-Photon-Counting X-Ray Detector using an Amorphous-Selenium Photoconductor with 11×11-μm^2 Pixels, *A. Camlica, A. El-Falou, R. Mohammadi, P. M. Levine, and K. S. Karim, University of Waterloo*

We report, for the first time, results from a single-photon-counting X-ray detector monolithically integrated with an amorphous semiconductor. Our prototype detector combines amorphous selenium (a-Se), a well-known X-ray photoconductive material suitable for large-area applications, with a 0.18-μm-CMOS readout integrated circuit containing two 26×196 photon counting pixel arrays. The detector features 11×11-um2 pixels to overcome a-Se count-rate limitations by unipolar charge sensing of the faster charge carriers (holes) via a unique pixel geometry that leverages the small pixel effect for the first time in an amorphous semiconductor. Measured results from a mono-energetic radioactive source are presented and demonstrate the untapped potential of using amorphous semiconductors for high-spatial-resolution photon-counting X-ray imaging applications.

Session 33: Modeling and Simulation - Device, Process and Reliability Modeling
Wednesday, December 5, 9:00 AM
Plaza A
Co-Chairs: S. Cea, Intel
W. Vandenberghe, University of Texas, Dallas

9:05 AM - 9:30 AM
33.1 Transport models based on NEGF and empirical pseudopotentials: a computationally viable method for self-consistent simulation of nanoscale devices., *M. G. Pala, O. Badami* and D. Esseni*, Univ. Paris-Sud, Universit´e Paris-Saclay, *University of Udine*

We present new theoretical developments and applications concerning Non-Equilibrium Green's Functions (NEGF) based transport modelling with an Empirical Pseudopotential (EP) Hamiltonian. We have extended the methodology to include arbitrary crystal orientations and strain conditions, and have reformulated quantum confinement and spatial discretization to improve the computational efficiency.

9:30 AM - 9:55 AM
33.2 First Principles Simulation of Energy efficient Switching by Source Density of States Engineering (Invited), *F. Liu, C. Qiu, Z. Zhang, L.-M. Peng, J. Wang*, Z. Wu**, and H. Guo, Peking University, *The University of Hong Kong, ** Institute of Microelectronics, Chinese Academy of Sciences*

Achieving sub-60 mV/decade FET switching is critical for reducing power dissipation in integrated circuits. Here we propose and theoretically investigate steep slope switching made possible by a “cold source” that suppresses “hot” electrons at the thermal tail of the Fermi distribution. We show sub-60 mV/decade switching with: (i) using gapless/gapped graphene as injection source, (ii) introducing a band gap in the source of Si FET. The feasibility and design of the cold source are investigated by first principles on different metals, pocket doping and disorder.

9:55 AM - 10:20 AM
33.3 Universal Swing Factor Approach For Performance Analysis Of Logic Nodes, *M. A. Pourghaderi, A.-T. Pham*, S. Kim, H. Chung, Z. Jiang*, H. Ilatikhameneh*, H.-H. Park*, S. Jin*, J. Kim, W.-Y. Chung, U. Kwon, W. Choi*, D. S. Kim and S. Maeda, Samsung Electronics, *Samsung Semiconductor Inc.*

Deterministic Boltzmann-transport solver has been integrated in performance analysis of logic cells. Employing universal-swing-factor (USF) approach, our setup accurately entails quasi-ballistic transport effects. The injection current and carrier mean free path (MFP) have been extracted for various channel

dimensions and interface qualities. The resulting database is used to study candidate architecture for logic nodes. In particular, performance of ring oscillator (RO) with tapered FinFET is presented. For a given junction profile and contact-poly-pitch (CPP), the optimum gate-length (Lg), spacer thickness and contact-CD (CCD) are evaluated. The feasible gain by lowering the spacer k-value and contact resistance is also reported.

10:20 AM - 10:45 AM
33.4 Multi-domain process modeling for advanced logic and memory devices: from equimpments to materials (Invited), *I. Jang, H. Ko, A. Schmidt, S.-J. Kim, M. Cha, H. Ahn, H. Park, D. S. Kim, and H.-K. Kang, Samsung Electronics Co. Ltd.*

For modern semiconductor devices, the level of details which we should investigate for predictive simulation is going extreme. Not only the atomistic simulation is required but equipment and transistor scale simulation is also needed to understand the formation of atomic scale feature. In this paper, practical applications of multi-domain simulations are introduced for advanced S/D process in logic, interface engineering in DRAM cell and cell stack ALD process of flash memory devices.

10:45 AM - 11:10 AM
33.5 Entire Bias Space Statistical Reliability Simulation By 3D-KMC Method and Its Application to the Reliability Assessment of Nanosheet FETs based Circuits, *W. Chen, Y. Li, L. Cai, P. Chang, G. Du and X. Liu, Peking University*

The trap behaviors based 3D-Kinetic Monte Carlo (KMC) simulator is developed for statistical reliability assessment over the entire bias space. The main features include (i) physical insight into trap charging/discharging, coupling and generation/recombination behaviors for tracking trap-induced degradation of MOSFETs with multilayer gate dielectrics in the entire bias space. (ii) simulation of statistical reliability for the MOSFETs biased under arbitrary mixed stress conditions. (iii) assessment of reliability degradation in circuit operations with various Vg/Vd stress patterns and self-heating. The statistical reliability in nanosheet (NS) FETs and corresponding circuits are investigated. The impacts of the initial interface state and bulk trap density on the threshold voltage shift during the stress and relaxation phases are also analyzed.

11:10 AM - 11:35 AM
33.6 A Physics-based Thermal Model of Nanosheet MOSFETs for Device-Circuit Co-design, *L. Cai, W. Chen, P. Chang, G. Du, X. Zhang, J. Kang and X. Liu, Peking University*

A physics-based thermal model is developed to describe the self-heating effects (SHE) on nanosheet MOSFETs. Three stages of transient temperature response due to the anisotropic heat dissipation and asymmetrical temperature distribution are well understood by the thermal RC network model, providing the physical insight into frequency-dependent SHE in AC operation. The proposed model is further implemented into SPICE simulator for high-efficient thermal assessment in circuit level by the flexible BEOL. Layout design in inverter cell correlated with thermal behavior is investigated for static and transient operation downwards 3nm CMOS node. The SHE and thermal-aware reliability in inverter-based ring oscillator are predicted. The thermal model can be used as a device-circuit co-design tool to assess the thermal behavior accurately and efficiently.

Session 34: Characterization, Reliability, and Yield - Advanced Technology Reliability
Wednesday, December 5, 9:00 AM
Plaza B
Co-Chairs: G. Reimbold, CEA-Leti
B. Weir, Broadcom, Inc.

9:05 AM - 9:30 AM

34.1 Understanding the intrinsic reliability behavior of n-/p-Si and p-Ge nanowire FETs utilizing degradation maps, *A. Chasin, E. Bury, J. Franco, B. Kaczer, M. Vandemaele, H. Arimura, E. Capogreco, L. Witters, R. Ritzenthaler, H. Mertens, N. Horiguchi, D. Linten, imec*

We compare and model the main reliability limitations of stacked Gate-All-Around (GAA) n-/p-channel Silicon and strained p-channel Germanium Nanowire (NW) transistors. Stress measurements in the entire {VG,VD} space allow to separate the different degradation modes and how they interact with each other. We show that these degradation modes are not universal, as they have a different relative weight depending on the considered technology, and that they can show different acceleration mechanisms. Moreover, we also discuss the impact of self-heating effects (SHE) by means of activation energy extraction in the entire {VG,VD} map.

9:30 AM - 9:55 AM

34.2 BTI Reliability Improvement Strategies in Low Thermal Budget Gate Stacks for 3D Sequential Integration, *J. Franco, Z. Wu, G. Rzepa*, A. Vandooren, H. Arimura, L.-Å Ragnarsson, G. Hellings, S. Brus, D. Cott, V. De Heyn, G. Groeseneken, N. Horiguchi, J. Ryckaert, N. Collaert, D. Linten, T. Grasser*, B. Kaczer, imec, *TU Wien*

Low thermal budget gate-stacks will be required for novel integration schemes, such as 3D Sequential stacking of device tiers. We demonstrate two strategies to tolerate the inherently larger high-k defect densities: i) replacing inversion mode devices with highly doped junction-less transistors, or ii) engineering dipoles at the SiO2/HfO2 interface to minimize the carrier-defect interaction. The latter approach is demonstrated for nMOS PBTI and, for the first time, also for pMOS NBTI.

9:55 AM - 10:20 AM

34.3 Characterization and understanding of slow traps in GeO_x-based n-Ge MOS interfaces, *M. Ke, P. Cheng, K. Kato, M. Takenaka, and S. Takagi, The University of Tokyo*

The properties of slow electron traps in n-Ge MOS interfaces over a wide range of electrical field across gate oxides (Eox) are systematically investigated. It is found through careful examination of the C-V hysteresis that slow trapping under low Eox conditions is attributed only to electron trapping into existing slow traps. Under large Eox conditions, on the other hand, generation of slow electron traps and hole trapping are found to additionally affect the slow trapping characteristics. We propose a new measurement scheme to discriminate existing and generated slow electron traps and apply this method to the three different GeOx-based MOS interfaces in order to clarify the nature of slow traps. It is revealed from this analysis that a pre-plasma oxidation process reduces existing slow electron traps and improves slow trapping in low Eox. On the other hand, ultrathin Y2O3 insertion reduces generation of slow electron traps and improves slow trapping in high Eox.

10:20 AM - 10:45 AM

34.4 Soft Error Trends in Advanced Silicon Technology Nodes (Invited), *B. Bhuva, Vanderbilt University*

Soft errors for planar and FinFET nodes have shown different trends for various designer-controlled parameters. This paper examines effects of some of these parameters for the 20-nm Planar and the 16-nm FinFET technology nodes. Latchup vulnerability of FinFET node is also investigated through simulations.

10:45 AM - 11:10 AM

34.5 CMOS-Compatible Doped-Multilayer-Graphene Interconnects for Next-Generation VLSI, *J. Jiang, J. H. Chu, and K. Banerjee, University of California, Santa Barbara*

Cu interconnects suffer from steep rise in resistivity and severe reliability degradation for sub-20 nm line widths. Other metals, including Co and Ru, have been demonstrated with higher electromigration (EM) resistance, but exhibit lower electrical conductivity that degrades circuit performance. This work reports multilayer graphene (MLG) directly grown on SiO2 substrate at 300 °C by a novel pressure-assisted solid-phase diffusion synthesis method, and, for the first time, demonstrates a CMOS-compatible intercalation doped graphene nanoribbon (DGNR) interconnect technology with smaller electrical resistivity than Cu, Co and Ru interconnects. The DGNR interconnect also exhibits < 4% conductivity degradation over 1000 hours at room temperature (RT) without any encapsulation or barrier layer, and negligible EM under 100 MA/cm2 current stress test at > 100 °C. The high current carrying capability of DGNR allows more aggressive vertical scaling w.r.t Cu, Co, or Ru, leading to lower parasitics and significantly smaller switching energy.

11:10 AM - 11:35 AM

34.6 Time Dependent Early Breakdown of AlGaN/GaN Epi Stacks and Shift in SOA Boundary of HEMTs Under Fast Cyclic Transient Stress, *B. Shankar, A. Soni, S. D. Gupta, S. Shikha, S. Singh, S. Raghavan and M. Shrivastava, Indian Institute of Science*

This experimental study reports first observations of (i) SOA boundary shift in GaN HEMTs and (ii) early time to fail of vertical AlGaN/GaN Epi stack under fast changing (sub-10ns risetime) cyclic transient stress conditions for a 600V qualified commercial grade HEMT stack. It is shown that a stack qualified for 10 years lifetime under DC stress, fails faster under cyclic transient stress. Integrated electrical and mechanical stress characterization routine involving Raman/PL mapping and CL spectroscopy reveals material limited unique failure physics under transient stress condition. Failure analysis using cross-sectional TEM investigations reveal signature of different degradation and failure mechanism under transient and DC stress conditions. A failure model is proposed for failure under cyclic transient stress.

Session 35: Process and Manufacturing Technology - Advanced Channel and Contact Technologies
Wednesday, December 5, 1:30 PM
Grand Ballroom B
Co-Chairs: Y. Zhao, Zhejiang University
T. Yamaguchi, Renesas

1:35 PM - 2:00 PM

35.1 Toward High Performance SiGe Channel CMOS: Design of High Electron Mobility in SiGe nFinFETs Outperforming Si, *C. H. Lee, R. G. Southwick III, S. Mochizuki, J. Li, X. Miao, M. Wang, R. Bao, I. Ok, T. Ando*, P. Hashemi*, D. Guo, V. Narayanan*, N. Loubet, and H. Jagannathan, IBM Research and *IBM T. J. Watson Research Center*

For the first time, high electron mobility in tensile-strained SiGe channel nFinFETs outperforming Si is reported to explore the feasibility of high performance SiGe CMOS. To examine the electron mobility behaviors in SiGe channel, a series of tensile-strained SiGe nFinFETs are fabricated on various strain relaxed buffer layers by taking into account the minimum threading dislocation density and strain engineering. For SiGe (Ge >20%) nFinFETs, we identify the existence of additional electron trapping site close to the conduction band edge in IL/HK, leading to the abnormal Vt shift, PBTI degradation, and low electron mobility. We also fabricated short-channel SiGe nFinFETs, which exhibit excellent cut-off behavior and electrostatics (SS ~65mV/dec and DIBL ~18mV at VDD=0.7V). In addition, the dynamic performance of tensile-strained SiGe CMOS against Si CMOS is evaluated by TCAD simulation based on experimental data.

2:00 PM - 2:25 PM

35.2 Advanced Arsenic Doped Epitaxial Growth for Source Drain Extension Formation in Scaled FinFET Devices, *S. Mochizuki, B. Colombeau*, L. Yu, A. Dube*, S. Choi, M. Stolfi*, Z. Bi, F. Chang*, R. A. Conti, P. Liu*, K. R. Winstel, H. Jagannathan, H.-J. Gossmann*, N. Loubet, D. F. Canaperi, D. Guo, S. Sharma*, S. Chu*, J. Boland*, Q. Jin*, Z. Li*, S. Lin*, M. Cogorno*, M. Chudzik*, S. Natarajan*, D. C. McHerron and B. Haran, IBM Research, *Applied Materials*

In this paper, we demonstrate a novel Source Drain Extension (SDE) approach to enable NMOS device scaling along with improved performance. For the first time, SDE formation with epitaxially grown As doped Si (Si:As) has been examined and compared to the current state-of-the-art SDE formation in FinFET at 10nm logic ground rules. It is found that a Si:As layer based SDE provides a clear improvement in the short channel effect and a significant device performance increase. It is also shown that a careful co-optimization of the Si:As layer and Source / Drain (S/D) lateral recess is required to achieve the optimum device gain. This paves the way for the ultimate nSDE formation for current and next generation CMOS devices.

2:25 PM - 2:50 PM

35.3 External Resistance Reduction by Nanosecond Laser Anneal in Si/SiGe CMOS Technology, *O. Gluschenkov, H. Wu, K. Brew, C. Niu*, L. Yu, Y. Sulehria, S. Choi, C. Durfee, J. Demarest, A. Carr, S. Chen*, J. Willis*, T. Thanigaivelan*, F.-L. Lie, W. Kleemeier*, and D. Guo, IBM Research, *GLOBALFOUNDRIES Inc., **ULTRATECH*

Significant pFinFET external resistance reduction (~40%) was achieved by nanosecond laser annealing of S/D structures. Selective melting of S/D elements is responsible for this improvement. Short channel characteristics are not degraded within the identified process window. Contacted gate pitch and fin number dependence of the process window is assessed.

2:50 PM - 3:15 PM

35.4 Parasitic Resistance Reduction Strategies for Advanced CMOS FinFETs Beyond 7nm, *H. Wu, O. Gluschenkov, G. Tsutsui, C. Niu, K. Brew, C. Durfee, C. Prindle, V. Kamineni, S. Mochizuki, C. Lavoie, E. Nowak, Z. Liu, J. Yang, S. Choi, J. Demarest, L. Yu, A. Carr, W. Wang, J. Strane, S. Tsai, Y. Liang, H. Amanapu, I. Saraf , K. Ryan, F. Lie, W. Kleemeier, K. Choi, N. Cave, T. Yamashita, A. Knorr, D. Gupta, B. Haran, D. Guo, H. Bu, and M. Khare, IBM Semiconductor Technology Research*

This work thoroughly investigates the external parasitic resistance in advanced FinFET technology. The optimization of the parasitic resistance is systematically examined in terms of 1) source/drain epi resistance, 2) contact resistance and 3) middle of line metal stud resistance. Various resistance reduction knobs have been experimentally explored in these three aspects and low contact resistivity of 1×10^{-9} and 7×10^{-10} Ωcm2 have been demonstrated on transistor level for NFET and PFET. By combining all the parasitic resistance reduction strategies, more than 70% and 60% reductions in external parasitic resistance have been realized on NFET and PFET, respectively.

3:15 PM - 3:40 PM

35.5 Sub-10-9 Ω-cm2 Specific Contact Resistivity on P-type Ge and GeSn: *In-situ* Ga Doping with Ga Ion Implantation at 300 °C, 25 °C, and -100 °C, *Y. Wu, L.-H. Chua*, W. Wang, K. Han, W. Zou*, T. Henry*, and X. Gong, National University of Singapore (NUS), *Applied Materials-Varian Semiconductor Equipment*

For the first time, Ga ion implantation (Ga I/I) on in-situ Ga-doped Ge (Ge:Ga) and GeSn (GeSn:Ga) films at various temperatures (300 °C, 25 °C, and -100 °C) was investigated. It is found that cryogenic (-100 °C)

and room temperature (RT, 25 °C) Ga I/I retains strain and the high quality of the GeSn layer after Ga activation while hot Ga I/I (300 °C) degrades the crystalline quality due to the implantation-induced defects. An ultra-low specific contact resistivity ρ_c of 8×10^{-10} Ω-cm^2 is achieved for Ti/p+-GeSn contact by in-situ Ga doping followed by cryogenic or RT Ga I/I while ρ_c increases to 2.3×10^{-9} Ω-cm^2 using hot Ga I/I. An ultra-low ρ_c of 9×10^{-10} Ω-cm^2 is also demonstrated for in-situ Ga-doped Ge followed by RT Ga I/I. This is the first realization of sub-10^{-9} Ω-cm^2 ρ_c on non-laser-annealed p-type Ge. The sub-10^{-9} Ω-cm^2 ρ_c is thermally stable up to an annealing temperature of 500 °C.

3:40 PM - 4:05 PM
35.6 Selective Fin Trimming after Dummy Gate Removal as the Local Fin Width Scaling Approach for N5 and Beyond, *T. Miyashita, S. Sun, S.Mittal, M. S. Kim, A. Pal, A. Sachid, K. Pathak, M. Cogorno, and N. S. Kim, Applied Materials Inc.*

Selective fin trimming after dummy gate removal is proposed as the local fin width scaling approach for further FinFET extension. TCAD simulation shows that the local fin trimming can improve electrostatics, while also providing the benefits of lower S/D resistance and PMOS high channel stress. Although, fin height reduction and parasitic capacitance increases are penalty, overall gate delay is improved due to strong Ion-Ioff boost. SelectraTM etch fin trimming is also presented demonstrating good fin width controllability and smaller variations without any critical fin damages.

Session 36: Nano Device Technology - Spintronic Devices and Applications
Wednesday, December 5, 1:30 PM
Continental Ballroom 1-3
Co-Chairs: Z. Chen, Purdue University
H. Fukutome, Samsung

1:35 PM - 2:00 PM
36.1 First experimental demonstration of a scalable linear majority gate based on spin waves, *F. Ciubotaru, G. Talmelli, T. Devolder*, O. Zografos, M. Heyns, C. Adelmann, and I. P. Radu, imec, *Univ. Paris-Sud*

We report on the first experimental demonstration of majority logic operation using spin waves in a scaled device with an in-line input and output layout. The device operation is based on the interference of spin waves generated and detected by inductive antennas in an all-electrical microwave circuit. We demonstrate the full truth table of a majority logic function with the ability to distinguish between strong and weak majority, as well as an inverted majority function by adjusting the operation frequency. Circuit performance projections predict low energy consumption compared to CMOS for large arithmetic circuits.

2:00 PM - 2:25 PM
36.2 Spintronic devices for low energy dissipation (Invited), *K. L. Wang, H. Wu, S. A. Razavi, and Q. Shao, University of California, Los Angeles*

Spintronic devices are considered as one of the best candidates for next-generation electronics to complement CMOS technology. First, we will briefly show the recent progresses on spintronic devices based on spin-transfer torque, spin-orbit torque and voltage-controlled magnetic anisotropy in reference to energy efficient applications. We will then discuss the recent progresses using antiferromagnets and topological insulators for applications in memory, logic and circuits. Finally, the new prospective of 2D materials for spintronic devices will be addressed.

2:25 PM - 2:50 PM

36.3 Room Temperature Highly Efficient Topological Insulator/Mo/CoFeB Spin-Orbit Torque Memory with Perpendicular Magnetic Anisotropy, *Q. Shao, H. Wu, Q. Pan, P. Zhang, L. Pan, K. Wong, X. Che and K. L. Wang, University of California, Los Angeles*

Spin-orbit torque (SOT)-MRAM is a promising candidate for future nonvolatile memory technology. Finding materials that have large SOT efficiency (ξ_{DL}) is critical for developing the SOT-MRAM. Topological insulators (TIs) have been shown to exhibit giant ξ_{DL} (>1) at room temperature. However, integration of high ξ_{DL} TIs with CoFeB with perpendicular magnetic anisotropy (PMA) at room temperature (RT) has not been achieved. In this work, we demonstrate a record-high ξ_{DL} (~2.66) in the (BiSb)2Te3 with PMA CoFeB and achieve magnetization switching with TI current density as low as $3x10^9 A/m^2$ at RT. For the first time, we propose to insert a light metal spacer between TI and CoFeB to achieve resistance matching and thus reduce write energy. We show that without insertion, TI/CoFeB show in-plane magnetic anisotropy but TIs show high ξ_{DL}, consistent with previous reports. We then insert a Mo spacer to achieve PMA at RT. We accurately determine the ξ_{DL} using both second harmonic method and MOKE for the first time. We investigate the SOT-driven switching and discover a memristor-like behavior in the TI/Mo/CoFeB.

2:50 PM - 3:15 PM

36.4 Scaled spintronic logic device based on domain wall motion in magnetically interconnected tunnel junctions, *E. Raymenants, D. Wan, S.Couet, O. Zografos,V.D. Nguyen, A.Vaysset, L. Souriau, A. Thiam, M. Manfrini, S. Brus, M. Heyns, D. Mocuta, D.E. Nikonov*, S. Manipatruni*, I. A. Young*, T. Devolder** and I. P. Radu, imec, *Intel Corporation, **Univ. Paris-Sud, Univ. Paris-Saclay*

We present a scaled device based on magnetic domain wall (DW) transport for logic applications. The device consists of multiple magnetic tunnel junctions (MTJs) connected by the same magnetic free layer (FL). Magnetic domain walls are injected by spin-transfer torque (STT) at the input MTJs and are sensed by tunneling magnetoresistance (TMR) at the output MTJ after propagation through the FL. Logic functions can be built by merging several domain walls. By enabling real-time detection of long range DW transport, we demonstrate a spintronic component which can be used for either Boolean or non-Boolean logic.

3:15 PM - 3:40 PM

36.5 Binary and Ternary True Random Number Generators based on Spin Orbit Torque, *H. Chen, S. Zhang, N. Xu*, M. Song**, X. Li, R. Li, Y. Zeng, J. Hong, L. You, Huazhong University of Science and Technology, *University of California, Berkeley, ** Hubei University*

In this work, we have experimentally demonstrated the binary- and ternary- True Random Number Generators (B-TRNG and T-TRNG) based on the stochastic switching characteristics of the nano-scale Ta/CoFeB/MgO heterostructures with perpendicular magnetization anisotropy. For the first time, the random code generation utilizes the spin orbit torque (SOT) induced by current flowing in the heavy metal underneath the CoFeB layer. The 3-XOR post-processed binary random codes pass the NIST SP800-22 test. Furthermore, the T-TRNG provides a much higher security level as compared to the B-TRNG counterpart.

Session 37: Memory Technology - 1S1R Arrays and Select Devices

Wednesday, December 5, 1:30 PM

Continental Ballroom 4

Co-Chairs: C. Petti, Western Digital Corp.

T. Yamaguchi, Toshiba Memory Corporation

1:35 PM - 2:00 PM

37.1 High-performance, cost-effective 2z nm two-deck cross-point memory integrated by self-align scheme for 128 Gb SCM, *T. Kim, H. Choi, M. Kim, J. Yi, D. Kim, S. Cho, H. Lee, C. Hwang, E.-R. Hwang, J. Song, S. Chae, Y. Chun, J.-K. Kim, SK-Hynix*

We demonstrate a high-performance and cost-effective cross-point memory (CPM) technology for two-deck 128 Gb storage class memory (SCM). The unit MAT size is 16 Mb consisting of a 2z nm 1S1M (one selector one memory) structure that is patterned by only two ArF-i steps per deck for a low cost per bit. The formidable task of self-align etch is enabled by the use of state-of-the-art etching and integration technology, which otherwise easily leads to hard fail or poor cell characteristics and reliabilities. New phase change materials (N-PCMs) are developed to have a large Vt window and a uniform Vt distribution for a sufficient read window margin (RWM) and a corresponding low raw bit error rate (RBER). New chalcogenide selectors (NCSs) are also developed to provide low Vt instability and very low leakage current. The new CPM is able to provide a sufficient RWM for 16 Mb MATs with very low latencies of write (set $\leq$ 300 ns) and read ($\leq$ 100 ns). We also demonstrate its decent write disturbance and high reliabilities such as endurance and thermal retention.

2:00 PM - 2:25 PM
37.2 A Highly Efficient and Scalable Model for Crossbar Arrays with Nonlinear Selectors, *A. Chen, IBM Reseach Division*

A scalable crossbar array model is proposed to solve arrays with various sizes and device characteristics. Computation is accelerated over 1000X by array reduction, enabling array scaling analysis and extensive design space exploration. Computation error can be reduced by extrapolation from calculations with different array reduction ratios. The impact of selectors on array performance is analyzed with this model, which can be applied to nonlinear, threshold switch, and rectifying selectors.

2:25 PM - 2:50 PM
37.3 Ultra-High Endurance and Low I_{OFF} Selector based on AsSeGe Chalcogenides for Wide Memory Window 3D Stackable Crosspoint Memory, *H. Y. Cheng, W. C. Chien, I. T. Kuo, C. W. Yeh, L. Gignac*, W. Kim*, E. K. Lai, Y. F. Lin, R. L. Bruce*, C. Lavoie*, C. W. Cheng*, A. Ray*, F. M. Lee, F. Carta*, C. H. Yang, M. H. Lee, H. Y. Ho, M. BrightSky* and H. L. Lung, IBM/Macronix PCRAM Joint Project, Macronix International Co., Ltd., *IBM T. J. Watson Research Center*

New selector materials with very-low IOFF and optimum Vth based on As-Se-Ge chalcogenides are studied. An optimized composition is proposed, which achieves a good trade-off between thermal stability and cycling endurance and it is successfully integrated with PCM in a 3D stackable pillar structure. SET/RESET operation are demonstrated with ~2V memory window. Selector is able to deliver 1mA ON current (7.9 MA/cm2) and fast speed (10 ns). More than 1E12 read cycling endurance is achieved in 1S1R (OTS+PCM) device due to the excellent endurance of the selector.

2:50 PM - 3:15 PM
37.4 Optimized Reading Window for Crossbar Arrays Thanks to Ge-Se-Sb-N-based OTS Selectors, *A. Verdy, M. Bernard, J. Garrione, G. Bourgeois, M. C. Cyrille, E. Nolot, N. Castellani, P. Noé, C. Socquet-Clerc, T. Magis, G. Sassine, G. Molas, G. Navarro and E. Nowak, CEA, LETI*

In this paper, we investigate the impact of Ovonic Threshold Switching (OTS) selector electrical parameters, such as the threshold and the holding current, on the reliability of the reading operation in 1S1R memory devices. Through physico chemical analysis and electrical characterization of Se rich Ge Se based OTS selectors, performed up to 400 °C, we demonstrate the possibility to reduce the fire voltage as well the leakage current thanks to N and Sb doping. Moreover, we describe the correlation that exists between the leakage current and the threshold current in OTS devices. We highlight the subsequent trade off between

the reading window and the array size in an OTS-based Memory Crossbar Array, evaluated up to an operating temperature of 150 °C. Finally, thanks to OTS engineering, we demonstrate how the reading window can be optimized for a target array size and application.

3:15 PM - 3:40 PM

37.5 Forming-free Mott-oxide threshold selector nanodevice showing s-type NDR with high endurance (> 10^{12} cycles), excellent V_{th} stability (< 5%), fast (< 10 ns) switching, and promising scaling properties, *T. Hennen, D. Bedau*, J. A. J. Rupp, C. Funck, S. Menzel**, M. Grobis*, R. Waser, and D. J. Wouters, RWTH Aachen University, *Western Digital San Jose Research Center, **Forschungszentrum Jülich GmbH*

Thin film (10 nm) $(V_{1-x}Cr_x)_2O_3$ Mott-oxide based nano-devices show volatile threshold switching. Fast (< 10 ns) and very stable (< 5% variation, > 10^12 cycles) switching is obtained. Thickness and area dependence of the NDR curves are consistent with uniform volume switching and are explained with a thermal feedback model.

Session 38: Optoelectronics, Displays, and Imagers - Displays, TFTs, and Optical Synapses

Wednesday, December 5, 1:30 PM

Continental Ballroom 5

Co-Chairs: B. Peterson, University of Michigan

L. Zhou, BOE Technology Group., Ltd.

1:35 PM - 2:00 PM

38.1 Fully Multi-Functional GaN-based Micro-LEDs for 2500 PPI Micro-displays, Temperature Sensing, Light Energy Harvesting, and Light Detection, *Z. Liu, K. Zhang, Y. Liu, S. Yan, H. S. Kwok, J. Deen, and X. Sun, Southern University of Science and Technology*

GaN-based Micro-LEDs were developed for more than a decade and are considered as the next generation of display technology. Micro-LEDs have more versatile functions than displays. We report fully multi-functional Micro-LEDs for micro-displays, temperature sensing, light energy harvesting, and light detection. The 2500 pixel per inch (PPI) Micro-LED devices displayed animations and pictures in display mode driven by a Si complementary metal-oxide-semiconductor (CMOS) backplane. In temperature sensing mode, it showed a sufficient linearity with a resolution of 795 K/V. It also had a fill factor of 65.9% and efficiency of 15.5% in light energy harvesting mode and a sensitivity of 1240 and external quantum efficiency (EQE) of 33% in light detection mode. Results real that the proposed devices can be used as a self-sustainable micro-system for low cost and eco-friendly applications.

2:00 PM - 2:25 PM

38.2 Environmentally Friendly Quantum Dots for Display Applications (Invited), *E. Jang, SAIT, Samsung Electronics*

Ever since the physics of quantum dot (QD) was discovered, much research effort has been carried out for more than 30 years, and lots of applications adopting QDs have been proposed. Especially, wide color gamut displays using QDs as active light emitting materials have drawn much attention. And, the QD-based consumer displays such as LED TVs, tablets, and special monitors are now on the market. They provide best color gamut, reasonable power efficiency, and affordable price showing superior competitive edge to OLED technology. However, still there are issues and argues using Cadmium containing materials in practical consumer devices. In spite of the European RoHS Exemptions, we need to be aware the environmental risk of producing large quantity of Cd-containing materials and using them in the consumer electronics. And, this growing apprehension for environmental issues formed great limitation for QD's applications. Therefore, we have dedicated to develop more environmentally friendly InP based QDs that

showed considerably high efficiency and saturated color spectrum compared to the Cd-containing materials. The structure of Cd-free QD was specially tailored for display applications and the synthetic process was optimized to produce reliable materials in commercial scales. In order to improve the efficiency and stability of the QDs in the devices operating under severe atmosphere, specific composite materials were designed and the fabrication process was optimized. From 2015, Samsung has released Cd-free QD adopted UHD TV for major product line-up which show the best color gamut among the current displays. Now we are trying to make additional breakthroughs in displays by using established QD material platform and broaden the technology to wider optoelectronic applications.

2:25 PM - 2:50 PM
38.3 Solution Processed High Performance Short Channel Organic Thin-Film Transistors with Excellent Uniformity and Ultra-low Contact Resistance for Logic and Display, *L. Feng, Y. Huang*, J. Fan*, J. Zhao*, S. Pandya**, S. Chen8, W. Tang*, S. Ogier, and X. Guo*, Wuhan Xinqu Chuangrou Optoelectronics Technology Co., Ltd, *Shanghai Jiao Tong University, **NeuDrive Limited*

High performance organic thin-film transistors (OTFTs) are fabricated by using normal spin-coating processes with the highest processing temperature of 115 ℃. The devices present negligible contact resistance and excellent uniformity over 4 inch area. An average mobility higher than 4 cm2/V.s is achieved with 7 μm channel length devices. Ring oscillators and AMOLED displays based on the OTFTs are demonstrated. A dual gate structure is implemented to tune the threshold voltage of the OTFTs for improving the compensation and gray-level adjusting capability of an AMOLED in-pixel compensation circuit.

2:50 PM - 3:15 PM
38.4 Record Static and Dynamic Performance of Flexible Organic Thin-Film Transistors, *J. W. Borchert, U. Zschieschang, F. Letzkus**, M. Giorgio***, M. Caironi***, J. N. Burghartz**, S. Ludwigs* and H. Klauk, Max Planck Institute for Solid State Research, *Functional Polymers, Institute of Polymer Chemistry, Universität Stuttgart, **Institut für Mikroelektronik Stuttgart (IMS CHIPS), ***Center for Nano Science and Technology @PoliMi, Instituto Italiano di Tecnologia (IIT)*

Organic transistors with record static and dynamic performance on flexible substrates are presented. They operate with 3 V and have channel lengths down to 0.6 μm, on/off ratios of 1E10, subthreshold slopes of 59 mV/decade and ring-oscillator delays of 79 ns. These results are enabled by a record-low contact resistance.

3:15 PM - 3:40 PM
38.5 Hybrid Structure of Silicon Nanocrystals and 2D WSe_2 for Broadband Optoelectronic Synaptic Devices, *Z. Ni, Y. Wang, L. Liu, S. Zhao, Y. Xu, X. Pi, and D. Yang, Zhejiang University*

Optoelectronic synaptic devices based on the hybrid structure of silicon nanocrystals (Si NCs) and 2D WSe2 are fabricated. The Si-NC/WSe2 synaptic devices can be optically stimulated in a broad spectral region from the ultraviolet to near-infrared. The energy consumption of the devices may be as low as ~75 fJ.

3:40 PM - 4:05 PM
38.6 High Performance 2D Perovskite/Graphene Optical Synapses as Artificial Eyes, *H. Tian, X. Wang, F. Wu, Y. Yang, T.-L. Ren, Tsinghua University*

Conventional von Neumann architectures feature large power consumptions due to memory wall. Partial distributed architecture using synapses and neurons can reduce the power. However, there is still data bus between image sensor and synapses/neurons, which indicates plenty room to further lower the power

consumptions. Here, a novel concept of all distributed architecture using optical synapse has been proposed. An ultrasensitive artificial optical synapse based on a graphene/2D perovskite heterostructure shows very high photo-responsivity up to 730 A/W and high stability up to 74 days. Moreover, our optical synapses has unique reconfigurable light-evoked excitatory/inhibitory functions, which is the key to enable image recognition. The demonstration of an optical synapse array for direct pattern recognition shows an accuracy as high as 80%. Our results shed light on new types of neuromorphic vision applications, such as artificial eyes.

Session 39: Compound Semiconductor and High Speed Devices - High Performance III-V Devices and Technology Towards 5G
Wednesday, December 5, 1:30 PM
Continental Ballroom 6
Co-Chairs: E. Lind, Lund University
Y. Sun, IBM

1:35 PM - 2:00 PM
39.1 First Transistor Demonstration of Thermal Atomic Layer Etching: InGaAs FinFETs with sub-5 nm Fin-width Featuring *in-situ* ALE-ALD, *W. Lu, Y. Lee*, J. Murdzek*, J. Gertsch*, A. Vardi, L. Kong, S. M. George*, and J. A. del Alamo, Massachusetts Institute of Technology, *University of Colorado*

For the first time, thermal atomic layer etching (ALE) on InGaAs-based III-V heterostructures is demonstrated. Also, we report the first transistors fabricated by the thermal ALE technique in any semiconductor system. We further highlight one unique advantage of thermal ALE: its integration with atomic layer deposition in a single vacuum chamber. Using in-situ ALE-ALD, we have fabricated the most aggressively scaled self-aligned In0.53Ga0.47As n-channel FinFETs to date, featuring sub-5 nm fin widths. The narrowest FinFET with Wf = 2.5 nm and Lg = 60 nm shows gm = 0.85 mS/um at Vds = 0.5 V. Devices with Wf = 18 nm and Lg = 60 nm demonstrate gm = 1.9 mS/um at Vds = 0.5 V. Subthreshold swings averaging Slin = 70 mV/dec and Ssat = 74 mV/dec across the entire range of Wf, at minimum Lg = 60 nm have been obtained. These are all record results. The transistors demonstrated here show an average 60% gm improvement over devices fabricated through conventional techniques. These results suggest a very high-quality MOS interface obtained by in-situ ALE-ALD.

2:00 PM - 2:25 PM
39.2 InGaAs-on-Insulator FinFETs with Reduced Off-Current and Record Performance, *C. Convertino, C. Zota, S. Sant*, F. Eltes, M. Sousa, D. Caimi, A. Schenk* and L. Czornomaz, IBM Research Zurich, *Integrated Systems Laboratory, ETH Zurich*

In this work, we demonstrate InGaAs-on-Insulator FinFETs on silicon with optimized on/off trade-off showing record performance. This is achieved by using carefully designed source/drain spacers and spacers extensions to mitigate the off-current, typically high in narrow band-gap materials, as part of a CMOS compatible replacement-metal-gate process flow. Using this technology, devices with LG = 20 nm, spacers width of 10 nm and Wfin = 15 nm achieve record high on-current of 350 µA/µm (IOFF = 100nA/µm and VDD = 0.5 V), for scaled III-V FETs on Si, enabled by an access resistance of 220 Ω µm, SSsat = 78 mV/decade and a gm = 1.5 mS/µm. We analyze the impact of spacers thickness, WFIN and LG on device performance. 2D TCAD simulations provide further insights into device functionality and about the dominant off-state leakage mechanisms.

2:25 PM - 2:50 PM
39.3 Balanced Drive Currents in 10-20 nm Diameter Nanowire All-III-V CMOS on Si, *A. Jönsson, J. Svensson, and L.-E. Wernersson, Lund University*

We use a self-aligned, gate-last process providing n-type (InAs) and p-type (GaSb) MOSFET co-integration with a common gate-stack and demonstrate balanced drive current capability at about 100 µA/µm. By utilizing HSQ-spacers, control of gate-alignment allows to fabricate both n- and p-type devices based on the same type of vertical heterostructure InAs/GaSb nanowire with short gate-lengths down to 60 nm. Refined digital etch techniques, compatible with both sensitive antimonide structures and InAs, enable down to 16 nm diameter GaSb channel regions and 10 nm InAs channels. Balanced performance is showcased for both n- and p-type MOSFETs with Ion = 156 µA/µm, at Ioff = 100 nA/µm, and 98 µA/µm, at |VDS| = 0.5, respectively.

2:50 PM - 3:15 PM

39.4 High Performance Quantum Well InGaAs-On-Si MOSFETs With sub-20 nm Gate Length For RF Applications, *C. B. Zota, C. Convertino, Y. Baumgartner, M. Sousa, D. Caimi and L. Czornomaz, IBM Research GmbH Zürich Laboratory*

We demonstrate RF-compatible quantum well InGaAs MOSFETs integrated on Si substrates, with LG down to 14 nm and a Si CMOS compatible RMG fabrication flow. Devices exhibit simultaneously extrapolated ft and fmax of 370 and 310 GHz, respectively, the highest reported combined ft/fmax for III-V MOSFETs on Si.

3:15 PM - 3:40 PM

39.5 High Performance InGaAs Gate-All-Around Nanosheet FET on Si Using Template Assisted Selective Epitaxy, *S. Lee, C. -W. Cheng, X. Sun, C. D'Emic, H. Miyazoe, M. M. Frank, M. Lofaro, J. Bruley, P. Hashemi, J. A. Ott, T. Ando, W. Spratt, G. M. Cohen, C. Lavoie, R. Bruce, J. Patel, H. Schmid*, L. Czornomaz*, V. Narayanan, R. T. Mo, and E. Leobandung, IBM T. J. Watson Research Center, *IBM Research GmbH Zürich Laboratory*

We report InGaAs gate-all-around nanosheet NFETs on Si substrate using template-assisted-selective-epitaxy (TASE) and a gate-last process with thermal budget advantages. Compared to our early report of the TASE process, in this paper we demonstrate that TASE can be scaled to a channel thickness of ~10 nm, which enables short gate devices without significant leakage. The defects and composition of the fabricated nanosheet FETs are also investigated. Enabled by this VLSI compatible process and a novel high-pressure deuterium annealing process, our 39 nm-Lg device shows a peak gm of 1.37 mS/um, a subthreshold slope in saturation of 72 mV/decade, and an Ion of 355 uA/um at 0.5 V Vgs, the highest among reported sub-50 nm-Lg III-V FETs on Si.

3:40 PM - 4:05 PM

39.6 Scaling Acoustic Filters Towards 5G, *Y. Yang, R. Lu, and S. Gong, University of Illinois at Urbana Champaign*

This paper presents a micro-electro-mechanical system (MEMS) filter at 10.8 GHz as the first step of scaling electromechanical filters towards fifth-generation (5G) frequencies beyond 6 GHz. The scaling of the center frequency to 10. 8 GHz is made possible by resorting to a higher order asymmetrical lamb wave mode (A3) in lithium niobate ($LiNbO_3$) thin film. The filter is then designed as a ladder configuration of A3 resonator arrays to reduce insertion loss and attain a low system impedance. The fabricated resonator has demonstrated an electromechanical coupling (kt2) of 3.6% and a quality factor (Q) of 337. The Q is among the highest reported for piezoelectric MEMS resonators operating at this frequency range. The

fabricated filter at 10.8 GHz has a 3 dB bandwidth of 70 MHz, a minimum insertion loss of 3.7 dB, an in-band ripple less than 0.1 dB, and a compact footprint of 0.7x0.5 mm2.

Session 40: Modeling and Simulation - Simulation and Modeling of Advanced Process and Emerging Memory
Wednesday, December 5, 1:30 PM
Continental Ballroom 7-9
Co-Chairs: S-D Kim, SK Hynix
J. Kang, Peking University

1:35 PM - 2:00 PM
40.1 Physics of hole trapping process in high-k gate stacks: A direct simulation formalism for the whole interface system combining density-functional theory and Marcus theory, *Y.-Y. Liu, X. Jiang, Chinese Academy of Sciences*

Charge trapping defects in high-κ dielectrics and at their interfaces are known to be a challenging obstacle for the silicon based modern transistors. To facilitate the solution of such problems, a deeply physical understanding of the charge trapping process at atomistic scale is mandatory. As such, we propose, for the first time, a direct method to calculate the exact hole trapping rates explicitly in the high-***k*** gate stack consisting of silicon channel, SiO2 interfacial layer and HfO2. The physics of multiple path (trap locations) hole trapping processes is revealed by combining density-functional theory and Marcus theory. The roles of physical quantities including defect reorganization, coupling constant and Gibbs free energy are discussed. It is suggested that oxygen vacancies at high-***k*** interface with interfacial layer SiO2 are dominant hole traps under NBTI stress. The developments and findings provide not only a deep physical insight into the hole trapping related reliability degradation mechanism, but also a new simulation framework.

2:00 PM - 2:25 PM
40.2 Parasitic Surface Reactions in High-Aspect Ratio Via Filling using ALD: A Stochastic Kinetic Model, *T. Muneshwar, G. Shoute, D. Barlage*, and K. Cadien*, Synthergy Inc., *University of Alberta*

A scalable kinetic Monte-Carlo model (sKMC) of molecular transport for atomic layer deposition (ALD) for high aspect-ratio (AR) features is developed. Surface coverage is a critical parameter studied here in detail. The capabilities of the stochastic model provide insight into challenges in growing ALD films in high-AR via structures faced by the industry, including the effects of parasitic surface reactions resulting in poor coverage. Furthermore, we provide experimental results verifying the model's prediction by growing ALD SiNx on high-AR via structures. By compensating for the processing errors corroborated by the model, we experimentally improved sidewall coverage from 70% to 92%.

2:25 PM - 2:50 PM
40.3 Physics-based modeling of volatile resistive switching memory (RRAM) for crosspoint selector and neuromorphic computing, *W. Wang, A. Bricalli, M. Laudato, E. Ambrosi, E. Covi, and D. Ielmini, Politecnico di Milano*

Volatile resistive switching memory (RRAM) is raising strong interest as potential selector device in crosspoint memory and short-term synapse in neuromorphic computing. To enable the design and simulation of memory and computing circuits with volatile RRAM, compact models are essential. To fill this gap, we present here a novel physics-based analytical model for volatile RRAM based on a detailed study of the switching process by molecular dynamics (MD) and finite-difference method (FDM). The analytical model captures all essential phenomena of volatile RRAM, e.g., threshold/holding voltages, on-off ratio, and size-dependent retention. The model is validated by extensive comparison with data from

Ag/SiOx RRAM. To support the circuit-level capability of the model, we show simulations of crosspoint arrays and neuromorphic time-correlated learning.

2:50 PM - 3:15 PM

40.4 Analytic Model for Statistical State Instability and Retention Behaviors of Filamentary Analog RRAM Array and Its Applications in Design of Neural Network, *P. Huang, Y. C. Xiang, Y. D. Zhao, C. Liu, B. Gao*, H. Q. Wu*, H. Qian*, X. Y. Liu, J. F. Kang, Peking University, *Tsinghua University*

For the first time, an analytic model is presented for the statistical state instability and retention behaviors of filamentary analog resistive random access memory (RRAM) array. In the model, the diffusion of oxygen vacancy (VO), the Brownian-like hopping of VO during the diffusion process and the recombination of VO are considered. The statistical state instability and retention behaviors of different states under various temperatures are accurately described by the model, which is verified by the measured data of 1Kb filamentary analog RRAM (FA-RRAM) array. Furthermore, the analytic model is successfully implemented to evaluate and optimize the reliability of FA-RRAM based multi-layer neural network. Guided by the model, optimized synapse structures and refresh operation are proposed to significantly enhance the reliability of FA-RRAM based neural network.

3:15 PM - 3:40 PM

40.5 Evidence of Magnetostrictive Effects on STT-MRAM Performance by Atomistic and Spin Modeling, *K. Sankaran, J. Swerts, R. Carpenter, S. Couet, K. Garello, R. F. L. Evans*, S. Rao, W. Kim, S. Kundu, D. Crotti, G. S. Kar, and G. Pourtois, imec, *University of York*

We demonstrate, using an atomistic description of a 30nm diameter spin-transfer-torque magnetic random access memories (STT-MRAM), that the difference in mechanical properties of its sub-nanometer layers induces a high compressive strain in the magnetic tunnel junction (MTJ) and leads to a detrimental magnetostrictive effect. Our model explains the issues met in engineering the electrical and magnetic performances in scaled STT-MRAM devices. The resulting high compressive strain built in the stack, particularly in the MgO tunnel barrier, and its associated non-uniform atomic displacements, impacts on the quality of the MTJ interface and leads to strain relieve mechanisms such as surface roughness and adhesion issues. We illustrate that the strain gradient induced by the different materials and their thicknesses in the stacks has a negative impact on the tunnel magneto-resistance, on the magnetic nucleation process and on the STT-MRAM performance.

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