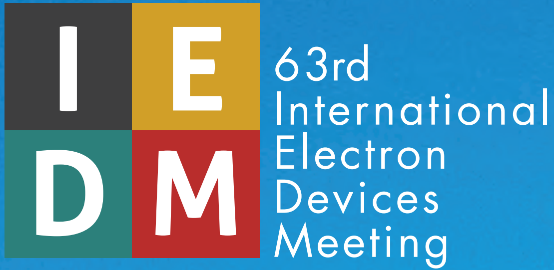

2017 IEDM Conference Proceedings

For More Information
IEDM Online: ieee-iedm.org

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Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

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- Wikipedia: https://en.wikipedia.org/wiki/International_Electron_Devices_Meeting

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Topics of Interest

CIRCUIT AND DEVICE INTERACTION (CDI)

Papers are solicited in the areas of CMOS platform technology, circuit design challenges in emerging technologies, and device technology interactions. Platform technologies include III-Vs, SiGe/Ge, and other underlying technologies for the "next node" (N+1). Topics also include digital and analog device and circuit performance and scaling issues, technology-design co-optimization, power-performance-area analysis, the impact of future device structures on circuit design, circuit and architectural implications of interconnect technology and performance, manufacturability issues such as design for manufacturability and process control, and emerging circuit design and technology concepts, including neuromorphic and non-von Neumann circuit approaches. Submission of papers discussing interactions between advanced device technology and design issues such as variability, power constraints, physical layout effects and design complexity in memory, logic, analog, and mixed-signal circuits is encouraged.

CHARACTERIZATION, RELIABILITY and YIELD (CRY)

Papers are solicited in all areas of characterization, yield, and reliability, at both the front-end and back-end of the process. Topics include hot carriers, dielectric wear-out and breakdown, process charging damage, latch-up, ESD, soft errors, noise and mismatch behavior, variability/reliability interaction and time dependent variability, bias temperature instabilities, and thermal modeling at the device, circuit, and packaging level for memory, logic, analog, and novel device technologies. Other topics include interconnect reliability, electromigration, the impact of back-end processing on devices, chip- package interaction, physics of failure analysis, and novel characterization techniques.

Compound Semiconductor and High Speed Devices (CHS)

Papers are solicited in the areas of compound semiconductor electronic devices and high-speed device technologies based on GaAs, InGaAs, InP, GaN, SiGe, Antimonides and their related alloys. Devices of interest include III-V MOS devices, ballistic devices, HBTs (III-V and group IV) and HEMTs, RF/microwave/millimeter-wave devices, SAW/BAW devices, and active and passive electron devices for analog applications. Topics include device physics, design, modeling, reliability and manufacturing processes.

MEMORY TECHNOLOGY (MT)

Papers are solicited covering all memory related technology topics, including devices for neuromorphic computing applications. Topics span the full range from novel cell concepts to fully integrated memories and manufacturing issues. Areas of interest include cell design and scaling, processing, reliability, and modeling for both volatile and nonvolatile memories, as well as conventional and novel memory cells including ReRAM, STT-MRAM, PCRAM, FeRAM, crosspoint and selectors, organic memory and NEMS-based devices. Devices and physics of memristors and other device concepts that support neural computing paradigms are also of interest. Higher level topics include array optimization, 3D architectures, novel read/program/erase schemes, solid state drive (SSD) applications, novel hierarchies and architectures for memory-centric systems, security, computing-in-memory and disruptive non-volatile memory-enabled emerging logic applications.

MODELING and SIMULATION (MS)

Papers are solicited in the areas of analytical, numerical, and statistical approaches to modeling electronic, optical, and hybrid devices (including sensors), and their isolation and interconnection. Topics include physical and compact models for devices and interconnects, modeling of fabrication processes and equipment, material modeling, process characterization, parameter extraction, early compact models for advanced technologies and novel devices, performance evaluation, design for manufacturing, reliability, variability, and technology benchmarking methodologies. Other topics of interest include the modeling of interactions between process, device, circuit, and packaging technology. Submissions should advance the art of modeling and simulation or apply existing techniques to gain new insights into devices.

NANO DEVICE TECHNOLOGY (NDT)

Papers are solicited on novel solid state and nanoelectronic devices and concepts. This includes devices based on novel transport mechanisms such as tunnel FETs and other steep-slope devices, molecular devices, and emerging concepts for devices based on topological insulators, phase transitions, quantum effects, and non-von Neumann devices. Non-charge based logic, magnetic logic, spintronics, plasmonics and quantum computing are also of interest. Furthermore, nanoelectronic devices based on low-dimensional systems are encouraged, including 2D materials, nanowires, nanotubes and quantum dots. Subsets of key topics include electron device physics, technology scaling issues, as well as novel transistor structures. Papers in NDT focus primarily on device physics and novel concepts; more mature "platform candidate" papers should be submitted to CDI.

OPTOELECTRONICS, DISPLAYS, and IMAGERS (ODI)

Papers are solicited on devices, structures, and integration for optoelectronics, photonics, displays, and imaging systems. Optoelectronic devices include photovoltaics, photonic bandgap structures and crystals, LEDs and lasers, as well as optoelectronic and photonic integrated circuits and optical interconnects. Papers on quantum photonics and photonic qubits for quantum computation are also of interest. Displays and imaging area topics include CMOS imagers, high-speed imagers, CCDs, TFTs, organic, amorphous, and polycrystalline devices, as well as emissive and reflective displays. Submission of papers addressing flexible and/or stretchable electronics, printed electronics, stacked image sensors with Si or other photosensitive materials, organic and inorganic displays, and covering new technology trends in imagers and displays are encouraged. Other relevant subjects include device/circuit design, fabrication, reliability, theory, and modeling.

POWER DEVICES (PD)

Papers are solicited on discrete and integrated power devices and modules using Si, diamond, and compound semiconductors. Papers exploring the system-level impact of power devices are also of interest. Topics of interest include power devices (FETs, superjunction devices, IGBTs, etc.), and materials (Si, SiC, GaN, Diamond, GaAs, AlN, Ga2O3, etc.), manufacturing processes, device design, modeling, physics, and reliability. Devices targeting the full range of power and power conversion applications, including hybrid vehicles, power supplies for computer and telecom, motor drives, utility and grid control, and wireless power transfer, are of interest.

PROCESS and MANUFACTURING TECHNOLOGY (PMT)

Papers are requested on innovations in individual process modules, process integration schemes, and process control techniques that enable improved device or circuit performance or enable new functionality. Examples of front-end process topics include substrate and isolation technologies, new transistor materials, integration of heterogeneous channel materials, multi-patterning and EUV lithography, self-assembly techniques, deposition and etch techniques, novel dielectrics and metal electrodes for transistor gate stacks and MIM capacitors, shallow junctions, and silicides. Examples of back-end process topics include conductor systems, low dielectric constant materials, contact and via processes, barrier materials, planarization, integration considerations for multi-level interconnects, photonics-electronics integration on CMOS, and advanced packaging. Also of interest are topics like emerging process modules, 3D integration, additive manufacturing for microelectronics, processes and tools designed to reduce variance, defect reduction in heterogeneous material systems, novel techniques for enhancing process control and stability.

SENSORS, MEMS, and BioMEMS (SMB)

Papers are solicited in the area of sensors, sensor networks, micro electromechanical systems (MEMS), BioMEMS, microfluidic as well as NEMS devices. The sensors area includes TFT-based sensors and sensors for chemical, molecular, and biological detection including electrochemical, mechanical and optical sensors. Topics of interest in the MEMS and BioMEMS area include resonators and resonant sensors, RF MEMS, integrated inertial measurement units, integrated biomedical sensing, integrated sensors and actuators, micro-optical devices, microfluidic and bio-electronic devices inspired or enabled by biomimetic structures, micro power generators, mechanical energy harvesting devices, opto-fluidic devices, and organic-inorganic hybrid-devices, with particular emphasis on new device concepts, integrated implementations, wearables, and complete sensor systems and networks.

Program

See the Program Download for all abstracts and speaker bios.

Tutorials

The tutorials are in their seventh year and are 90 minute stand alone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields, and facilitate understanding of the technical sessions. In contrast, the traditional short courses are intensive full-day events focused on a single technical topic.

The tutorial sessions will take place on Saturday, December 2nd. Three tutorials are given in parallel in two time slots, at 3:15 p.m. and 5:00 p.m. respectively.

Topics presented at 3:15 – 4:45 p.m:

- The Evolution of Logic Transistors toward Low Power and High Performance IoT Applications, Dae Won Ha, Samsung Electronics
- Hardware Opportunities in Cognitive Computing: Near- and Far-term, Geoffrey Burr, IBM Research-Almaden
- Silicon Photonics for Next-Generation Optical Interconnects, Joris Van Campenhout, IMEC

Topics presented at 5:00 p.m.-6:30 p.m:

- Negative Capacitance Transistors, Sayeef Salahuddin, University of California, Berkeley
- Fundamental, Thermal, and Energy Limits of PCM and ReRAM, Eric Pop, Stanford University
- 2.5D Interposers and High Density Fanout Packaging as Enablers for Future Systems Integration, Venkatesh Sundaram, Georgia Institute of Technology

Short Courses

IEDM will offer two, full-day short courses with in-depth coverage of logic and memory topics from world experts.

Short Course 1 – Boosting Performance, Ensuring Reliability, Managing Variation in sub-5nm CMOS

Course Organizer: Sandy Liao, Intel Corporation

Short Course 2 – Memories for the Future: Devices, Technologies, and Architecture

Organizer: Kevin Zhang, Vice President, Design and Technology Platform, TSMC

Plenary Session

Welcome and Awards

IEDM General Chair Stefan De Gendt, imec

Plenary Papers

IEDM Technical Program Chair Ken Rim, Qualcomm

- Multi-Chip Technologies to Unleash Computing Performance Gains over the Next Decade, Lisa Su, AMD
- Energy efficient computing and sensing in the Zettabyte era: from silicon to the cloud, Adrian Ionescu, EPFL
- System Scaling Innovation for Intelligent Ubiquitous Computing, Jack Sun, TSMC

Wednesday, December 6

Plenary Paper

- Development of Sustainable Smart Society based on Transformative Electronics, Hiroshi Amano, Nagoya University Nobel Prize, Physics 2014

IEDM Awards

2016 Roger A. Haken Best Student Paper Award To: Roman Koerner, University of Stuttgart/Philips U-L-M Photonics For the paper entitled: "The Zener-Emitter: A Novel Superluminescent Ge Optical Waveguide-Amplifier with 4.7 dB Gain at 92 mA Based on Free-Carrier Modulation by Direct Zener Tunneling Monolithically Integrated on Si"

IEEE EDS Awards

EDS Paul Rappaport Award To: Takatoshi Tsujimura, Takeshi Hakii, and Suguru Noda For the paper entitled: "A Color-Tunable Polychromatic Organic-Light-Emitting-Diode Device With Low Resistive Intermediate Electrode for Rollto-Roll Manufacturing"

EDS George E. Smith Award To: Rongming Chu, Yu Cao, Mary Chen, Ray Li, and Daniel Zehnder For the paper entitled: "An Experimental Demonstration of GaN CMOS Technology"

2017 EDS Education Award To: Mansun Chan "For pioneering innovative approaches in electronic engineering education"

2017 EDS J.J. Ebers Award To: Kang L. Wang "For contributions and leadership in strained SiGe and magnetic memory technologies"

2017 Distinguished Service Award To: Paul Yu "To recognize and honor outstanding service to the Electron Devices Society"

EDS Celebrated Members To: Gordon Moore and Simon Sze "For fundamental contributions to the field of electron devices for the benefit of humanity"

2017 IEEE/EDS Fellows

*This is a complete listing of the 2017 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2017 IEDM.

- Hugh Barnaby, Arizona State University, Tempe, Arizona, USA
- Yu Cao, Arizona State University, Tempe, Arizona, USA
- Edoardo Charbon, Delft University of Technology, Delft, Netherlands
- Wei-ting Chien, SMIC-Semiconductor Mfg. Int'l Corp., Shanghai, China
- Terry Ericsen, Ericsen Innovations LLC, Annapolis, Maryland, USA
- Christopher Hierold, Swiss Federal Institute of Technology, Zurich, Switzerland
- Ru Huang, Peking University, Beijing, China
- Tian-wei Huang, National Taiwan University, Taipei, Taiwan
- Chia-hong Jan, Intel Corporation, Portland, Oregon, USA
- Quanxi Jia, University of Buffalo, Buffalo, New York, USA
- Hongrui Jiang, University of Wisconsin, Madison, Wisconsin, USA
- Richard King, Arizona State University, Tempe, Arizona, USA
- Hulya Kirkici, Auburn University, Auburn, Alabama, USA
- Steven Koester, University of Minnesota, Minneapolis, Minnesota, USA
- Xiuling Li, University of Illinois, Champaign, Illinois, USA
- Donald Lie, Texas Tech University, Lubbock, Texas, USA
- Theresa Mayer, Virginia Tech, Blacksburg, Virginia, USA
- Junichi Nakamura, Brillnics Japan Inc., Tokyo, Japan
- Borivoje Nikolic, University of California, Berkeley, California, USA
- Akihiro Nitayama, Tohoku University, Sendai, Japan
- Tomas Palacios, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA
- Dimitrios Peroulis, Purdue University, West Lafayette, Indiana, USA
- Ramgopal Raovalipe, Indian Institute of Technology, Powai, Mumbai, India
- Akira Toriumi (2016), University of Tokyo, Japan
- Andrei Vladimirescu, Berkeley Wireless Research Center, Berkeley, California, USA
- Sorin Voinigescu, University of Toronto, Toronto, Ontario, Canada
- Xin Zhang, Boston University, Boston, Massuchusetts, USA

Focus Sessions

IEDM 2017 features four Special Focus Sessions with invited talks from world experts to highlight the latest developments in emerging sectors of semiconductor technology:

3D-Integration and Packaging (Session 3)

An industry perspective of packages to come: "Simpler is better" to "Advanced Packaging saves the day for continued scaling". The session will address the latest in 3D, from alternative packaging to 3D stacking, applications and technologies for Integrated Power Microelectronics.

- "3D sequential integration: Application driven technological achievements and guidelines," by Perrine Batude et al, CEA LETI
- "Pixel/DRAM/Logic 3-layer Stacked CMOS image sensor technology," by Hidenobu Tsugawa et al, Sony Semiconductor Solutions Corp.
- "Power Inside – Applications and Technologies for Integrated Power in Microelectronics," Cian O'Mathuna, University of Cork
- "3D System Package architecture as alternative to 3D Stacking of Ics with TSV at System level," by Rao Tummala, Georgia Institute of Technology
- "Advanced Packaging Saves the Day! – How TSV Technology Will Enable Continued Scaling," by Luke England et al, Global Foundries.
- "Advanced Packaging with greater simplicity," by Douglas Yu, TSMC
- "Towards Cube-Sized Compute Nodes: Advanced Packaging Concepts enabling Extreme 3D Integration," by Thomas Brunschwiler et al, IBM Research, Zurich.

Nanosensors for disease diagnostics (Session 10)

This session reviews the latest advances from microfluidics down to nanosensing for the detection of diseases such as cancer, sepsis and diabetes, using biomarkers ranging from (bio)molecules and individual cells up to in vitro tissue models.

- "Nanofluidics for cell and drug delivery," by Mauro Ferrari et al, Houston-Methodist Research Institute.
- "Rapid Antibiotic Susceptibility Testing System: Life Saving BioMEMS devices," by Sunghoon Kwon et al , Quantamatrix and celemics.
- "Development of high frequency Bulk Accoustic Wave resonators as Biosensors and Bioactuators," by Xuexin Duan et al, Tianjin University.
- "Encapsulated organoids and organ-on-a-chip for cancer modelling," by Nathalie Picollet d'hahan et al, CEA-LETI
- "A Single Bacterium and Mammalian Cell Analysis by Ionic Current Measurements in a Microchannel," by Noritada Kaji et al, Nagoya University
- "Tissue Microenvironment and Cellular Imaging," by Karen Cheung et al, University of British Columbia
- "Microscale profiling of circulating tumour cells" Reza Mohamadi et al, University of Toronto.

Modelling Challenges for Neuromorphic Computing (Session 11)

An exciting session addressing opportunities and challenges of efficient synaptic processes from learning models to device-circuit implementations of neuromorphic architectures. Half the session will discuss learning models in stochastic processes with the other half devoted to opportunities and challenges in RRAM for deep neural networks and neuromorphic computing.

- "Stochastic synapses as resources for efficient deep learning machines," by Emre Neftci, University of California at Irvine.
- "Attractor networks and associative memories with STDP learning in RRAM synapses," by Elisabetha Chicca et al, University of Bielefeld
- "Energy use constrains brain information processing," by Renaud Jolivet et al, CERN, Switzerland.
- "Understanding the trade-offs of device, circuit and applications in RRAM based neuromorphic computing systems," by Hai Li et al, Duke University.
- "Device and Circuit optimization of RRAM for Neuromorphic Computing," by Huaqiang Wu et al, Tsinghua University.
- • "Challenges and opportunities toward online training acceleration using RRAM based hardware neural network,"

by Tuohung Hou et al, National Chiao Tung University.

- “Multiscale modeling of neuromorphic computing devices: from materials to device operations,” by Luca Larcher et al, Universita di Modena e Reggio-Emilia.

Silicon Photonics: Current status and perspectives (Session 34)

This session addresses the state-of-the-art in silicon photonics technology from high volume manufacturing, optical transceivers and interconnects to femto-joule per bit integrated nanophotonics for up-coming market applications in optical computing.

- “Developments in 300mm Silicon Photonics using traditional CMOS fabrication methods and materials,” by Charles Baudot et al, STMicroelectronics.
- “Reliable 50Gb/s Silicon Photonics Platform for Next-Generation Data Center Optical Interconnects,” by Philippe Absil et al, imec
- “Advanced Silicon Photonics Technology Platform Leveraging the Semiconductor Supply Chain,” by Peter De Dobbelaere, Luxtera
- “Femto-joule-per-bit integrated nanophotonics and challenge for optical computation,” by Masaya Notomi et al, NTT Corporation
- “Advanced devices and packaging of Si-photonics based optical transceiver for optical interconnection,” by K Kurata et al, Photonics Electronics Technology Research Association

MRAM Posters & Forum

Sponsored by the IEEE Magnetics Society

Two IEEE Magnetics Society events at IEDM 2017

With the rising interest of the microelectronics industry in STT-MRAM, it is very important to strengthen the relationship between the microelectronics and magnetism communities in order to accelerate the development of this new hybrid technology. For that, two special events related to MRAM technology are being organized around IEDM by the IEEE Magnetics Society.

1) A special poster session dedicated to MRAM on Tuesday from 2-5:30 pm, Yosemite Room

Various topics will be covered including MRAM materials, phenomena, technology, testing, hybrid CMOS/MTJ technology and circuits, spin-logic. A similar MRAM poster session took place at IEDM 2016 and was very successful with 33 posters presented and very active cross-disciplinary discussions. This session is technically organized by the IEEE Magnetics Society. It appears as a special MRAM poster session scheduled on Tuesday afternoon 5 December 2017 in the IEDM program (https://ieee-iedm.org/2017/program/). This event will be a great opportunity to bring together experts in magnetism and in microelectronics. This year, 35 posters were accepted for presentation. The list can be found on the IEEE Magnetics Society website (http://www.ieeemagnetics.org/).

Participants in this poster session need to register at IEDM as regular attendees. More information can be found at http://www.ieeemagnetics.org/

2) The 9th MRAM Global Innovation Forum (Hilton Union Square, Imperial Ballroom on the Ballroom level, 7 Dec 2017)

This is a one-day forum organized the day following IEDM (i.e on 7 December 2017, 8:45am – 5:30pm) in the same hotel as IEDM (Hilton Union Square, 333 O’Farrell St, San Francisco). The Forum will consist of 10 invited talks from leading experts and a panel discussion. The program is indicated below. Various MRAM related topics will be covered including STT-MRAM technology, memory and processor demonstrations, spin orbit torque MRAM, and the needs, challenges and potential of MRAM. The Forum was originally initiated by Samsung Semiconductor, and this forum marks the 9th edition of the series.

The Forum is entirely sponsored by Samsung Semiconductor. The registration to the Forum is free of charge, including free lunch. However the number of attendees is limited. To register to the Forum, send an email to sandra.ingrassia@cea.fr with first name, last name, contact email, affiliation. A confirmation email will be sent to you. The deadline for is 3rd November 2017.

Program committee: Bernard Dieny (chair, SPINTEC, France), Bruce Terris (Western Digital, USA), Kyung Jin Lee (Korea Univ., South Korea), Hideo Ohno (Tohoku Univ., Japan), Daniel Worledge (IBM, USA).

9th MRAM Global Innovation Forum 2017

Program:

8:45 -9:00: Welcome and introduction (Bernard Dieny)

Session 1: STT-MRAM Technology (Chair Daniel Worledge, IBM)

- 9:00-9:30 Luc Thomas (TDK/Headway) STT-MRAM for embedded memory applications from eNVM to Last Level Cache
- 9:30-10:00 Guohan Hu (IBM) Low-Current Spin Transfer Torque MRAM with Double MTJs
- 10:00-10-30 Cheng-Ming Lin (TSMC) MRAM Technology Solution for Embedded Memory Applications

Session 2: Memory demonstration and impact on processor performance (Chair: Bruce Terris, WD)

- 11:00 – 11:30 Seung Kang (Qualcomm) MRAM and Its Derivative Devices for Secure Semiconductor Systems in the Era of Internet-of-Things
- 11:30 – 12 : 00 Dave Eggleston (Global Foundries) eMRAM: The March to Manufacturing
- 12:00 – 12:30 Yong Kyu Lee (Samsung Foundry Business, Samsung Electronics Co.) Highly Manufacturable STT-MRAM Embedded Technology based on 28nm FDSOI RF-Logic Process

Session 3: SOT-MRAM and VCMA (chair: Kyung Jin Lee, Korea Univ.)

- 14:00 – 14:30 Sunshuke Fukami (Tohoku Univ.) Spin-orbit torque switching for ultralow-power VLSI and AI hardware
- 14:30 – 15:00 Hiroaki Yoda (Toshiba) Voltage-Control Spintronics Memory having potentials for high-density and high-speed applications

Session 4: The needs (Automotive, IoT and AI) and potential/challenges ahead of MRAM (chair: Bernard Dieny)

- 15:00 – 15:30 Tetsuo Endoh (Tohoku) Embedded Nonvolatile Memory with STT-MRAMs and its Application for Nonvolatile Brain-Inspired VLSIs
- 15:30 – 16:00 Thomas Jew (NXP) Embedding MRAM in Automotive and IoT Microcontroller Solutions

16: 30 -17:30 Panel discussion: PCRAM, ReRAM, MRAM: competing or complementary technologies?

- Moderator: Daniel Worledge (IBM)
- Panelists: Gabriele Navarro (CEA/LETI), Seung Kang (QUALCOMM), Thomas Jew (NXP), Tetsuo Endoh (Tohoku University), Chris Petti (Sandisk/WD)

Bernard DIENY and Bruce TERRIS, IEEE Magnetics Society

- 14:00 – 14:30 S. Fukami (Tohoku Univ.) Spin-orbit torque switching for ultralow-power VLSI and AI hardware
- 14:30 – 15:00 H.Yoda (Toshiba) Voltage-Control Spintronics Memory having potentials for high-density and high-speed applications

The needs (Automotive, IoT and AI) and potential/challenges ahead of MRAM

- 15:00 – 15:30 Tetsuo Endoh (Tohoku) Embedded Nonvolatile Memory with STT-MRAMs and its Application for Nonvolatile Brain-Inspired VLSIs
- 15:30 – 16:00 Thomas Jew (NXP) Embedding MRAM in Automotive and IoT Microcontroller Solutions

16: 30 -17:30 Panel discussion: PCRAM, ReRAM, MRAM: competing or complementary technologies?

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Bernard DIENY and Bruce TERRIS, IEEE Magnetics Society

Technical Program

See the Program Download for all abstracts and speaker bios.

Monday — 9:00 a.m. – Noon

- Session 1 — Plenary Session

Monday – 1:30pm – 5:00pm

- Session 2: Memory Technology — ReRAM and Selectors
- Session 3: Focus Session – Process and Manufacturing Technology — 3D Integration and Packaging
- Session 4: Modeling and Simulation — Modeling and Simulation of Advanced Non-volatile Memory
- Session 5: Nano Device Technology — 2D and Carbon Nanotube Devices
- Session 6: Circuit and Device Interaction — Devices and Circuits for Neuromorphic and Stochastic Computing
- Session 7: Characterization, Reliability and Yield — Reliability of Advanced Devices
- Session 8: Optoelectronics, Displays, and Imagers — Thin Film Transistors and Detectors
- Session 9: Power Devices — SiC and GaN Vertical Power Devices
- Session 10: Focus Session – Sensors, MEMS, and BioMEMS — Nanosensors for Disease Diagnostics

Monday 6:30 pm – 8:00 pm

- Grand Ballroom — RECEPTION

Tuesday – 9:00 am – 12:30 p.m.

- Session 11: Focus Session – Memory Technology — Modelling Challenges for Neuromorphic Computing
- Session 12: Circuit and Device Interaction — Circuit-Device Challenges in More Moore and More than Moore
- Session 13: Modeling and Simulation — Modeling and Simulation of Advanced CMOS Transistors
- Session 14: Process and Manufacturing Technology — Interconnect Patterning and Memory Integration
- Session 15: Nano Device Technology — Negative Capacitance and Other Steep-Slope Devices 1
- Session 16: Optoelectronics, Displays and Imagers — Image Sensors and Single-Photon Detectors
- Session 17: Compound Semiconductor and High Speed — 1D and 2D III-V Nanoscale MOSFETs
- Session 18: Sensors, MEMS, and BioMEMS — Bio and Chemical Sensors

Tuesday – 12:30 p.m.

- Continental 4 — Entrepreneurs Lunch at IEDM

Tuesday – 2:00 pm – 5:30 pm

- Session 19: Memory Technology — Charge Based Memories and Advanced Memories
- Session 20: Circuit and Device Interaction — Path-Forward for Advanced CMOS Scaling
- Session 21: Characterization, Reliability and Yield — Memory Reliability
- Session 22: Process and Manufacturing Technology — Advanced Metal Gate and Contact Technology
- Session 23: Nano Device Technology — Negative Capacitance and Other Steep-Slope Devices 2
- Session 24: Optoelectronics, Displays and Imagers — Silicon Technology Based Optoelectronics
- Session 25: Power and High-Speed Devices — Novel Device Concepts
- Session 26: Sensors, MEMS, and BioMEMS — Technologies for Neural Activity Monitoring and DNA Analysis

Tuesday – 8:00 pm – 10:00 pm

- Continental 1-5 — Session 27 – IEDM Evening Panel Session

Wednesday – 9:00 am – 12:00 pm

- Session 28: Memory Technology — In-Memory Computing
- Session 29: Circuit and Device Interaction — Advanced Platform Technologies
- Session 30: Plenary Session II
- Session 31: Modeling and Simulation — Simulations of Nano-devices
- Session 32: Process and Manufacturing Technology — 3D Integration
- Session 33: Power Devices — Development of GaN Power Devices Technologies

- Session 34: Focus Session – Optoelectronics, Displays and Imagers — Silicon Photonics

Wednesday – 1:30 pm – 4:05 pm

- Session 35: Modeling and Simulation — Progress in Modeling Methodology and Approaches
- Session 36: Nano Device Technology — Device Technologies for Disruptive Computing
- Session 37: Process and Manufacturing Technology — Advanced Transistor Technologies
- Session 38: Memory Technology — STT-MRAM
- Session 39: Characterization, Reliability and Yield — Advanced Reliability Characterization and Circuits
- Session 40: Sensors, MEMS, BioMEMS — MEMS for Internet-of-Things (IoT)

Evening Panel Discussion

The 2017 IEDM Panel will use a new format – "talk show style" – with Professor Phillip Wong (Stanford University) as the moderator.

Topic: Where will the next Intel be headquartered?

Dennard scaling has fulfilled its historic mission and traditional Moore's Law is coming to an end. Who will drive and lead innovation in the semiconductor industry in the coming decades? We have assembled a panel of experts and industry veterans to address this important question. Who – foundry, IDM, fabless, application developers (the FAMGA) – will drive newer generations of technologies? Are foundries and IDMs becoming the "Home Depot" of architects and application developers who will drive all the value propositions? Can fabless without a system product still survive? Will system houses reach down to invest and develop the chip technologies? Who – U.S., Europe, Japan, Korea, Taiwan, China – will become the dominant chip supplier? Can R&D investments by sovereign countries change the landscape? Will countries reap benefits by investing in R&D specifically within the country? Who – material scientists, device technologists, circuit designers, system architects, application developers – will be the source of technology innovations and advances? Which region – US, Europe, Japan, China, Taiwan, Korea – will present the most innovative papers at the IEDM in a decade? Who – logic companies, memory companies, analog companies – will be the next Intel? And where will that company do research, development, and manufacturing?

Entrepreneur's Luncheon

The Entrepreneurs Luncheon will be held on Tuesday, December 5th, 12:30 pm – 1:30 pm.

Jointly sponsored by IEDM and IEEE Women in Engineering, the Entrepreneurs Lunch will feature Courtney Gras, Executive Director for Launch League, a local nonprofit focused on developing a strong startup ecosystem in NE Ohio. The moderator will be Prof. Leda Lunardi from North Carolina State University.

Courtney is an engineer by training and an entrepreneur by nature. After leaving her job as a power systems engineer at NASA to work for her own startup company, she discovered a passion for building startup communities and helping technology-focused companies meet their goals.

Courtney co-founded the Akron-based clean energy startup, Design Flux Technologies as an undergraduate student studying Electrical Engineering at the University of Akron. While serving as Chief Operations Officer Courtney was named a "Forbes 30 Under 30" in 2016. She has also been names to the "Top 40 Under 40" in Cleantech by Midwest Energy News and one of Crain's "Twenty in their 20s". She also received the ComEd Female Founder Prize for 2015 through the Clean Energy Challenge.

After spending 7 years with Design Flux Technologies, Courtney decided to fully-commit her career to supporting startups and helping technology companies reach their goals for growth. She does this this through her work as Executive Director for Launch League and her work as a business development consultant for local technology companies.

Courtney loves sharing her stories of founding a cleantech company, especially with young entrepreneurs. She travels around the globe speaking on the topics of entrepreneurship, women in tech, and clean energy at venues such as TEDx Budapest, the Pioneers Festival, the IEEE WIE International Women's Leadership Conference.

Exhibits & Exhibit Events

IEDM 2017 will host an Exhibits area during the conference where you can learn more about the latest products and publications. This will be open in the Yosemite Ballroom during the conference from Monday 12:00 pm, through Wednesday 12:00 pm. Stop by any time during the exhibition open hours to browse the booths and enjoy complementary coffee. The Exhibition will be open to all IEDM attendees as well as qualified Exhibit Only participants.

Exhibition Opening Times

Monday: 12-4 Tuesday: 8-4 Wednesday: 8-12

Complementary coffee will be available in the exhibits area

Exhibitor Special Events Calendar – All events are on the Fourth Floor of the Hilton

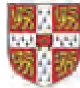
INFORMATION ON EXHIBITING IN 2017

2017 IEEE – IEDM exhibits will feature products, equipment and services directly related to the areas covered by the Conference. Information is available by writing to:

Scien-Tech Associates, Inc., P.O. Box 2097, Banner Elk, NC 28604-2097

Tel: 1-828-898-7001 Fax: 1-828-898-6379

Email: dbarbsta@aol.com



Appendix - Abstracts, Bios & Technical Program

WELCOME FROM THE GENERAL CHAIR

Stefan De Gendt
General Chair

Ken Rim
Technical
Program Chair

Mariko Takayanagi
Technical Program
Vice Chair

On behalf of the entire IEDM committee, I would like to welcome you to the 2017 IEEE International Electron Devices Meeting to be held December 2-6, 2017 2017 in San Francisco, CA. This will be the 63rd annual IEDM, and promises to continue the long tradition of being the world's premier venue for presenting the latest breakthroughs in electron device technologies.

This year's edition of IEDM will feature outstanding contributed and invited papers presented by industrial and academic leaders as well as students from around the world. An outline of the technical program and short summaries of all the papers are available on the IEDM web site, which we encourage everyone to visit – http://www.ieee-iedm.org/. We will continue to distribute an abbreviated digest at the meeting, along with the full digest in electronic format. An IEDM smartphone and tablet app that supports iPhone, iPad and Android platforms is also available. The full digest will also be available through IEEE Xplore after the conference.

The meeting's technical activities begin on Saturday afternoon, December 2, when we will continue to offer our highly successful tutorials. Now in their 7th year, these tutorials are targeted at students, engineers, or anyone who wants an introduction to, or review of, the basics of key charge and spin based devices technologies. Three tracks run in parallel, for a total of six tutorial topics; see the IEDM website for full information. On Sunday, two comprehensive short courses will be offered: "Boosting Performance, Ensuring Reliability, Managing Variation in sub-5nm CMOS", and "Memories for the Future: Devices, Technologies, and Architecture". These full-day courses are organized and presented by internationally recognized researchers from industry and academia active in these areas of technology. The topics and instructors have been carefully chosen to have broad appeal to IEDM participants, and will include material suitable for both newcomers as well as experts.

The Plenary Session on Monday morning will feature the EDS awards and three invited talks. Dr. Lisa Su from AMD will give us her perspectives in a talk entitled "Multi-Chip Technologies to Unleash Computing Performance Gains over the Next Decade," followed by Dr. Adrian Ionescu from EPFL who will describe efforts to go beyond current computing paradigms in his talk on "Energy efficient computing and sensing in the Zettabyte era: from silicon to the cloud." The third plenary talk, "System Scaling for Intelligent Ubiquitous Computing" will be given by Dr. Jack Sun from TSMC. Furthermore, IEDM 2017 will have the IEEE awards presented on Wednesday, followed by a plenary talk by 2014 Nobel Laureate, Hiroshi Amano, from Nagoya University on "Development of a Sustainable Smart Society based on Transformative Electronics".

In addition to the excellent contributed paper sessions, four special "Focus Sessions" will feature talks from leading experts in exciting new and rapidly-advancing areas. The topics of the focus sessions this year include Modelling Challenges for Neuromorphic Computing, Silicon Photonics: Current status and perspectives, 3D-Integration and Packaging, and Nanosensors for disease diagnostics.

On Tuesday night, we will feature an interactive panel session that promises to be both relevant and engaging. The panel: "Where will the next Intel be headquartered?" will be moderated by Professor Philip Wong from Stanford University. He will entertain a panel of experts and industry veterans into a lively discussion on who will drive and lead innovation in the semiconductor industry in the coming decades.

IEDM will also feature an entertaining entrepreneurial luncheon on Tuesday. In an informal setting Professor Leda Lunardi will interview Courtney Gras, named Forbes 30 Under 30 in Cleantech (2016) and a passionate entrepreneur and recognized leader with a diverse career in engineering, project management, and sales for the cleantech, defense, and aerospace industries. She will share her thoughts and experiences towards leadership and entrepreneurship.

For the second year, IEDM 2017 will host an Exhibits area during the conference where you can learn more about the latest products and publications. Stop by any time during the exhibition open hours to browse the booths and enjoy complementary coffee. Also, we will host in this venue the 2nd edition of the MRAM poster session, a joint initiative with the IEEE Magnetics Society. The poster session will cover MRAM materials/phenomena/ technology/testing, hybrid CMOS/MTJ technology and circuits, and spin-logic.

On behalf of Ken Rim, Technical Program Chair, and Mariko Takayanagi Technical Program Vice-Chair, as well as the entire IEDM committee, I want to express my sincere appreciation to all of the authors and speakers who contributed to the technical program. Your efforts are the engine that continues to make IEDM the premier conference in electron devices and related technologies. I also wish to thank each of the members of the IEDM executive and technical subcommittees whose dedication and efforts were critical in planning and organizing the 2017 conference.

IEDM is sponsored by the IEEE Electron Devices Society. If you are not already an IEEE member, please consider joining this great institution that has played such an important role globally for over 120 years. More detailed information regarding the IEEE is available at the conference and on their website – http://www.ieee.org.

It is again my great honor and pleasure to extend a warm welcome to everyone attending the 2017 IEEE International Electron Devices Meeting in helping to celebrate our 63rd year.

AWARD PRESENTATIONS

PLENARY SESSION AWARD

Monday, December 4

2016 Roger A. Haken Best Student Paper Award

To: Roman Koerner, University of Stuttgart/Philips U-L-M Photonics

For the paper entitled: "The Zener-Emitter: A Novel Superluminescent Ge Optical Waveguide-Amplifier with 4.7 dB Gain at 92 mA Based on Free-Carrier Modulation by Direct Zener Tunneling Monolithically Integrated on Si"

2016 EDS Paul Rappaport Award

To: Takatoshi Tsujimura, Takeshi Hakii, and Suguru Noda

For the paper entitled: "A Color-Tunable Polychromatic Organic-Light-Emitting-Diode Device With Low Resistive Intermediate Electrode for Rollto-Roll Manufacturing"

2016 EDS George Smith Award

To: Rongming Chu, Yu Cao, Mary Chen, Ray Li, and Daniel Zehnder

For the paper entitled: "An Experimental Demonstration of GaN CMOS Technology"

2017 EDS Education Award

To: Mansun Chan

"For pioneering innovative approaches in electronic engineering education"

2017 EDS J.J. Ebers Award

To: Kang L. Wang

"For contributions and leadership in strained SiGe and magnetic memory technologies"

2017 EDS Distinguished Service Award

To: Paul Yu

"To recognize and honor outstanding service to the Electron Devices Society"

2017 EDS Celebrated Members

To: Gordon Moore and Simon Sze

"For fundamental contributions to the field of electron devices for the benefit of humanity"

2017 IEEE/EDS Fellows

**This is a complete listing of the 2017 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2017 IEDM.*

Hugh Barnaby, Arizona State University, Tempe, Arizona, USA
Yu Cao, Arizona State University, Tempe, Arizona, USA
Edoardo Charbon, Delft University of Technology, Delft, Netherlands
Wei-ting Chien, SMIC-Semiconductor Mfg. Int'l Corp., Shanghai, China
Terry Ericsen, Ericsen Innovations LLC, Annapolis, Maryland, USA
Christopher Hierold, Swiss Federal Institute of Technology, Zurich, Switzerland

Ru Huang, Peking University, Beijing, China
Tian-wei Huang, National Taiwan University, Taipei, Taiwan
Chia-hong Jan, Intel Corporation, Portland, Oregon, USA
Quanxi Jia, University of Buffalo, Buffalo, New York, USA
Hongrui Jiang, University of Wisconsin, Madison, Wisconsin, USA
Richard King, Arizona State University, Tempe, Arizona, USA
Hulya Kirkici, Auburn University, Auburn, Alabama, USA
Steven Koester, University of Minnesota, Minneapolis, Minnesota, USA
Xiuling Li, University of Illinois, Champaign, Illinois, USA
Donald Lie, Texas Tech University, Lubbock, Texas, USA
Theresa Mayer, Virginia Tech, Blacksburg, Virginia, USA
Junichi Nakamura, Brillnics Japan Inc., Tokyo, Japan
Borivoje Nikolic, University of California, Berkeley, California, USA
Akihiro Nitayama, Tohoku University, Sendai, Japan
Tomas Palacios, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA
Dimitrios Peroulis, Purdue University, West Lafayette, Indiana, USA
Ramgopal Raovalipe, Indian Institute of Technology, Powai, Mumbai, India
Akira Toriumi (2016), University of Tokyo, Japan
Andrei Vladimirescu, Berkeley Wireless Research Center, Berkeley, California, USA
Sorin Voinigescu, University of Toronto, Toronto, Ontario, Canada
Xin Zhang, Boston University, Boston, Massuchusetts, USA

Entrepreners Luncheon

Tuesday, December 5, 12:30 – 2:00 p.m.
Continental 4

Speaker: Courtney A. Gras, Executive Director for Launch League.

Jointly sponsored by IEDM and IEEE Women in Engineering, the Entrepreneurs Lunch will feature Courtney A. Gras, Executive Director for Launch League. A local nonprofit focused on developing a strong startup ecosystem in NE Ohio. The moderator will be Professor Leda Lunardi from North Caroliuna State University.

IEDM Panel

Tuesday, December 5
Continental 1-5
Moderator: H.S. Philip Wong, Stanford University

Title: **Where will the next Intel be headquartered?**

Session 30: Plenary Session II
Wednesday, December 6
Grand Ballroom B

IEEE Awards
General Chair: Stefan De Gendt, imec

2017 IEEE Cledo Brunetti Award

To: Guido Groeseneken

"For contributions to the characterization and understanding of the reliability physics of advanced MOSFET nanodevices."

2017 IEEE Andrew S. Grove Award

To: Sorin Cristoloveanu

"For contributions to silicon-on-insulator technology and thin body devices."

2017 IEEE Frederik Philips Award

To: Gary L. Patton

"For industry influence and leadership in the development of leading-edge microelectronics technology and collaborative research."

Tutorials
Saturday, December 2
3:15 – 6:30 p.m.

Topics Presented at 3:15 – 4:45 p.m.
Continental 1-3 // Continental 4// Continental 5

The Evolution of Logic Transistors toward Low Power and High Performance IoT Applications

Dae Won Ha, Samsung Electronics

For more than 4 decades, logic transistors have been successfully evolved to satisfy the ever-increasing demands for high performance and low power consumption. Three innovative technologies have been applied to suppress the abrupt increase in standby and/or dynamic power consumption; HKMG (Hi-K Metal Gate) and mobility enhancement S/D strain engineering and FinFET device architecture. This tutorial will cover the evolution of logic transistors from past to future, starting with the limitation of planar transistors, i.e., excess standby power consumption. Then, today's state-of-the-art FinFET technologies will be introduced in detail, including layout, key design rules, short channel effects, multi-Vth engineering, local layout effects (LLE), variability, and so on. Finally, potential future GAA (Gate-All-Around) device architectures such as MBCFET (Multi-Bridge Channel FET) and VFET (Vertical FET) will be discussed. This tutorial will give attendees an overview and background sufficient to allow them to follow and participate in discussions on logic transistor technologies, especially focusing on FinFET.

Hardware Opportunities in Cognitive Computing: Near- and Far-term

Geoffrey Burr, IBM Research-Almaden

For more than 50 years the capabilities of Von Neumann-style information processing systems — in which a "memory" delivers operations and then operands to a dedicated "central processing unit" — have improved dramatically. While it may seem that this remarkable history was driven by ever-increasing density (Moore's Law), the actual driver was Dennard's Law: the amazing realization that each generation of scaled-down transistors could actually perform better, in every way, than the previous generation. Unfortunately, Dennard's Law terminated some years ago, and as a result, Moore's Law is now slowing considerably. In a search for ways to continue to improve computing systems, the attention of the IT industry has turned to approaches for computing that are not so dependent on getting billions of devices to work absolutely perfectly. One such approach is to move towards Non-Von Neumann algorithms, and in particular, to Cognitive Computing architectures motivated by the human brain. In this talk, I will review recent progress towards hardware implementation and/or acceleration of such brain-inspired computing architectures. This progress ranges from systems that combine conventional CMOS devices in different and unconventional ways to systems built around emerging NVM (Non-Volatile Memory) devices; and from systems designed to accelerate conventional ML (Machine Learning) through hardware innovation to systems that seek to transcend the limitations of current ML algorithms (such as the requirement for batch-based learning using vast datasets of static and labeled data).

Silicon Photonics for Next-Generation Optical Interconnects

Joris Van Campenhout, IMEC

Demand for data communication in cloud datacenters is projected to grow exponentially in the next few years. Leveraging the advanced manufacturing capability available in CMOS Fabs, silicon photonics has emerged in the past decade as a highly prospective integrated photonics technology, enabling scalable, Tb/s scale optical interconnects. In this tutorial, we will take a deep dive into the capabilities of this platform. First, we will discuss the short-reach optical interconnect scaling trends and industry roadmap. Next, we will discuss a variety of silicon photonics devices, covering passive devices as well as high-speed Si or GeSi modulators and photodetectors capable of operating at data rates as high as 100Gb/s. We will describe how these building blocks can be combined with low-power CMOS driving circuits to implement Tb/s scale electro-optical transceivers with unsurpassed bandwidth density and power efficiencies below 5pJ/bit. Finally, we will discuss future prospects for integrating GaAs and InP based laser sources on silicon by direct epitaxial growth.

Topics Presented at 5:00 – 6:30 p.m.
Continental 1-3 // Continental 4// Continental 5

Negative Capacitance Transistors

Sayeef Salahuddin, University of California, Berkeley

The physics of ordered and correlated systems allow for fundamental improvement of the energy efficiency when a transition happens between two distinguishable states. For ferroelectric materials where such order forms due to interaction between many dipoles, thermodynamics dictates that charge can be switched with much lower energy compared to conventional dielectrics. This leads to a situation where a ferroelectric material can be stabilized at a state of negative capacitance. In this tutorial, I shall discuss the physical origin of negative capacitance and how it can be stabilized to obtain an amplification of the electrostatic field. When combined with the gate of a transistor, this state of stabilized negative capacitance could lead to reduction in the supply voltage and/or increase of the ON current of a transistor. I shall discuss our understanding of this phenomena based on the most recent experimental results and possible pathways to optimize transistor performance for scaled nodes.

Fundamental, Thermal, and Energy Limits of PCM and ReRAM

Eric Pop, Stanford University

This tutorial will introduce the operation mechanism and fundamental limitations of non-volatile phase-change memory (PCM) and resistive random access memory (ReRAM). The two memory types will be presented in context, with emphasis placed on their thermal and energy limitations, down to atomic scale dimensions. We will also discuss modern devices, challenges, test structures, and simple models required to understand their operation. The tutorial will give attendees an overview and background sufficient to allow them to think and actively contribute to the discussion on the ultimate (i.e. sub-5 nm) limits of these memory technologies.

2.5D Interposers and High Density Fanout Packaging as Enablers for Future Systems Integration

Venkatesh Sundaram, Georgia Institute of Technology

As Moore’s law struggles to sustain the performance gains and cost reduction that has fueled the growth in electronics systems, advanced packaging has stepped in to complement transistor scaling with system scaling at the package level. Two major packaging technologies, 2.5D interposers and high density fan-out (HDFO), have gained prominence in recent years in enabling multi-die integration for higher bandwidth, lower power consumption and reduced design cycle times. This tutorial will provide an introduction to interposer and fanout packaging technologies, market drivers, application examples and infrastructure evolution, as well as latest state of the art innovations. In addition to silicon, organic and glass 2.5D interposers, emerging fanout technologies such as InFO used in Apple iPhones and embedded bridge (EMIB) introduced by Intel will also be explained.

Interposers bridge the interconnect gap between back end of the line (BEOL) pitch and current organic BGA packages. Interposers started out as a 2.5D multi-die integration step towards full 3D IC stacking. However, they are now viewed as a system integration platform with pervasive applications now and into the future. In the past couple of years, the technology development and manufacturing infrastructure maturity has been progressing rapidly. The first volume products using silicon interposers have been introduced in the graphics market since 2015 integrating high bandwidth memory (HBM) and GPUs. Several other applications are also exploring product designs based on interposer concepts. It is certainly an exciting time for interposer technologies. Emerging alternatives such as glass and new organic interposers are promising cost reduction from wafer based silicon interposers that should enable a much broader adoption of interposers. Although fanout packaging emerged in the first years of this century with approaches such as eWLB by Infineon, the introduction of high density fanout packages by TSMC to package application processors in iPhones in 2016-2017 has generated unprecedented excitement about the promise of this system integration approach that eliminates traditional substrate and assembly processes. This year's tutorial by one of the top advanced packaging experts in the world includes significant new material covering the latest advances in 2.5D and 3D interposers, and high density fanout packages. The course will address both fundamentals of interposer and fanout technology, as well as applications and supply chain infrastructure. The course will be interactive and include audience Q&A and samples of latest interposer demonstrators will be passed around for a hands-on experience.

Short Course

Boosting Performance, Ensuring Reliability, Managing Variation in sub-5nm CMOS

Sunday, December 3, Continental 1-5
9:00 a.m. – 5:30 p.m.

Course Organizer: Sandy Liao, Intel Corporation

In this short course six presenters from leading edge industry and government organizations will present their insights on the future of the semiconductor technology and scaling beyond the 5nm node. The entire stack will be covered from device physics and transistor scaling, to interconnect to BEOL and extending to system level requirements. Each expert will first introduce the state-of the art technologies implemented for 7nm, and then proceed to discuss opportunities and challenges such as novel materials, integration schemes, architectures and design techniques which will aid us in bridging the gap to 5nm and beyond.

The first speaker in the course is Gen Tsutsui, who will discuss transistor performance boosters for the 5nm node and beyond. He will focus on Si and SiGe based FinFET technologies and discuss device performance optimization in terms of mobility and reliability, while discussing issues specific to the gate dielectric interface on SiGe channels. He will be followed by Steve Hung who will focus on gate stack engineering for advanced FinFETs, in particular from Vt modulation perspective using work function engineered metal gate electrodes.

The interconnect challenges for the sub-5nm nodes will be covered by Zsolt Tokei, in which he will cover both fabrication challenges related to EUV lithography, track height scaling in standard cells and novel conductor materials, as well as performance issues such as trade-offs in power rails and signal wires and the circuit sensitivity to RC delay.

Two talks are dedicated to reliability issues at the transistor and BEOL level, respectively. First, Stephen M. Ramey will discuss transistor reliability issues such as gate oxide integrity, self-heating and transistor aging issues like BTI and hot carrier effects. He will be followed by Cathryn Christiansen who will cover BEOL reliability and performance challenges. She will start with an overview of reliability basics and improvements established for TDDB and EM through the 7nm node, and then follow-up with a discussion of potential boosters for 5nm nodes and beyond, including asymmetric spacing, thinner barriers/liners, alternative metals, lower-k dielectrics, airgap, and self-aligned vias. Putting everything into perspective, Andy Wei will wrap up the short course with a presentation about design-technology co-optimization for beyond 5nm Node. The focus will be on an evaluation of device options beyond the 5nm node combined with a discussion of opportunities for system level innovation and future product requirements.

Introduction and Overview
Organizer: Sandy Liao, Intel Corporation

Transistor Performance Elements for 5nm Node and Beyond
Instructor: Gen Tsutsui, Research Staff Member, IBM

- Performance elements overview
- SiGe/Ge FinFET intrinsic benefit -mobility, reliability, Vt tenability
- Gate dielectrics interface engineering for SiGe fin
- Si and SiGe CMOS FinFET integration

Multi-Vt Engineering and Gate Performance Control for Advanced FinFET Architecture
Instructor: Steven CH Hung, Gate Stack Module, Cross Business Unit, Applied Materials Inc.

- Introduction on sub 5nm landscape and challenges
- Scaling and performance control for Si and SiGe channel
  - Impact of trace element on scaling and performance
  - Process options to achieve scaling target
- Gate level Vt engineering
  - Vt modulation through WF layer thickness control
  - Vt modulation through ALD dipole formation
  - Vt modulation through material modulation

Sub-5nm Interconnect Trends and Opportunities
Instructor: Zsolt Tokei, Distinguished Member of Technical Staff, IMEC

- Recent trends and landscape in interconnect technology
- Consequence of track height scaling on BEOL
- Trade-off power and signal wires, circuit sensitivity to RC
- Dimensional scaling and examples of technology boosters (e.g. Supervia, buried rail...)
- Multipatterning and EUV for logic BEOL (LE^x, SADP, SAQP, ...)
- Material choices; conductors and dielectrics; emergence of alternative metals
- Conductor resistance and variability
- Extending dual damascene and opportunities in semi-damascene
- New materials, new opportunities

Transistor Reliability: Physics, Current Status, and Future Considerations
Instructor: Stephen M. Ramey, Manager, Transistor Reliability Group, Logic Technology Development, Intel Corporation

- Gate oxide breakdown (TDDB)
- Transistor aging: BTI
- Self-heat
- Transistor aging: Hot carrier
- Aging Variation

Back End Reliability Scaling Challenges, Variation Management, and Performance Boosters for sub-5nm CMOS
Instructor: Cathryn Christiansen, Senior Manager/Deputy Director, BEOL Reliability, Quality and Reliability Assurance, GLOBALFOUNDRIES

- Reliability basics, scaling and variability challenges, and improvements through 7nm for BEOL time dependent dielectric breakdown (TDDB)
- Reliability basics, scaling and variability challenges, and improvements through 7nm for electromigration (EM)
- BEOL Performance Boosters for sub-5nm and effects on TDDB and EM, including asymmetric spacing, thinner barriers/liners, alternative metals, lower-k dielectrics, airgap, and fully aligned vias.

Design-Technology Co-Optimization for Beyond 5nm Node
Instructor: Andy Wei, Senior Fellow, TechInsights

- I thought Moore's Law was dead: What's driving accelerated scaling?
- DTCO Overview: PPA + C + TTM
- Challenges: beyond the 40 nm pitch barrier and Gate All Around
- Beyond 5nm device option evaluation
- System level innovation and future product requirements

Short Course

Memories for the Future: Devices, Technologies, and Architecture
Sunday, December 3, Continental 6
9:00 a.m. – 5:30 p.m.

Course Organizer: Kevin Zhang, Vice President, Design and Technology Platform, TSMC

Memories play an increasingly important role in all VLSI applications, ranging from high-performance computing, mobile and IoT to automotive, which each domain presenting their specific challenges. The demand for higher density, lower-power, and non-volatility has led to extensive investments across the industry into new memory technologies. Some of these so-called "emerging memories" have are now reaching maturity, leading to new usage models based on their unique technology attributes. In this short-course, seven experts will cover a broad range of topics in the area of novel memory technology. First, Alfonso Maurelli will discuss the scaling of embedded nonvolatile memories for automotive applications. He will present the key technology scaling challenges and discuss their solutions to drive the eNVM technology to meet the future requirements for automotive electronics. Nirmal Ramaswamy will follow with a technology overview of ReRAM technology for 3D Crosspoint Memories, this new class of memory boast an unparalleled storage density while rivaling DRAM in terms of access latency. Thomas Mikolajick will discuss the key breakthroughs in Ferroelectric devices that have the potential to bring this memory into CMOS-based technologies for embedded applications, furthermore both ReRAM and ferroelectric devices are of interest for neuromorphic applications. Spin-Transfer-Torque (STT) MRAM has drawn lots of interest in recent years due to its unique memory characteristics and scalability. Danny Shum will present state-of-the-art STT-MRAM memories and their applications. To give a broader perspective on the future of memories, the short course will finish with two lectures on memory circuit design for low-power applications and future architectures merging memory and logic to provide 1000X power efficiency improvements. They will be given by Jonathan Chang and Subhasish Mitra, respectively. Overall, the short-course is intended to provide both good breadth and in-depth coverage on the most recent memory technology advancement and the future direction.

1. **Embedded Non Volatile Memory for Automotive applications,** Alfonso Maurelli, STMicroelectronics
   Introduction
   eNVM market overview
   Automotive requirements for eNVM
   Main NVM cells and technology implementations in production
   Perspectives
   Conclusions

2. **3D ReRAM: Crosspoint Memory Technologies,** Nirmal Ramaswamy, Micron
   Memory scaling
   DRAM and NAND scaling
   ReRAM introduction
   ReRAM memory options
   Selector review and options
   Selector requirements for Crosspoint memory
   Margin tradeoffs for cell+selector schemes
   Integration options
   General selector and cell requirements for 'deck by deck' vs 3D
   High level conclusions on cost requirements and trade offs

3. **Ferroelectric Memory in CMOS Processes,** Thomas Mikolajick, Namlab
   Basics of Ferroelectricity
   Ferroelectricity in Hafnium Oxide
   Ferroelectric RAM using 1T-1C Architecture
   Ferroelectric Field Effect Transistors
   Other Applications
   Summary and Outlook

4. **Embedded Memories Technology scaling & STT-MRAM for IoT & Automotive,** Danny P. Shum, GLOBALFOUNDRIES
   What are embedded memories and scaling limitations

Why are embedded STT-MRAM memories important
What are the challenges for STT-MRAM as embedded memories usage
How are embedded STT-MRAM memories used – Application specific IoT & Automotive

5. **Embedded Memories for Energy Efficient Computing,** Jonathan Chang, TSMC
   Embedded memory landscape
   Requirements of embedded memories for energy efficient computing
   SRAM scaling
   eFlash for automotive
   MRAM for IoT applications
   MRAM for mobile applications
   RRAM for IoT applications
   Summary

6. **Memory Centric Abundant Data Computing,** Subhasish Mitra, Stanford University
   Memory wall in processors and accelerators
   In-memory compute
   Monolithic 3D Integration vs TSV 3D
   Interwoven memory, logic and sensor arrays using heterogeneous technologies
   Abundant data applications: graph analytics, deep learning
   Summary

Session 1: Plenary
Monday, December 4
Grand Ballroom B

Welcome and Awards
General Chair: Stefan De Gendt, imec

Plenary Papers
Technical Program Chair: Ken Rim, Qualcomm

1.1 Multi-Chip Technologies to Unleash Computing Performance Gains over the Next Decade (Invited), *L. T. Su, S. Naffziger, and M. Papermaster, Advanced Micro Devices*

Datacenter and high-performance computing capabilities have continued their exponential improvements in performance over the prior decade, driven by the proliferation of devices and data through the internet of things (IoT), and new applications in the enterprise and cloud. This trend will continue over the next decade as the demand for compute performance continues to grow with exabytes of data being created daily and new use models incorporating machine learning and artificial intelligence become more prevalent. As Moore's Law has slowed in recent years, numerous techniques including system, architectural and software innovation have been used to extend the high-performance processor performance improvements. We examine these techniques and demonstrate that although some of these will continue, new innovations are needed especially at the system level to continue the performance trend over the next decade. We believe that multi-chip technologies and system level innovations are key to unlocking the performance gains in computing over the next decade.

1.2 Energy Efficient Computing and Sensing in the Zettabyte Era: from Silicon to the Cloud (Invited), *A. M. Ionescu, Nanolab, Ecole Polytechnique Fédérale de Lausanne*

In this paper we will present and discuss some of the great research challenges and opportunities related to 21st Century energy efficient computing and sensing devices and systems, in the context of the Internet of Things revolution. It is suggested that in the future major innovations in Information and Communication Technologies (ICT) will requires holistic approaches encompassing silicon and cloud technologies and will be centered on big/deep data and context. The predicted future global amounts of stored, computed, communicated and sensed information will challenge the world capability to deal with zettabytes of data, which sets both fundamental and practical needs for energy efficiency.

1.3 System Scaling for Intelligent Ubiquitous Computing (Invited), *J. Y-C. Sun, Taiwan Semiconductor Manufacturing Company*

Wafer based 3Dx3D system scaling revolutionizes machine learning (ML) and artificial intelligence (AI) as well as mobile computing. It may trigger a big bang in intelligent ubiquitous computing. 3D CMOS scaling continues with many challenges and opportunities for relentless innovation in materials, processes, devices, circuits, design, EDA, computing architectures, algorithms, and software. 3D stacking and heterogeneous system integration, e.g., CoWoS® and InFO, not only augments but also amplifies the benefits of 3D CMOS logic, 3D memory, integrated specialty technologies and 3D sensors for intelligent ubiquitous computing. The virtuous cycles of 3Dx3D system scaling innovation may expand like a galaxy or universe. The aggregate transistor count in a 3Dx3D sub-system may reach the equivalent of human brain in the 2020s to provide brain-like augmented intelligence.

Session 2: Memory Technology - ReRAM and Selectors
Monday, December 4
Grand Ballroom A
Co- Chairs: Rainer Waser, RWTH Aachen University
Gabriele Navarro , CEA-Leti

1:35 PM
2.1 Breakthrough of Selector Technology for cross-point 25-nm ReRAM, *S. G. Kim, J. C. Lee, T. J. Ha, J. H. Lee, J. Y. Lee, Y. T. Park, K. W. Kim, W. K. Ju, Y. S. Ko, H. M. Hwang, B. M. Lee, J. Y. Moon, W. Y. Park, B. G. Gyun, B.-K. Lee, D. Yim, and S.-J. Hong, SK Hynix Inc.*

In this paper, the authors report for the first time the outstanding selector performance from an innovative oxide selector. SiO_2, one of conventional and common materials in semiconductor industry, was chosen as a matrix oxide material. Metal atoms which are non-mobile and easy to handle were injected into the oxide films. Off-current and threshold voltage (Vth) could be controlled by using arsenic (As), which doping method and concentration were carefully investigated to achieve threshold switching behavior. Finally ReRAM (Resistance switching Random Access Memory) cell array consisted of one selector-one resistor (1S1R) was successfully demonstrated with the full integration of the newly developed selector.

2:00 PM
2.2 An Ultra High Endurance and Thermally Stable Selector based on TeAsGeSiSe Chalcogenides Compatible with BEOL IC Integration for Cross-Point PCM, *H. Y. Cheng, W. C. Chien, I. T. Kuo, E. K. Lai, Y. Zhu*, J. L. Jordan-Sweet*, A. Ray*, F. Carta*, F. M. Lee, P. H. Tseng, M. H. Lee, Y. Y. Lin, W. Kim*, R. Bruce*, C. W. Yeh, C. H. Yang, M. BrightSky* and H. L. Lung, Macronix International Co., Ltd., *IBM TJ Watson Research Center*

We present the results of a primary study on a OTS chalcogenide material system (TeAsGeSi) that incorporating Se and an extra dopant. Vth and IOFF are trade-off parameters that can be tuned by modification of OTS composition, thickness and process temperature. The resulting new selector material demonstrated excellent endurance (>1010 with 50ns-pulsed 400uA On-current) and robust OTS characteristics after 350 C/30 mins annealing. The thin film could withstand 500 C annealing.

2:25 PM
2.3 In-depth investigation of programming and reading operations in RRAM cells integrated with Ovonic Threshold Switching (OTS) selectors, *M. Alayan, E. Vianello, G. Navarro, C. Carabasse, S. La Barbera1, A. Verdy, N. Castellani, A. Levisse, G. Molas, L. Grenouillet, T. Magis, F. Aussenac, M. Bernard, B. DeSalvo, J. M. Portal*, E. Nowak, CEA, LETI, *Aix-Marseille Université, IM2NP, CNRS UMR*

This paper presents an HfO_2 based resistive switching memory (RRAM) in series with a GeSe- based Ovonic Threshold Switching (OTS) selector. Detailed investigation of the main memory operations, forming, set, reset and read is presented for the first time to our knowledge. An innovative reading strategy is proposed. The selector switching is performed only if the RRAM cell is in the Low Resistive State (LRS), while the reading of the High Resistive State (HRS) is performed without switching the OTS selector, preventing disruptive reading when the RRAM cell is in HRS. Up to 106 read cycles have been demonstrated with a stable memory window of one decade and a stable OTS OFF state.

2:50 PM *Coffee Break*

3:15 PM
2.4 BEOL Based RRAM with One Extra-mask for Low Cost, Highly Reliable Embedded Application in 28 nm Node and Beyond, *H. Lv, X. Xu, P. Yuan, D. Dong, T. Gong, J. Liu, Z. Yu, P. Huang***, K. Zhang, C. Huo, C. Chen, Y. Xie, Q. Luo, S. Long, Q. Liu, J. Kang***, D. Yang*, S. Yin*, S. Chiu* and M. Liu, Chinese Academy of Sciences, *Semiconductor Manufacturing International Corporation, **University of Chinese Academy of Sciences, ***Peking University*

In this work, we demonstrated a low cost, BEOL based embedded RRAM technology by adding only one extra mask on standard 28 nm logic platform. Satisfactory characteristics such as forming free, high on/off ratio (>100) and high operation speed (<100 ns) were achieved. Array level performance on thermal stability shows both LRS and HRS exhibit excellent stability at high temperature up to 260 oC. The resistance fluctuation caused by RTN signal and atomic structural change were clarified experimentally. Memory window and reading voltage selection are crucial to diminish the resistance variation. Compared with conventional eFLASH, this BEOL based RRAM technology provides a competitive solution for low power, low cost embedded application in 28 nm node and beyond.

3:40 PM
2.5 A Comprehensive Study of 3-stage High Resistance State Retention Behavior for TMO ReRAMs from Single Cells to a Large Array, *Y.-H. Lin, Y.-H. Ho, M.-H. Lee, C.-H. Wang, Y.-Y. Lin, F.-M. Lee, K.-C. Hsu, P.-H. Tseng, D.-Y. Lee, K.-H. Chiang, K.-C. Wang, T.-Y. Tseng*,and C.-Y. Lu, Macronix International Co., Ltd., *National Chiao Tung University*

For the first time, the retention of high resistance state in ReRAM is found to compose of three stages — extending tail-bits, distribution shift, and distribution broadening. A three-dimensional kinetic Monte Carlo simulation is proposed to explain the mechanisms and resistance fluctuation of each stage in different time and temperature scales.

4:05 PM
2.6 Integrated HfO_2-RRAM to Achieve Highly Reliable, Greener, Faster, Cost-Effective, and Scaled Devices, *C.H. Ho, S.-C. Chang, C.-Y. Huang, Y.-C. Chuang, S.-F. Lim, M.-H. Shieh, S.-C. Chang, and H.-H. Liao, Winbond Electronics Corp.,*

For the first time, this work demonstrated a 90nm 512Kb SPI HfO2-RRAM product vehicle successfully with reducing read / write power by 18X / 2X, boosting read / write speed by 5X / 10X, and scaling feature size by 2X, compared to presented 512Kb SPI EEPROM; while sustaining high reliability on million cycle endurance, even better post-cycle retention (85oC retention 100years for post 100K cycles), and 150oC high temperature operation, by optimized mismatching, read-integrity, relaxation, and noise as discussed in this work. Technology also offers alternative solution for greener, highly-reliable, and scaled NOR Flash applications. A new plasma dicing technology was implemented to further increase gross die per wafer.

4:30 PM
2.7 8-layers 3D Vertical RRAM with Excellent Scalability towards Storage Class Memory Applications, ***Q****. Luo, X. Xu, T. Gong , H. Lv, D. Dong, H. Ma, P. Yuan, J. Gao, J. Liu, Z. Yu, J. Li, S. Long, Q. Liu, M. Liu, Chinese Academy of Sciences, *University of the Chinese Academy of Sciences*

For the first time, we experimentally demonstrated a bit cost scalable (BiCS) 8-layer 3D vertical RRAM with ultimate scalability. The design of self-selective cell (SSC) with non-filamentary switching were successfully extended to 8 stacks and exhibits salient features, including high nonlinearity (>102), forming free and high endurance (>107). An extremely scaled 3D structure with 5 nm size and 4 nm vertical pitch was further demonstrated. The sub µA operation current is quite promising for low power applications, but not good for sensing speed. A fixed bitline voltage sensing circuit was proposed to address the latency issue. Sub-µs read latency in bit sensing mode was successfully achieved.

Session 3: Focus Session - Process and Manufacturing Technology - 3D Integration and Packaging
Monday, December 4
Grand Ballroom B
Co-Chairs: Kuan-Neng Chen, National Chiao Tung University
Lucile Arnaud, CEA-Leti

1:35 PM
3.1 3D Sequential Integration: Application-driven technological achievements and guidelines (Invited), *P. Batude, L. Brunet, C. Fenouillet-Beranger, F. Andrieu, J-P. Colinge, D. Lattard, E. Vianello, S. Thuries, O. Billoint, P. Vivet, C. Santos, B. Mathieu, B. Sklenard, C.-M. V. Lu, J. Micout, F. Deprat, E. Avelar Mercado, F. Ponthenier, N. Rambal, M.-P. Samson**, M. Cassé, S. Hentz, J. Arcamone, G. Sicard, L. Hutin, L. Pasini, A. Ayres, O. Rozeau, R. Berthelon, F. Nemouchi, P. Rodriguez, J-B. Pin*, D. Larmagnac*, A. Duboust*, V. Ripoche*, S. Barraud, N . Allouti, S. Barnola, C. Vizioz, J.-M. Hartmann, S. Kerdiles, P. Acosta Alba, S. Beaurepaire, V. Beugin, F. Fournel, P. Besson**, V. Loup, R. Gassilloud, F. Martin, X. Garros, F. Mazen, B. Previtali, C.Euvrard-Colnat, V. Balan, C. Comboroure, M. Zussy, Mazzocchi, O. Faynot, and M. Vinet, .CEA- leti, Minatec, *Applied Materials, **STMicroelectronics*

3D Sequential Integration (3DSI) with ultra-small 3D contact pitch (<100nm) offers new 3D partitioning options at fine granularities. This paper reviews potential applications ranging from computing to sensor interface and gives an update on 3DSI device development. Low-temperature processing techniques have made great progress and High Performance (HP) digital stacked FETs for computing application can be achieved with a 500°C Thermal Budget (TB). In addition, ULK/metal lines capable of withstanding this TB can be used between stacked tiers. Ultra-Low TB FETs (<400°C) have potential for low-power applications and allow for the stacking of multiple layers.

2:00 PM
3.2 Pixel/DRAM/logic 3-layer stacked CMOS image sensor technology (Invited), *H. Tsugawa, H. Takahashi, R. Nakamura, T. Umebayashi, T. Ogita, H. Okano, K. Iwase, H. Kawashima, T. Yamasaki*, D. Yoneyama*, J. Hashizume, T. Nakajima, K. Murata, Y. Kanaishi, K. Ikeda*, K. Tatani, T. Nagano, H. Nakayama*, T. Haruta and T. Nomoto, Sony Semiconductor Solutions Corp., Kanagawa, *Sony Semiconductor Manufacturing Corp.*

We developed a CMOS image sensor (CIS) chip, which is stacked pixel/DRAM/logic. In this CIS chip, three Si substrates are bonded together, and each substrate is electrically connected by two-stacked through-silica vias (TSVs) through the CIS or dynamic random access memory (DRAM). We obtained low resistance, low leakage current, and high reliability characteristics of these TSVs. Connecting metal with TSVs through DRAM can be used as low resistance wiring for a power supply. The Si substrate of the DRAM can be thinned to 3 μm, and its memory retention and operation characteristics are sufficient for specifications after thinning. With this stacked CIS chip, it is possible to achieve less rolling shutter distortion and produce super slow motion video.

2:25 PM
3.3 Power Inside - Applications and Technologies for Integrated Power in Microelectronics (Invited), *C. Ó Mathúna, S. Kulkarni, Z. Pavlovic, D. Casey, J. Rohan, A-M Kelleher, G. Maxwell, J. O'Brien, P. McCloskey, Tyndall National Institute, University College Cork*

The emergence of miniaturized and integrated Power Supply on Chip (PwrSoC) and Power Supply in Package (PwrSiP) platforms will be enabled by the application of thin-film, integrated magnetics on silicon. A process flow for, and the design of, a thin-film coupled-inductor, switching at 60MHz, is described. Based on the large signal characterization data, measured up to 100MHz,, the efficiency of the inductor is measured to be 91.7% for a power of 0.5W.

2:50 PM
3.4 3D System Package Architecture as Alternative to 3D Stacking of ICs with TSV at System Level (Invited), *R. Tummala, Georgia Tech.*

The 3D packaging started in 1970s for packaging of memory packages. Memory density has always been the bottleneck in high performance computing systems that led to two paths; increasing memory density within a chip in 2D and increasing by stacking many either packaged or bare chips in 3D. The barrier to systems performance, however, has been latency and bandwidth between logic and memory. 3D stacking of logic and memory has been viewed as the ultimate solution for a decade but it has its own barriers. While these barrier are being overcome by many approaches, the ultimate goal is to form miniaturized systems with highest performance and reliability at lowest cost. This paper presents a 3D system package architecture to address both bandwidth and other system requirements at system level in contrast to 3D ICs at device level.

3:15 PM *Coffee Break*

3:40 PM
3.5 Advanced Packaging Saves the Day! - How TSV Technology Will Enable Continued Scaling (Invited), *L. England and I. Arsovski, GLOBALFOUNDRIES*

Technology scaling is becoming more difficult and costly with each generation. As we scale below 7nm, there is uncertainty in the methodology that will be used for device formation and integration. Now, more than ever, the use of advanced packaging technologies is needed to help extend the lifetimes of our most advanced fab technologies. In this "More Than Moore" era, transistor density can be considered in terms of volume rather than area, and the proliferation of TSV integration is the key enabling technology.

4:05 PM
3.6 Advanced Packaging with Greater Simplicity (Invited), *D. C.H. Yu, Taiwan Semiconductor Manufacturing Company*

Integrated Fan-Out (InFO) is developed with greater simplicity, based on subtraction in structure, process flow and supply chain management. It achieved un-precedent results compared to others using "additional" structure, including electrical performance, power consumption, thermal resistance, form factor/thickness and cost effectiveness. Greater simplicity continues play critical role for advanced packaging to achieve system PPAC goals.

4:30 PM
3.7 Towards Cube-Sized Compute Nodes: Advanced Packaging Concepts enabling Extreme 3D Integration (Invited), ***T***. *Brunschwiler, G. Schlottig, A. Sridhar, P. Bezerra*, P. Ruch, N. Ebejer, H. Oppermann**, J. Kleff**, W.*

*Steller***, M. Jatlaoui^, F. Voiron^, Z. Pavlovic^^, P. McCloskey^^, D. Bremner^^^, P. Parida#, F. Krismer2, J. Kolar2, and B. Michel1, IBM Research – Zurich, *ETH – PES, Zurich, **FhG – IZM, ***FhG – IZM – ASSID, ^Murata, ^^Tyndall National Institute, Cork, ^^^Optocap, Livingston, #IBM TJ Watson Research Center*

Novel heat removal and power delivery topologies are required to enable 'extreme 3D integration' with cube-sized compute nodes. Therefore, a technology roadmap is presented supporting memory-on-logic and logic-on-logic in the medium and long-term, by (i) dual-side cooling and integrated voltage regulators, and (ii) interlayer cooling and electrochemical power delivery.

Session 4: Modeling and Simulation - Modeling and Simulation of Advanced Non-volatile Memory
Monday, December 4
Continental Ballroom 1-3
Co-Chairs: Masumi Satoh, Toshiba Corporation
Richard Williams, IBM

1:35 PM
4.1 Atomistic Investigation of the Electronic Structure, Thermal Properties and Conduction Defects in Ge-rich Ge_xSe_{1-x} Materials for Selector Applications, *S. Clima, B. Govoreanu, K. Opsomer, A. Velea, N.S. Avasarala, W. Devulder, I. Shlyakhov*, G. L. Donadio, T. Witters, S. Kundu, L. Goux, V. Afanasiev*, G.S. Kar, G. Pourtois, imec, *University of Leuven*

We investigate the electronic structure and defects of GexSe1-x materials at the atomic level, using full-layer-thickness (5nm) amorphous models. In Ge-rich GexSe1-x, the nature of the mobility gap defects is mostly related to miscoordinated Ge. The population/localization of mobility-gap states changes solely under the effect of electric field. Strong covalent bonds introduced by N doping in the material increase its thermal conductivity and crystallization temperature beyond 600C. C/N dopants are found to add/remove mobility-gap states in the doped systems. Our investigation sets guidelines for material design in view of improved electro-thermal device performance.

2:00 PM
4.2 Ab-*initio* Modeling of CBRAM Cells: from Ballistic Transport Properties to Electro-Thermal Effects, *F. Ducry, A. Emboras, S. Andermatt, M. H. Bani-Hashemian, B. Cheng, J. Leuthold and M. Luisier, ETH Zurich*

We present atomistic simulations of conductive bridging random access memory cells from first-principles combining density-functional theory and the Non-equilibrium Green's Function formalism. Realistic device structures containing an atomic-scale filament have been constructed and their transport properties have been studied in the ballistic limit and in the presence of electron-phonon scattering.

2:25 PM
4.3 Fundamental Mechanism Behind Volatile and Non-Volatile Switching in Metallic Conducting Bridge RAM, *N. Shukla, R. Krishna Ghosh, B. Grisafe and S. Datta, University of Notre Dame*

In this work, we: (a) define an active-electrode selection criterion for non-volatile and volatile switching in metallic CBRAM; (b) simulate using MD+NEGF, the predicted volatile and non-volatile switching behavior in Ag/HfO2/Pt and Co/HfO2/Pt, along with the intrinsic switching time; (c) predict the switching behavior of other CBRAM active-electrodes, and corroborate with experiments.

2:50 PM
4.4 Modeling Disorder Effect of the Oxygen Vacancy Distribution in Filamentary Analog RRAM for Neuromorphic Computing, *B. Gao, H. Wu, W. Wu, X. Wang, P. Yao, Y. Xi, W.Zhang, N. Deng, P. Huang*, X. Liu*, J. Kang*, H.-Y. Chen**, S. Yu***, and H. Qian, Tsinghua University, *Peking University, **GigaDevice Semiconductor Inc., ***Arizona State University*

Physical mechanism of abrupt switching to analog switching transition is investigated using KMC simulation. A disorder-related model for Vo distribution is proposed with an order parameter to quantify the analog behaviors. Simulation results are verified by experiments performed on 1kb-RRAM-array. It is suggested that disordered Vo distribution is desired for analog switching.

3:15 PM *Coffee Break*

3:40 PM

4.5 Comprehensive Investigations on Charge Diffusion Physics in SiN-based 3D NAND Flash Memory through Systematical *Ab* initio Calculations, *J. Wu, D. Han*, W. Yang, S. Chen**, X. Jiang* and J. Chen, Shandong University,*Chinese Academy of Sciences, **East China Normal University*

Aiming at comprehensive understandings on the underlying physics of the charge diffusion in charge-trap (CT) 3D NAND flash memories, various hydrogen (H) and oxygen (O) incorporated defects in SiN CT layer are studied via ab initio calculations. It is found that, O atom incorporated defects are extremely shallow and could be the main reason of fast charge loss, while H atom incorporated defects should be the dominant traps in SiN CT layer. More importantly, though H passivation is effective to eliminate shallow traps, excessive H will generate other shallow traps on the contrary. Then, with further discussions on H bond stabilities, it is proposed that replacing H with Deuterium (D) could be an effective approach to suppress shallow trap generations during Write/Erase cycling and improve memory reliabilities.

4:05 PM

4.6 A Physics-based Quasi-2D Model to Understand the Wordline (WL) Interference Effects of Junction-Free Structure of 3D NAND and Experimental Study in a 3D NAND Flash Test Chip, *W.-C. Chen, H.-T. Lue, C.-C. Hsieh, Y.-C. Lee, P.-Y. Du, T.-H. Hsu, K.-P. Chang, K.-C. Wang and C.-Y. Lu, Macronix International Co., Ltd*

This paper provides a quasi-2D model simulating the surface potential variation inside a junction-free 3D NAND. It is clarified that the neighbor WL Vpass and Vt interference effects are the outcome of the surface potential continuity instead of WL fringe field effect. WL interference is studied in a 32Gb 16-layer single-gate vertical-channel (SGVC) 3D NAND Flash test chip. It is found that the far-neighbor WL cell also contributes to the WL interference, which could be suppressed by applying a lower BL sensing voltage. A practical WL iterating programming method can greatly cancel the WL interference effects and produce tight programmed Vt distribution for multi-level cell (MLC) operations.

4:30 PM

4.7 Temperature Activation of the String Current and its Variability in 3-D NAND Flash Arrays, *D. Resnati, A.Mannara, G. Nicosia, G. M. Paolucci*, P. Tessariol*, A.L. Lacaita, A.S.Spinelli, and C. Monzio Compagnoni, Politecnico di Milano, *Micron Technology Inc.*

After calibrating a TCAD model for current transport through the thin polysilicon channel of 3-D NAND Flash strings, we show for the first time that the variability in the polysilicon grain configuration in cell channel represents a nonnegligible source of statistical broadening for the array VT distribution when temperature is changed.

Session 5: Nano Device Technology - 2D and Carbon Nanotube Devices

Monday, December 4

Continental Ballroom 4

Co-Chairs: Wei-Chih Chien, Macronix

Rossella Ranica, STMicroelectronics

1:35 PM

5.1 Gate-tunable memristors from monolayer MoS_2 (Invited), V. K. Sangwan, H.-S. Lee, and M. C. Hersam, Northwestern University

We report here gate-tunable memristors based on monolayer MoS2 grown by chemical vapor deposition (CVD). These memristors are fabricated in a field-effect geometry with the channel consisting of polycrystalline MoS2 films with grain sizes of 3-5 microns. The device characteristics show switching ratios up to ~500, with the resistance in individual states being continuously gate-tunable by over three orders of magnitude. The resistive switching results from dynamically varying threshold voltage and Schottky barrier heights, whose underlying physical mechanism appears to be vacancy migration and/or charge trapping. Top-gated devices achieve reversible tuning of threshold voltage, with potential utility in non-volatile memory or neuromorphic architectures.

2:00 PM

5.2 First Demonstration of High Performance 2D Monolayer Transistors on Paper Substrates, S. Park and D. Akinwande, The University of Texas

In this work, we realize high performance transistors with graphene and MoS2 on commercially available paper substrates for the first demonstration. CVD graphene and MoS2 FETs feature record GHz operation and flexibility on paper, which indicates that high performance nanoelectronics on low-cost paper substrates for IoT and sensors is achievable.

2:25 PM

5.3 Room Temperature 2D Memristive Transistor with Optical Short-term Plasticity, X. Xie, J. Kang, Y. Gong*, P. M. Ajayan* and Kaustav Banerjee, University of California, Santa Barbara, *Rice University

A room temperature light-sensitive memristive transistor is demonstrated for the first time. This is achieved by creating a quantum dot superlattice structure fabricated on monolayer MoS2 where the quantum dots work as charge traps that induce memristive resistance, which can be modulated by a gate-induced electric field and exhibits light stimulation.

2:50 PM

5.4 Coexistence of volatile and non-volatile resistive switching in 2D *h*-BN based electronic synapses, Y. Shi, C. Pan, V. Chen*, N. Raghavan**, K. L. Pey**, F. M. Puglisi***, E. Pop*, H.-S. P. Wong*, M. Lanza, Soochow University, *Stanford University, **Singapore University, ***Università di Modena e Reggio Emilia

We fabricate electronic synapses using multilayer hexagonal boron nitride as switching layer. Their main advantage is that they show both volatile and non-volatile resistive switching depending on the programming stresses applied, which allows implementing short-term and long-term plasticity rules using a single device and without the need of complex architectures.

3:15 PM *Coffee Break*

3:40 PM

5.5 Scaling Carbon Nanotube CMOS FETs towards Quantum Limit (Invited), C. Qiu, Z. Zhang, and L.-M. Peng, Peking University

Owing to its ultra-thin body and high carrier mobility, semiconducting carbon nanotube (CNT) has been considered as an ideal channel material for future field-effect transistors (FETs) with sub 10 nm channel length. With well-designed device structure and when combined with graphene, we demonstrated high performance top-gated CNT FETs with gate length scaled down to 5nm. Scaling trend study reveals that sub-10 nm CNT CMOS FETs significantly outperform Si CMOS FETs with the same gate length but at much lower supply voltage Vds (0.4 V vs. 0.7 V), with an excellent sub- threshold slope swing (SS) of about 73mV/decade even with the gate length being scaled down to 5 nm. The 5 nm CNT FET begins to touch the quantum limit of a FET, and involves approximately only one electron when switching between on- state and off-state. These results show that CNT CMOS technology has the potential to go much further than that of Si towards quantum limit.

4:05 PM

5.6 Solution-Processed Carbon Nanotubes based Transistors with Current Density of 1.7 mA/µm and Peak Transconductance of 0.8 mS/µm, D. Zhong, M. Xiao, Z. Zhang, and L.-M. Peng, Peking University

High performance field-effect transistors are fabricated based on solution processed carbon nanotubes film. Via adopting stacked contacts and double gates, the FETs with gate length of 120 nm exhibit maximum drive current density of 1.7 mA/um and peak transconductance of 0.8 mS/um,which create a new record for CNT FETs.

4:30 PM

5.7 Benchmarking of Monolithic 3D Integrated MX_2 FETs with Si FinFETs, T. Agarwal, A. Szabo*, M.G. Bardon, B. Soree, I. Radu, P. Raghavan, M. Luisier*, W. Dehaene, and M. Heyns, imec, *ETH, Zurich

In this paper, monolayer transition metal dichalcogenide (MX2) FETs are benchmarked with Si FinFET using energy-delay as figure-of-merits and a physical compact model. The model is validated with the help of both atomistic simulations and experimental data for different materials, without the use of any fitting parameter. Single-gate (SG) and double-gate (DG)

MX2 FETs are compared from ON current, device capacitance and energy-delay perspective. DG MX2 FETs perform 25-30% faster than SG MX2 FETs for the same energy consumption in case of dominating wire load. WS2 DG FET shows both better energy and speed among chosen MX2 materials. However, in comparison to FinFET, WS2 DG FETs are shown to be ~ 35% slower, but more energy efficient. Therefore, to match FinFET's performance with MX2 FETs, monolithic 3D integrated MX2 SG and DG FETs are explored. It is shown that 3-5 stacked WS2 DG FETs are needed to meet N3 FinFET performance.

Session 6: Circuit and Device Interaction - Devices and Circuits for Neuromorphic and Stochastic Comparison
Monday, December 4
Continental Ballroom 5
Co-Chairs: Shimeng Yu, Arizona State University
Runsheng Wang, Peking University

1:35 PM
6.1 NeuroSim+: An Integrated Device-to-Algorithm Framework for Benchmarking Synaptic Devices and Array Architectures, *P.-Y. Chen, X. Peng and S. Yu, Arizona State University*

NeuroSim+ is an integrated simulation framework for benchmarking synaptic devices and array architectures in terms of the system-level learning accuracy and hardware performance metrics. It has a hierarchical organization from the device level (transistor technology and memory cell models) to the circuit level (synaptic array architectures and neuron periphery) and then to the algorithm level (neural network topologies). In this work, we study the impact of the "analog" eNVM non-ideal device properties and benchmark the trade-offs of SRAM, digital and analog eNVM based array architectures for online learning and offline classification.

2:00 PM
6.2 Ferroelectric FET Analog Synapse for Acceleration of Deep Neural Network Training, *M. Jerry, P.-Y. Chen*, J. Zhang, P. Sharma, K. Ni, S. Yu* and S. Datta, University of Notre Dame, * Arizona State University*

We experimentally demonstrate a FeFET analog synapse based on partial polarization switching in HZO for acceleration of on-chip learning in neural networks. The symmetric 5-bit potentiation and depression characteristics of the FeFET synapse results in 90% accuracy for image recognition after training on the MNIST database. Further, the 75ns experimental programing pulse width improves training time on 1M images by 1000× compared to demonstrated RRAM devices while maintaining a 10× area advantage over SRAM.

2:25 PM
6.3 Random Sparse Adaptation for Accurate Inference with Inaccurate Multi-level RRAM Arrays, *A. Mohanty, X. Du, P.-Y. Chen, J.-s. Seo, S. Yu and Y. Cao, Arizona State University*

This work proposes Random Sparse Adaptation (RSA) to efficiently recover the accuracy due to RRAM variations. RSA integrates a small, accurate on- chip memory with the main, inaccurate RRAM array. It completely eliminates Write of RRAM, achieving 10-100X speedup in MNIST and CIFAR-10, and >10% accuracy enhancement.

2:50 PM *Coffee Break*

3:15 PM
6.4 Time-Dependent Variability in RRAM-based Analog Neuromorphic System for Pattern Recognition, *J. Kang, Z. Yu, L. Wu, Y. Fang, Z. Wang, Y. Cai1*, Z. Ji, J. Zhang**, R. Wang, Y. Yang and R. Huang, Peking University, *National Key Laboratory of Science and Technology on Micro/Nano Fabrication, **Liverpool John Moores University*

For the first time, this work investigated the time-dependent variability (TDV) in RRAMs and its interaction with the RRAM-based analog neuromorphic circuits for pattern recognition. It is found that even the circuits are well trained, the TDV effect can introduce non-negligible recognition accuracy drop during the operating condition. The impact of TDV on the neuromorphic circuits increases when higher resistances are used for the circuit implementation, challenging for the future low power operation. In addition, the impact of TDV cannot be suppressed by either scaling up with more synapses or increasing the response time and thus threatens both real-time and general-purpose applications with high accuracy

requirements. Further study on different circuit configurations, operating conditions and training algorithms, provides guidelines for the practical hardware implementation.

3:40 PM

6.5 Fast, Energy-Efficient, Robust, and Reproducible Mixed-Signal Neuromorphic Classifier Based on Embedded NOR Flash Memory Technology, *X. Guo, F. Merrikh-Bayat, M. Bavandpour, M. Klachko, M. R. Mahmoodi, M. Prezioso, K. K. Likharev*, and D. B. Strukov, UC Santa Barbara, * Stony Brook University*

We describe a prototype mixed-signal neuromorphic network with 100K+ floating-gate memory cells, redesigned from a commercial 180-nm NOR flash memory. The circuit can perform reliably and reproducibly classification of MNIST benchmark set images with ~95% fidelity and record-breaking sub- 1-µs time delay and sub-20 nJ energy consumption per pattern.

4:05 PM

6.6 Design Guidelines of Stochastic Computing Based on FinFET: A Technology-Circuit Perspective, *Y. Zhang, R. Wang, X. Jiang, Z. Lin, S. Guo, Z. Zhang, Z. Zhang and R. Huang, Peking University*

Stochastic computing (SC) is a promising alternative to conventional deterministic computing, which enables ultralow power, high error-tolerance and massive parallelism, but not requiring new devices. In this paper, the feasibility of SC circuits based on state-of-the-art FinFET technology are investigated for the first time, with on-chip image processing application as an example. Practical technical issues are carefully examined, including static and transient device variations in 16/14nm FinFET. SC design optimization procedure is also proposed, which can considerably decrease its energy consumption without the penalty of accuracy. The results provide helpful guidelines for energy-efficient stochastic circuit design in new-paradigm computing.

Session 7: Characterization, Reliability and Yield - Reliability of Advanced Devices

Monday, December 4
Continental Ballroom 6
Co-Chairs: Hideki Aono, Renesas Electronics Corporation
Paul K. Hurley, Tyndall National Institute

1:35 PM

7.1 Complete degradation mapping of stacked gate-all-around Si nanowire transistors considering both intrinsic and extrinsic effects, *A. Chasin, E. Bury, B. Kaczer, J. Franco, P. Roussel, R. Ritzenthaler, H. Mertens, N. Horiguchi, D. Linten, A. Mocuta, imec*

We assess the degradation of stacked Silicon Gate- All-Around (GAA) Nanowire (NW) nFETs in the full {VG,VD} bias space. We perform extensive characterization to separate the intrinsic (i.e. the various degradation modes) from extrinsic effects (i.e., parasitic FETs and source/drain series resistance). The modelling of the degradation includes various channel hot-carrier (CHC) modes as well as PBTI and allows an extrapolation to 10-years lifetime in the full bias space. Moreover, by extraction of the activation energies of each of the degradation modes, and by obtaining the thermal resistance by S-parameter measurements, we compensate for any self-heating-induced acceleration or deceleration during overstress. As a result, we obtain a fully intrinsic nGAA-NWFET lifetime map in the entire bias space.

2:00 PM

7.2 New Insights into the Hot Carrier Degradation (HCD) in FinFET: New Observations, Unified Compact Model, and Impacts on Circuit Reliability, *Z. Yu, J. Zhang, R. Wang, S. Guo, C. Liu, R. Huang, Peking University*

In this paper, hot carrier degradation (HCD) in FinFET is studied for the first time from trap-based approach rather than conventional carrier-based approach, with full Vgs/Vds bias characterization and self-heating correction. New HCD time dependence is observed, which cannot be predicted by traditional models. A trap-based HCD compact model is proposed and verified in both n- and p-type FinFETs, which is unified across different Vgs/Vds regions with different carrier transport mechanisms. Impacts of HCD on analog circuits is also demonstrated, showing bias runaway effect. The results provide new insights of HCD in FinFET, which are helpful to circuit design for reliability.

2:25 PM

7.3 Modeling of NBTI Time Kinetics and T Dependence of VAF in SiGe p-FinFETs, *N. Parihar, R. G. Southwick*, M. Wang*, J. H. Stathis** and S. Mahapatra, Indian Institute of Technology Bombay, *IBM Albany, **IBM T. J. Watson Research Center*

NBTI in Replacement Metal Gate (RMG) High-K Metal Gate (HKMG) SiGe p-FinFETs is modeled. Time kinetics for DC and AC stress and recovery, temperature (T) dependence of voltage acceleration factor (VAF), and impact of Ge% and N% are quantified. Benchmarking is done with Si p- FinFETs, and process (Ge%, N%) dependence is explained by TCAD and band structure calculations.

2:50 PM *Coffee Break*

3:15 PM

7.4 Towards Optimal ESD Diodes in Next Generation Bulk FinFET and GAA NW Technology Nodes, *S.-H. Chen, G. Hellings, D. Linten, T. Chiarella, H. Mertens, R. Boschke*, J. Mitard, S. Kubicek, R. Ritzenthaler, E. Bury, N. Wang*, G. Groeseneken*, A. Mocuta and N. Horiguchi, imec, *KU Leuven*

Beyond dimensional scaling, new process options in CMOS roadmap often result in degradation of ESD device performance. Using 3D TCAD and ESD characterization, the impacts of device architecture, middle-of-line contact scheme, and S/D epitaxy process options are explored on ESD diode performance in next generation bulk FF and GAA technologies.

3:40 PM

7.5 Characterization of Oxide Defects in InGaAs MOS Gate Stacks for High-Mobility n-Channel MOSFETs (Invited), *J. Franco, V. Putcha, A. Vais, S. Sioncke, N. Waldron, D. Zhou, G. Rzepa*, Ph. J. Roussel, G. Groeseneken, M. Heyns, N. Collaert, D. Linten, T. Grasser*, B. Kaczer, imec, *TU Wien*

We review our recent studies of oxide traps in InGaAs MOS gate stacks for novel high-mobility n- channel MOSFETs. We discuss and correlate various trap characterization techniques such as Bias Temperature Instability, defect Capture-Emission- Time maps (applied here to InGaAs devices), Random Telegraph Noise, hysteresis traces, multi- frequency C-V dispersion, all performed on a variety of device test vehicles (capacitors, planar MOSFETs, finFETs, nanowires). Finally we demonstrate guidelines for developing sufficiently reliable IIIV gate stacks.

4:05 PM

7.6 Thermal effects in 3D sequential technology, *K. Triantopoulos, M. Cassé, L. Brunet, P. Batude, C. Fenouillet-Beranger, B. Mathieu, M. Vinet, G. Ghibaudo and G. Reimbold, CEA LETI, * IMEP-LAHC*

An experimental study of thermal effects in 3D sequential integration including Self-heating and thermal coupling between the two levels of transistors, using different thermometry techniques and different heater-sensor configurations. This work can be used to manage thermal effects and to further optimize 3DSI circuits through both technology and design solutions.

Session 8: Optoelectronics, Displays and Imagers - Thin Film Transistors and Detectors

Monday, December 4

Continental Ballroom 7-9

Co-Chairs: Arokia Nathan, University of Cambridge

Changhee Lee, Seoul National University

1:35 PM

8.1 Flexible CMOS electronics based on p-type $Ge_2Sb_2Te_5$ and n-type $InGaZnO_4$ semiconductors, *A. Daus, S. Han, S. Knobelspies, G. Cantarella, C. Vogt, N. Münzenrieder*, and G. Tröster, ETH Zürich, *University of Sussex*

Flexible ultra-thin chalcogenide glass Ge2Sb2Te5 (GST) p-type thin-film transistors (TFTs) are investigated. For the first time, GST TFTs show saturating output characteristics. Together with n-type InGaZnO4, 2017 flexible CMOS inverters with a voltage gain of 69 and NANDs are realized. The devices sustain tensile bending to a radius of 6 mm.

2:00 PM

8.2 Highly Robust Oxide Thin Film Transistors with Split Active Semicondcutor and Source/Drain Electrodes, *S. Lee,; D. Geng*, L. Li*, M. Liu* and J. Jang, Kyung Hee University, *University of Chinese Academy of Sciences*

We report extremely stable and high performance etch-stopper a-IGZO TFT on plastic substrate by using split semiconductor and electrodes. The a-IGZO TFTs exhibit high mobility over 70cm2/Vs and extremely stable under bias and mechanical stress. Therefore, this technology can be used for the manufacturing of high resolution flexible AMOLED displays.

2:25 PM

8.3 Manufactured-on-demand steep subthreshold organic field effect transistor for low power and high sensitivity ion and fluorescence sensing, *J. Zhao, Q. Li, Y. Huang, S. Li, W. Tang, S. Peng, S. Chen, W. Liu and X. Guo, Shanghai Jiao Tong University*

A printable device structure design is introduced to fabricate low voltage organic field effect transistor (OFET) of steep subthreshold (80 mV/dec) using thick gate dielectric layers and high throughput printing/coating processes. The device design also bring benefit on excellent bias stress stability. The device is shown to able to be biased in the subthreshold regime with near zero gate voltage for low power and high sensitivity detection of both small H+ concentration (< 10 uW cm-2) changes.

2:50 PM

8.4 Black Phosphorus Carbide Infrared Phototransistor with Wide Spectrum Sensing for IoT Applications, *W. C. Tan, L. Huang, R. J. Ng, L. Wang and K.-W. Ang, National University of Singapore*

We demonstrate a novel black phosphorus carbide (b-PC) phototransistor with a wide absorption spectrum that spans most molecular fingerprints till 8,000 nm and a tunable responsivity and response time at a wavelength of 2,004 nm. The b- PC phototransistor achieves a high responsivity of 2,163 A/W and a short response time of 5.6 ps, showing promise for sensing applications in the coming age of the internet-of-things (IoT).

3:15 PM *Coffee Break*

3:40 PM

8.5 Thermally Stable and Flexible Paper Photosensors Based on 2D BN Nanosheets, *C.-H. Lin, B. Cheng, M.-L. Tsai, H.-C. Fu, W. Luo*, L. Zhou*, S.-H. Jang*, L. -B. Hu and J.-H. He, King Abdullah University of Science and Technology (KAUST), * University of Maryland*

Flexible solar-blind deep-ultraviolet sensors consisting of BN nanosheets show ultrahigh thermal conductivity (146 W/m K), fast recovery-time (0.393 s), and excellent flexibility and bending durability. This shows great potential to be a key electronic component to fully activate flexible electronics for meeting the demand of internet of things.

4:05 PM

8.6 High-Performance, Flexible Graphene/Ultra-thin Silicon Ultra-Violet Image Sensor, *A. Ali, K. Shehzad, H. Guo, Z. Wang*, P. Wang*, A. Qadir, W. Hu*, T. Ren**, B. Yu*** and Y. Xu, Zhejiang University, *Chinese Academy of Sciences, **Tsinghua University, ***State University of New York*

We report a high-performance graphene/ultra-thin silicon metal-semiconductor-metal ultraviolet (UV) photodetector, which benefits from the mechanical flexibility and high-percentage visible light rejection of ultra-thin silicon. The proposed UV photodetector exhibits high photo-responsivity, fast time response, high specific detectivity, and UV/Vis rejection ratio of about 100, comparable to the state-of-the-art Schottky photodetectors

4:30 PM

8.7 Graphene/Silicon-Quantum-Dots/Si Schottky-PN Cascade Heterojunction for Short-Wavelength Infrared Photodetection, *S. Du, Zhenyi Ni, X. Liu, H.Guo, A. Ali, Y. Xu and X. Pi, Zhejiang University*

By taking advantage of the fast photo-carriers transfer between graphene and silicon-quantum- dots, along with infrared tunable Schottky- barrier height of graphene-silicon junction, a novel Schottky- PN cascade heterojunction based

photodetector has been demonstrated. The hyper- boron-doped silicon-quantum-dots, interacting with the graphene-silicon Schottky photodiode, effectively and fast harvest infrared-excited charge-carriers.

Session 9: Power Devices - SiC and GaN Vertical Power Devices
Monday, December 4
Imperial Ballroom A
Co-Chairs: Jun Suda, Nagoya University
Srabanti Chowdhury, UC Davis

1:35 PM
9.1 Body PiN diode inactivation with low on-resistance achieved by a 1.2 kV-class 4H-SiC SWITCH-MOS, *Y. Kobayashi, N. Ohse, T. Morimoto*, M. Kato*, T. Kojima, M. Miyazato, M. Takei, H. Kimura and S. Harada*, Fuji Electric Co., Ltd., *National Institute of Advanced Industrial Science and Technology (AIST)*

We have developed a novel SBD-integrated SiC-MOSFET with small cell pitch, called SWITCH-MOS, to solve body-PiN-diode-related problems known such as forward degradation and reverse recovery loss. The fabricated 1.2 kV SWITCH-MOS successfully inactivated the body-PiN-diode without degradation of on- and off-state characteristics as compared with conventional UMOS.

2:00 PM
9.2 1200 V GaN Vertical Fin Power Field-Effect Transistors, *Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu*, Y. Lin, X. Gao**, K. Shepard*** and T. Palacios, Massachusetts Institute of Technology, *Singapore-MIT Alliance for Research and Technology, **RF LLC, ***Columbia University*

We demonstrate record performance in a novel normally- off GaN vertical transistor with submicron fin-shaped channels. This transistor only needs n-GaN layers. An on-resistance of 0.2 mΩ·cm2, a breakdown voltage over 1200 V and currents up to 10 A have been demonstrated, rendering a figure of merit up to 7.2 GW/cm2.

2:25 PM
9.3 Determination of intrinsic phonon-limited mobility and carrier transport property extraction of 4H-SiC MOSFETs, *M. Noguchi, M. Electric Corporation; T. Iwamatsu, H. Amishiro, H. Watanabe, K. Kita* and S.Yamakawa, Mitsubishi Electric Corporation, *The University of Tokyo*

We determined the intrinsic phonon-limited mobility in the SiC MOSFET, for the first time. Based on this finding, the carrier transport properties of 4H-SiC MOSFETs were experimentally evaluated. The surface roughness scattering does not limit inversion layer mobility in high effective normal field, suggesting the modification of conventional mobility models.

2:50 PM *Coffee Break*

3:15 PM
9.4 Demonstrating >1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices, *D. Ji, Chirag Gupta*, S. H. Chan*, A. Agarwal*, W. Li, S. Keller*, U. K. Mishra* and S. Chowdhury, University of California, Davis, *University of California, Santa Barbara*

A over 1.4 kV normally off (VTH = 4.7 V) vertical GaN OG-FET with a low specific on-state resistance of 2.2 milliohm-cm2 has been successfully demonstrated. The fabricated large- area transistor offered a breakdown voltage of 900 V and an on-state resistance of 4.1 ohm. The average channel electron mobility is 185 cm2/Vs.

3:40 PM
9.5 Progress and Future Challenges of SiC Power Devices and Process Technology (Invited), *T. Kimoto, H. Niwa, N. Kaji, T. Kobayashi, Y. Zhao, S. Mori*, and M. Aketa*, Kyoto University, *ROHM Co., Ltd.*

Recent progress in SiC device physics and development of power devices is reviewed. The authors determined the impact ionization coefficients in the wide temperature range, which enables accurate device simulation of SiC. 13 kV SiC pin diodes with an extremely low on-resistance and 11 kV SiC epitaxial MPS diodes are presented. MOS physics of SiC is also discussed and finally 3 kV reverse-blocking MOSFETs are demonstrated.

4:05 PM

9.6 High Voltage Vertical p-n Diodes with Ion-Implanted Edge Termination and Sputtered SiN_x Passivation on GaN Substrates, *J. Wang, L. Cao, J. Xie*, E. Beam*, R. McCarthy**, C. Youtsey** and P. Fay, University of Notre Dame, *Qorvo Inc., **MicroLink Devices Inc.*

High-voltage vertical GaN-on-GaN diodes with Baliga figure of merit of 13.5 GW/cm2 are demonstrated in a simple implant-termination process flow. Measured breakdown voltage (Vbr) exceeding 1.2 kV, forward current above 8 kA/cm2, and Ron as low as 0.11 mΩcm2 are obtained. The devices do not require field plates or complex edge terminations to achieve material-limited performance.

Session 10: Focus Session - Sensors, MEMS, BioMEMS - Nanosensors for Disease Diagnostics
Monday, December 4
Imperial Ballroom B
Co-Chairs: Séverine Le Gac, University of Twente
Edwin Carlen, University of Tsukuba

1:35 PM

10.1 Nanofluidics for cell and drug delivery (Invited), *N. D. Trani, A. Grattoni, M. Ferrari, Houston Methodist*

Management of chronic pathologies requires the development of novel strategies for the delivery of drugs and cell therapies, ad hoc. We have developed implantable micronanofluidic-based platforms that leverage molecular nanoconfinement for the controlled administration of drugs and transplantation of cells. These rely on silicon nanofabricated membranes and 3D-printed polymeric architectures that afford long term function in vivo without complex pumping mechanisms or actuation. In this work, we present our recent advances in zero-order drug delivery implants, remotely tunable delivery devices, and subcutaneous encapsulations for endocrine cells transplantation.

2:00 PM

10.2 Development of High-frequency Bulk Acoustic Wave (BAW) Resonators as Biosensors and Bioactuators (Invited), *X. Duan, S. Pan and W. Pang, Tianjin University*

Using of bulk acoustic wave resonators for biosensing applications grows rapidly in recent years. In this review, we summarized the recent trend developing of these devices for biodetection from two aspects: 1) as biosensors to provide label- free measurement of biomarkers. 2) as bioacutuators to manipulate biomolecules and enhance biosensing performance.

2:25 PM

10.3 A Single Bacterium and Mammalian Cell Analysis by Ionic Current Measurements in a Microchannel (Invited), *N. Kaji, M. Sano, S. Ito, H. Yasaki, T. Yasui, H. Yukawa, and Y. Baba, Nagoya University*

A microfluidic device based on ionic current detection system for high-throughput and practical single bacteria and mammalian cell sizing was developed, and furthermore, discrimination of bacterial species and mammalian cell deformability was achieved. The highly precise sizing system based on blocking ionic current at narrow microchannel provided the information on antibiotic resistant strains of bacteria. Deformability changes associated with passage of adipose tissue- derived stem cells (ASCs) were also successfully detected by the device without any chemical or biological modification.

2:50 PM

10.4 Rapid Antibiotic Susceptibility Testing System: Life Saving bioMEMS Devices (Invited), *H. Y. Jeong, E.-G. Kim*, S. Han*, G. Y. Lee, S. Han*, B. Jin*, T. Lim, H. C. Kim**, T. S. Kim**, D. Y. Kim* and S. Kwon, Seoul National University, *Quantamatrix Inc, **Seoul National University Hospital*

For the prompt prescription of patients suffering from infectious diseases such as tuberculosis or bloodstream infection, a rapid antimicrobial susceptibility test (RAST) is highly necessary. This paper describe rapid antibiotic susceptibility test system composed of biochips and automated expert system, which can determine the antibiotic susceptibility of bacteria and mycobacteria derived from various parts of body. With RAST, antibiotic susceptibility was available in six hours, which

was conventionally taking more than two days. Device design consideration, clinical verification, commercialization, and application of RAST system to infectious diseases are reviewed.

3:15 PM *Coffee Break*

3:40 PM
10.5 Microscale Profiling of Circulating Tumor Cells(Invited), *R. Mohamadi and S. Kelley, University of Toronto*

Microscale analysis has facilitated significant progress towards the development of approaches that enable the capture of rare circulating tumor cells (CTCs) from the blood of cancer patients. This is a critical capability for noninvasive tumor profiling. These advances have allowed the capture and enumeration of CTCs with unique sensitivity. However, it has become clear that simply counting tumor cells cannot provide the information that could help to make significant clinical decisions. CTCs are heterogeneous and they can change as they enter the bloodstream. Therefore, profiling of CTCs at single cell level is critical to unraveling the complex and dynamic properties of these potential cancer markers. In this paper we discuss new nanoparticle-enabled microscale technologies for CTC characterization, developed in our laboratory, which profiles CTCs based on their surface expression profile. Validation data presented here show that cancer cells with varying surface expression generate different binning profiles. We then applied the new technologies to reveal the dynamic phenotypes of CTCs in unprocessed blood from animal models. We will also discuss the application of these technologies in analyzing blood samples from cancer patients. While most technologies developed for analyzing CTCs are based on microscopic imaging we have developed and integrated new electrochemical sensors with our CTC capture strategies that enabled us to gather further molecular information on these rare cells.

4:05 PM
10.6 Encapsulated Organoids & Organ-on-a-chip platform for cancer modeling (Invited), *N. Picollet-D'hahan, B. Laperrousaz, S. Porte,P. Obeid, A. Tollance, F. Kermarrec, C. Belda-Marin*, A. Romero-Millan, V. Haguet, D.K. Martin* and X. Gidrol, University Grenoble Alpes, INSERM, CEA, BIG, *TIMC-IMAG / CNRS UMR*

This review highlights our major developments in the fields of organoids and organ-on-chip to address issues in fundamental and biomedical research by modeling development and cancer. We illustrate how contemporary miniaturized technologies (e.g. microfluidics, 3D scaffolding, 3D imaging) combined with RNAi-based organoids HTS (High-Throughput Screening), would help forming and analyzing consistent, efficient and reproducible organoids. Moreover, we illustrate the potential of engineered organ-on-chip devices for creating novel human organ and disease models, with a particular focus on "prostate-on-a chip" developments.

4:30 PM
10.7 Tissue Microenvironment and Cellular Imaging (Invited), *S.S. Nasseri, S.M. Grist, S. Chen, Y.Y. Tam, P. Cullis, and K.C. Cheung, University of British Columbia*

Small tissue constructs comprising several cell types within a three-dimensional environment can better mimic tissue, and may provide a better system to screen and validate drugs than current two-dimensional monolayer cultures. We developed a microfluidic flow-focusing method to rapidly and reproducibly create multicellular, 3-D spheroids that can better model several aspects of the tumour in vivo, including diffusion gradients of O2 and drugs. When evaluating effects of drugs on arrays of micro-tissues in high content screening, we will need to image deep within the tissues to assess parameters such as cell viability at the tissue cores or drug penetration into the tissue as a function of time. We have developed an on-chip method to rapidly clear arrays of 3-D cell cultures and micro-tissues, compatible with two-photon microscopy to track drug and nanomedicine penetration into the tissues.

Session 11: Focus Session - Memory Technology - Modelling Challenges for Neuromorphic Computing
Tuesday, December 5
Grand Ballroom A
Co-Chairs: Denis Rideau, STMicroelectronics
Meng-Fan Chang, National Tsing Hua University

9:05 AM

11.1 Stochastic Synapses as Resource for Efficient Deep Learning Machines (Invited), *E. Neftci, University of California, Irvine*

Synaptic unreliability was shown to be a robust and sufficient mechanism for inducing the stochasticity in biological and artificial neural network models. Previous work demonstrated multiplicative noise (also called dropconnect) as a powerful regularizer during training. Here, we show that always-on stochasticity at networks connections is a sufficient resource for deep learning machines when combined with simple threshold non-linearities. Furthermore, the resulting activity function exhibits a self-normalizing property that reflects a recently proposed "Weight Normalization" technique, itself fulfilling many of the features of batch normalization in an online fashion. Normalization of activities during training can speed up convergence by preventing so-called internal covariate shift caused by changes in the distribution of inputs as the parameters of the previous layers are trained. Collectively, our findings can improve performance of deep learning machines with fixed point representations and argue in favor of stochastic nanodevices as primitives for efficient deep learning machines with online and embedded learning capabilities.

9:30 AM
11.2 Attractor networks and associative memories with STDP learning in RRAM synapses (Invited), *V. Milo, D. Ielmini and E. Chicca*, Politecnico di Milano and IU.NET, *Bielefeld University*

Attractor networks can realistically describe neurophysiological processes while providing useful computational modules for pattern recognition, signal restoration, and feature extraction. To implement attractor networks in small-area integrated circuits, the development of a hybrid technology including CMOS transistors and resistive switching memory (RRAM) is essential. This work presents a summary of recent results toward implementing RRAM-based attractor networks. Based on realistic models of HfO_2 RRAM devices, we design and simulate recurrent networks showing the capability to train, recall and sustain attractors. The results support the feasibility of RRAM-based bio-realistic attractor networks.

9:55 AM
11.3 Energy use constrains brain information processing (Invited), *M. Conrad, E. Engl* and R. B. Jolivet, University of Geneva, *Lodestar Insights*

The brain is an energetically expensive organ to build and operate, and a large body of literature links the evolutionary development of many of the human brain's components to the need to save energy. We, and others, have shown experimentally and through computational modelling that synapses in the brain do not maximise information transfer, but instead transfer information in an energetically efficient manner. Strikingly, this optimum implies a high failure rate in the transmission of individual information-carrying signals (action potentials or spikes). This design principle may be important when considering trade-offs between energy use and information transfer in man-made devices.

10:20 AM
11.4 Understanding the Trade-offs of Device, Circuit and Application in ReRAM-based Neuromorphic Computing Systems (Invited), *B. Yan, C. Liu*, X. Liu**, Y. Chen and H. Li, Duke University, *Clarkson University, **AMD, Sunnyvale*

ReRAM technology demonstrates great potential in the development of neuromorphic computing systems. This paper discusses the importance of the comprehensive understanding across the device, circuit, and application levels in ReRAM-based neuromorphic system, through the discussion of three major problems—weight mapping, reliability, and system integration.

10:45 AM *Coffee Break*

11:10 AM
11.5 Device and circuit optimization of RRAM for Neuromorphic computing (Invited), *H. Wu, P. Yao, B. Gao, W. Wu, Q. Zhang, W. Zhang, N. Deng, D. Wu, H.-S. P. Wong*, S. Yu**, and H. Qian, Tsinghua University, *Stanford University, **Arizona State University*

RRAM is a promising electrical synaptic device for efficient neuromorphic computing. The device structure and materials stack were optimized to achieve reliable bidirectional analog switching behavior. A human face recognition task was

demonstrated on a 1k-bit 1T1R RRAM array using an online training perceptron network. A binarized-hidden-layer (BHL) circuit architecture is proposed to minimize the needs of A/D and D/A converters required between RRAM crossbars. Several non-ideal RRAM characteristics were carefully evaluated for handwritten digits' recognition task with proposed BHL architecture and modified neural network algorithm.

11:35 AM
11.6 Challenges and Opportunities toward Online Training Acceleration using RRAM-based Hardware Neural Network (Invited), *C.-C. Chang, J.-C. Liu, Y.-L. Shen, T. Chou, P.-C. Chen, I-T. Wang, C.-C. Su, M.-H. Wu, B. Hudec, C.-C. Chang, C.-M. Tsai, T.-S. Chang, H.-S. P. Wong*, and T.-H. Hou, National Chiao Tung University, *Stanford University*

This paper highlights the feasible routes of using resistive memory (RRAM) for accelerating online training of deep neural networks (DNNs). A high degree of asymmetric nonlinearity in analog RRAMs could be tolerated when weight update algorithms are optimized with reduced training noise. Hybrid- weight Net (HW-Net), a modified multilayer perceptron (MLP) algorithm that utilizes hybrid internal analog and external binary weights is also proposed. Highly accurate online training could be realized using simple binary RRAMs that have already been widely developed as digital memory.

12:00 PM
11.7 Multiscale modeling of neuromorphic computing: from materials to device operations (Invited), *L. Larcher, A. Padovani* and V. Di Lecce*, University of ModenaReggio Emilia, *MDLSoft Inc.*

In this paper, a multiscale modeling platform for neuromorphic computing devices connecting the atomic material properties to the electrical device performances is presented. The main ingredients of the modeling platform are discussed in view of the different technologies (e.g. RRAM, PCM, FTJ) proposed for 3D integrated neuromorphic computing.

Session 12: Circuit and Device Interaction - Circuit-Device Challenges in More Moore and More than Moore
Tuesday, December 5
Grand Ballroom B
Co-Chairs: Greg Yeric, ARM
James Chen, TSMC

9:05 AM
12.1 Twin Mode NV Logic Gates for High Speed Computing System on 16nm FINFET CMOS Logic Process, *W.-Y. Chien, T.-M. Wang, Y.-D. Chih*, J. Chang*, C. J. Lin, Y.-C. King, National Tsing Hua University, *Taiwan Semiconductor Manufacturing Company*

A twin-mode non-volatile logic gates allowing multiple logic functions to be obtained by controlling its non-volatile states is proposed for the first time. This floating metal gate based cell consisting of an inverter controlled by slot contact inputs is successfully demonstrated by standard FinFETs processes in a 16nm technology node. This new twin-mode gates can not only enable reconfiguration capability for logic systems at a gate level, but also prompt the realization of tunable ring oscillators, for multi-functional IOT applications.

9:30 AM
12.2 A Novel PUF Against Machine Learning Attack: Implementation on a 16 Mb RRAM Chip, *Y. Pang, H. Wu, B. Gao, D. Wu, A. Chen*, H. Qian, Tsinghua University, *Semiconductor Research Corporation*

Physical unclonable function (PUF) is an important hardware security primitive. This paper proposes a novel PUF design based on a double-layer RRAM array architecture and digital RRAM programming achieved by splitting resistance distribution after a continuous distribution was formed. The proposed PUF was implemented on a 16 Mb RRAM test chip and its randomness was verified with NIST test suite. The experimental results demonstrate strong reliability and significantly enhanced resistance against machine learning attack of this novel PUF design.

9:55 AM
12.3 Large-Scale Terahertz Active Arrays in Silicon Using Highly-Versatile Electromagnetic Structures (Invited), *C. Wang, Z. Hu, G. Zhang, J. Holloway and R. Han, Massachusetts Institute of Technology*

The high integration capability of silicon technologies, as well as the small wavelength of terahertz (THz) signals, make it possible to build a high-density, very-large-scale active THz array on a single chip. This is, however, very challenging in practice, due to the low device efficiency and large footprint of conventional circuit designs. To address these problems, we introduce a set of compact while versatile circuits, which utilize the multi-mode behaviors from structures with tight device-electromagnetic integration. These circuits have enabled large-scale (1) homogeneous arrays for high-power, collimated radiation, and (2) heterogeneous arrays for fast broadband spectral scanning. In particular, 0.1-mW power generation (20-mW effective isotropically-radiated power) at 1 THz, simultaneous transmit/receive capability, and high-parallelism molecular spectroscopy are demonstrated. New opportunities that these works bring about are also discussed.

10:20 AM *Coffee Break*

10:45 AM

12.4 Variability- and Reliability-Aware Design for 16/14nm and Beyond Technology (Invited), *R. Huang1, X. B. Jiang, S. F. Guo, P. P. Ren, P. Hao, Z. Q. Yu, Z. Zhang, Y. Y. Wang, R. S. Wang, Peking University*

Device variability and reliability are becoming increasingly important for nano-CMOS technology and circuits, due to the shrinking circuit design margin with the downscaling supply voltage (Vdd). Therefore, robust design should have the awareness of both variability and reliability. In FinFET technology, strong correlation between the variations of device electrical parameters is found, due to the larger impacts of line-edge roughness (LER) in FinFET structure. Accurate compact models and new design methodology for random variability in FinFETs were proposed for the variation- and correlation-aware design. For the reliability awareness, the impacts of BTI-induced temporal shift and the layout dependent aging effects should be taken into account for the optimization of end-of- life (EOL) performance/power/area (PPA). New-generation aging model and circuit reliability simulator for FinFETs were proposed and developed in industry-standard EDA tools. Future challenges are also pointed out, such as statistical BTI and RTN. The results are helpful for the robust and resilient design for 16/14nm and beyond.

11:10 AM

12.5 A Novel Bit-Level Characterization Methodology to Benchmark The FinFET based SRAM Performance Under The Influence of Leakage Current, *J.C. Liu, S. Mukhopadhyay, Y.F. Wang, Y.S. Tsai, S.C. Chen, J.H. Lee, Ryan Lu, Y.-H. Lee, and J. He, Taiwan Semiconductor Manufacturing Company*

Leakage current due to intrinsic or extrinsic device failure can severely impact the 6-T SRAM performance. This study introduces a 'Pseudo- Leakage' current source in the SRAM circuit and takes a pragmatic approach to analyze the possible impact on the overall SRAM performance matrices which are affected by such leakage issues.

11:35 AM

12.6 TSV-free FinFET-based Monolithic $3D^+$-IC with Computing-in-Memory SRAM Cell for Intelligent IoT Devices, *F.-K. Hsueh, H.-Y. Chiu*, C.-H. Shen, J.-M. Shieh, Y.-T. Tang, C.-C. Yang, H.-C. Chen, W.-H. Huang, B.-Y. Chen, K.-M. Chen, G.-W. Huang,W.-H. Chen*, K.-H. Hsu*, S. .R Srinivasa**, N. Jao**, A. Lee***, H. Lee***, V. Narayanan**, K.-L. Wang***, M.-F. Chang* and W.-K. Yeh,*
*National Nano Device Laboratories, *National Tsing Hua University, **The Pennsylvania State University, ***University of California at Los Angeles*

This paper presents the first monolithic 3D vertical cross-tier computing-in-memory (CIM) SRAM cell fabricated using low cost TSV-free FinFET- based 3D+-IC technology. The 9T 3D CIM SRAM cell is able to compute NAND/AND, OR/NOR and XOR/XNOR operations within a single memory cycle. We fabricated stackable multi-fin single-grained Si FinFET using low thermal-budget CO2 far-infrared laser annealing (FIR-LA) for activation and self- aligned silicide. The proposed device achieved high Ion (320 uA/um (n-FET) and 275 uA/u□m (p-FET)) and high Ion/Ioff (>107). The proposed scheme enables the fabrication of energy and area efficient circuits for cost-aware intelligent IoT devices. For proposed 9T CIM SRAM cell, the monolithic 3D device reduces area overhead by 51%, compared to the 2D version, thanks to the stacking of three additional transistors above the 6T SRAM cell.

Session 13: Modeling and Simulation - Modeling and Simulation of Advanced CMOS Transistors
Tuesday, December 5
Continental Ballroom 1-3

Co-Chairs: Geert Eneman, imec
Lee Smith, Synopsys

9:05 AM
13.1 Hot-Carrier Degradation in FinFETs: Modeling, Peculiarities, and Impact of Device Topology, *A. Makarov, S. Tyaginov, B. Kaczer*, A. Chasin*, A. Grill, G. Hellings*, M. Vexler**, D. Linten* and T. Grasser, Vienna Technical University, *imec, **A.F. Ioffe Inst.*

We perform a comprehensive analysis of hot- carrier degradation (HCD) in FinFETs. To accomplish this goal we employ our physics-based HCD model and validate it against experimental data acquired in n-FinFETs with a channel length of 28 nm. We use this verified model to study the distribution of the trap density across the fin/stack interface. The methodology is applied to analyze the effect of transistor architectural parameters, namely fin length, width, and height, on HCD. Our results show that at the same conditions HCD becomes more severe in shorter devices and in transistors with wider fins, while the impact of the fin height on the damage is weak. Finally we demonstrate that a proper HCD description can be achieved only with a physics- based model.

9:30 AM
13.2 Performance comparison for FinFETs, Nanowire and Stacked Nanowires FETs: Focus on the influence of Surface Roughness and Thermal Effects, *O. Badami, F. Driussi, P. Palestri, L. Selmi, and D. Esseni, University of Udine*

We perform a comprehensive comparison of FinFETs, stacked nanowires (stacked NWs), circular and square gate-all-around (GAA) *n*-FETs with same footprint, by using an in-house deterministic BTE solver accounting for quantum confinement, a wide set of scattering mechanisms and self-heating. We show that an increase in surface roughness (SR) can frustrate the improvement in on current, I*on*, that for high-quality interfaces we observe in stacked NWs compared to FinFETs. Simulations suggest that SR also influences whether or not In0.53Ga0.47As can provide better I*on* than strained silicon (sSi).

9:55 AM
13.3 Monte Carlo Benchmark of $In_{0.53}Ga_{0.47}As$- and Silicon-FinFETs, *F. Bufler, G. Eneman, N. Collaert, A. Mocuta, imec*

Monte Carlo simulation reproducing measured transfer characteristics of FinFETs with LG=20 nm and W=9 nm shows that InGaAs has similar performance as Si for Vdd of 0.5 V. However, ideal InGaAs-FinFETs loose all advantage upon reducing W to 5 nm because of a charge reduction due to n-type channel doping.

10:20 AM *Coffee Break*

10:45 AM
13.4 Modelling nanoscale n-MOSFETs with III-V compound semiconductor channels: from advanced models for band structures, electrostatics and transport to TCAD (Invited), *L. Selmi, E. Caruso, S. Carapezzi*, M. Visciarelli*, E. Gnani*, N. Zagni**, P. Pavan**, P. Palestri, D. Esseni, A. Gnudi*, S. Reggiani*, F.M. Puglisi**, G. Verzellesi**, University of Udine (DPIA), *University of Bologna, **University of Modena e Reggio Emilia*

We review a few state of the art solutions and recent developments to model short channel III-V compound semiconductor n-MOSFETs based on full quantum transport, semiclassical multi-valley / multi-subband transport and TCAD models. The pros and cons of each, and the insights they can deliver, are illustrated with examples from recent technology developments and literature. Areas where improvements and implementations at TCAD level are most necessary are highlighted as well.

11:10 AM
13.5 Ferroelectric Transistor Model based on Self-Consistent Solution of 2D Poisson's, Non-Equilibrium Green's Function and Multi-Domain Landau Khalatnikov Equations, *A. Saha, P. Sharma*, I. Dabo, S. Datta* and S. Gupta, Penn State University, *University of Notre Dame*

We present a physics-based model for FEFETs/ NCFETs without an inter-layer metal between ferroelectric and dielectric in the gate stack. The model self-consistently solves 2D Poisson's equation, NEGF based charge and transport equations, and multi-domain Landau Khalatnikov (LK) equations with the domain interaction term. The proposed simulation

framework captures the variation of FE polarization along the gate length due to non-uniform electric field along the channel. To calibrate the LK equations, we fabricate and characterize 10nm HZO films. Based on the calibrated model, our results highlight the importance of larger domain interaction to boost the benefits of FEFETs with subthreshold swing (SS) as small as ~50mV/decade achieved at room temperature. As domain interaction increases, the characteristics of FEFETs without inter-layer metal approach those of FEFETs with inter-layer metal.

11:35 AM
13.6 A New Framework of Physics-Based Compact Model Predicts Reliability of Self-Heated Modern ICs: FinFET, NWFET, NSHFET Comparison, *W. Ahn, C. Jiang, J. Xu* and M. A. Alam, Purdue University, *Tsinghua University*

Self-heating effects (SHE) has emerged as an unfortunate corollary of confined-gate transistors (e.g. FinFET; Nanowire-FET, NWFET; NanoSheet-FET, NSHFET) needed for electrostatically-robust sub- 10nm ICs [1-3]. The IC-specific SHE reflects increasing thermal resistances (R_th) associated with all three tiers (i.e., transistor, circuit, and system) of the hierarchy. Many groups have developed tier-specific thermal models, which can neither predict the junction temperature (T_J) accurately nor suggest innovative strategies to reduce T_J by identifying/removing thermal bottlenecks in the hierarchy. In this paper, we develop computationally efficient, physics-based compact models for each tier, and then stack them to estimate T_J-dictated performance/reliability of sub-10nm technologies. Specifically, we (i) refine thermal compact model for front-end-of-line (FEOL) level (TCM_F) based on 3D FEM transient thermal simulations; (ii) investigate SHE by BSIM- CMG circuit simulation for ICs with refined FEOL model; (iii) develop a physics-based thermal compact model for back-end-of line (BEOL) interconnects and interposers (TCM_B) by using image charge and effective medium theory (EMT). The TCM_F and TCM_B are then integrated to predict T_j-specific ICs reliability (i.e., NBTI, HCI, EM) for 14, 201710, and 7nm FinFETs, NWFETs, and NSHFETs; and finally (iv) we propose various mitigation strategies using thermal shunts to suppress SHE. Our work demonstrates that NSHFET is a good candidate at sub-10nm nodes considering both lower subthreshold swing (SS) than that of FinFET and better reliability than that of NWFET.

Session 14: Process and Manufacturing Technology - Interconnect Patterning and Memory Integration
Tuesday, December 5
Continental Ballroom 5
Co-Chairs: Hsin-Ping Chen, TSMC
John Dukovic, Applied Materials

9:05 AM
14.1 20 Years of Cu BEOL in Manufacturing, and its Future Prospects (Invited), *D. Edelstein, IBM TJ Watson Research Center*

This year marks the 20th anniversary of IBM's an-nouncement of its impending plans to insert CMOS/Cu BEOL technology into production, and its having shipped the first functional CPU prototypes. The subsequent manufacturing ramp in mid-1998 provided the first commercial IC chips with Cu BEOL. This invited paper covers the timeline of this tech-nology, with its key defining elements, subsequent innova-tions, and likely future directions. The original, basic features of this technology have endured to this day, though with many evolutionary improvements. But now, in its 10th generation of manufacturing, and 12th in research, we are finally seeing changes beyond evolutionary. The replacement of Cu metal for the finest wiring levels may occur over the next 1-3 nodes.

9:30 AM
14.2 Fully Aligned Via Integration for Extendibility of Interconnects to Beyond the 7 nm Node, *B. D. Briggs, C. B. Peethala, D. L. Rath*, J. Lee, S. Nguyen, N. V. LiCausi***, P. S. McLaughlin*, H. You**, D. Sil, N. A. Lanzillo, H. Huang, R. Patlolla, T. Haigh Jr, Y. Xu, C. Park***, P. Kerber*, H. K. Shobha, Y. Kim^, J. Demarest, J. Li, G. Lian**, M. Ali**, C. t Le**, E. T. Ryan***, L. A. Clevenger, D. F. Canaperi, T. E. Standaert, G. Bonilla, and E. Huang, IBM at Albany Nanotech, *IBM T.J. Watson Res. Ctr., **IBM Systems, ***GLOBALFOUNDRIES, ^Samsung Electronics*

A novel fully aligned via (FAV) BEOL integration scheme is demonstrated at 36 nm pitch, with extendibility to beyond the 7 nm node. FAV enables full control of via/line CD and edge placement, which in turn enables essential resistance and reliability benefits for post 7 nm BEOL wiring.

9:55 AM
14.3 All-Carbon Interconnect Scheme Integrating Graphene-Wires and Carbon-Nanotube-Vias, *J. Jiang, J. Kang, J. H. Chu and K. Banerjee, University of California, Santa Barbara*

An "all-carbon" interconnect scheme that integrates horizontal multilayer graphene wires and vertical carbon-nanotube vias is demonstrated for the first time. The hybrid interconnect scheme is shown to surpass copper in terms of performance, energy efficiency, and reliability down to 5-nm node, paving the way for carbon nanomaterials in VLSI technology.

10:20 AM *Coffee Break*

10:45 AM
14.4 Continuing Moore's Law with EUV Lithography (Invited), *B. Turkot, S. Carson and A. Lio, Intel Corp.*

Extreme Ultra-Violet (EUV) lithography, with its exposure wavelength of 13.5nm, offers a compelling alternative to 193nm-immersion lithography, improving imaging resolution and reducing a key contribution to Edge Placement Error (EPE). Recently, significant progress has been made in the development of EUV exposure tools, with source power meeting the roadmap target for EUV insertion1 as well as demonstrating improvements in system availability and infrastructure such as mask blank defectivity, pellicle membrane manufacturing, and EUV photoresist materials. This paper reviews the current status and challenges of EUV lithography for High Volume Manufacturing (HVM).

11:10 AM
14.5 Electron Beam Detection of Cobalt Trench Embedded Voids Enabling Improved Process Control for Middle-Of-Line at the 7nm Node and beyond, *N. Breil, D. Shemesh, J. Fernandez, R. Hung, N. Bekiaris, J. Tseng, M. Naik, J.H. Park, J. Bakke, A. Kumar, K. Nafisi, A. Litman, A. Karnieli, V. Kuchik, A. Wachs, N. Khasgiwale and M. Chudzik, Applied Materials*

Inline detection of embedded voids within Middle- Of-Line (MOL) cobalt metal lines is a major industry gap at 7nm technology node and below, for both developing the new metallization solutions, as well as for monitoring during ramp and production. We present a new non-destructive electron beam cobalt void detection method, leveraging an improved scanning electron microscope (SEM) imaging technique, which enable an accurate detection of voids embedded inside MOL metal trenches. After explaining the potential process mechanisms causing void formation, we introduce the e-beam technique, and demonstrate by simulation and experiments the correlation between the electron signal and the volume and depth of the voids. We conclude this paper by discussing how a defect inspection strategy using a massive metrology approach can lead to a faster and more efficient development of the Cobalt metallization.

11:35 AM
14.6 Improvement of HfO_2 based RRAM array performances by local Si implantation, *M. Barlas, A. Grossi, L. Grenouillet, E. Vianello, E. Nolot, N. Vaxelaire, P. Blaise, B. Traoré, J. Coignus, F. Perrin, R. Crochemore, F. Mazen, L. Lachal, S. Pauliac, C. Pellissier, S. Bernasconi, S. Chevalliez, J.F. Nodin, L. Perniola, E. Nowak, CEA-Leti, Minatec*

A thorough insight of Si implantation in HfO2- based OXRAM is presented, from a material standpoint up to a 4 kbit 1T-1R array. We demonstrate for the first time that local implantation enables switching area localization and significantly decreases forming, set and reset voltages, improves data retention (tails at 3sigma are stable up to 1000 min at 165°C), while not being detrimental for endurance. In particular using low voltage programming conditions (VF < 3V with 100 ns pulses), a memory window of 10 at 3sigma is demonstrated, paving the way to low power OxRAM arrays with lower variability and improved robustness.

Session 15: Nano Device Technology - Negative Capacitance and Other Steep-Slope Devices 1
Tuesday, December 5
Continental Ballroom 6
Co-Chairs: Kuan-Lun Cheng, TSMC
Lars-Erik Wernersson, Lund University

9:05 AM
15.1 14nm Ferroelectric FinFET Technology with Steep Subthreshold Slope for Ultra Low Power Applications, *Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J.Liu, J.Shi, H.J. Kim, R. Sporer, C. Serrao, A.Busquet, P.*

Polakowski, J. Müller*, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, GLOBALFOUNDRIES, *Fraunhofer IPMS*

Doped hafnia ferroelectric layers with thicknesses from 3 to 8nm are integrated into state-of-the-art 14nm FinFET technology without any further process modification. Ferroelectric devices show improved subthreshold slope (as low as 54mV/dec) and Idsat (up to 165% increase). C-V curves show slight ferroelectric hysteresis. For the first time, we show that ring oscillators with ferroelectric devices can operate at frequencies similar to regular dielectrics, while improved subthreshold slope reduces their active power. We also propose a model for ferroelectric MOSFETs that spans both negative (NCFET) and positive (PCFET) ferroelectric capacitance (CFE) devices. By carefully designed capacitance matching ferroelectric devices can provide significant power savings without sacrificing the speed.

9:30 AM
15.2 Perspective of Negative Capacitance FinFETs Investigated by Transient TCAD Simulation, ***H****. Ota, K. Fukuda, T. Ikegami, J. Hattori, H. Asai, S. Migita and A. Toriumi*, *National Institute of Advanced Industrial Science and Technology (AIST),* *The University of Tokyo

The guideline of the ferroelectric material and the device design to deliver the best performance in NC- FinFETs with avoiding the instability of negative capacitance is shown by exploiting newly developed transient TCAD simulation. We discuss that proposed FinFETs are expected to operate at a quarter volt and that they are very promising for future IoT applications.

9:55 AM
15.3 Hysteresis-free Negative Capacitance Germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec, *W. Chung, M. Si, and P. D. Ye*, Purdue University*

In this paper, we report the first hysteresis-free Ge CMOS FinFETs exhibiting sub-60mV/dec subthreshold slope (SS) in both forward/reverse sweeps at room temperature with ferroelectric Hf0.5Zr0.5O2 (HZO) and Al2O3/GeOx. Minimum SS (7mV/dec) is achieved with HZO (10nm) in Ge pFinFET with hysteresis (-4.3V). With scaled HZO (2nm), Ge p- and nFinFET demonstrate SS (forward/reverse) of 56/41 and 43/49 mV/dec respectively with negligible hysteresis (pFinFET:-4mV, nFinFET:17mV).

10:20 AM
15.4 Ge Nanowire FETs with $HfZrO_x$ Ferroelectric Gate Stack Exhibiting SS of Sub-60 mV/dec and Biasing Effects on Ferroelectric Reliability, C.-J. Su, T.-C. Hong*, Y.-C. Tsou**, F.-J. Hou, P.-J. Sung1, M.-S. Yeh, C.-C. Wan***, K.-H. Kao**, Y.-T. Tang, C.-H. Chiu***, C.-J. Wang, S.-T. Chung*, T.-Y. You, Y.-C. Huang, C.-T. Wu, K.-L. Lin. G.-L. Luo, K.-P. Huang^, Y.-J. Lee, T.-S. Chao*, W.-F. Wu, G.-W. Huang, J.-M. Shieh, W.-K. Yeh, and Y.-H. Wang**, National Nano Device Laboratories, *National Chiao Tung University, **National Cheng Kung University, ***National Chiao Tung University, ^Industrial Technology Research Institute

Ge nanowire FETs exhibits SS of 54 mV/dec at room temperature with ferroelectric HfZrOx gate stack. ION/IOFF ratios higher than 107 (p-NWFETs) and 106 (n-NWFETs) are achieved by gate-all-around configuration. Electrical biasing effects on HfZrOx ferroelectric reliability has been investigated. Ge HfZrOx CMOS inverter shows voltage gain of 24.8 V/V.

10:45 AM *Coffee Break*

11:10 AM
15.5 Frequency Dependence of Performance in Ge Negative Capacitance PFETs Achieving Sub-30 mV/decade Swing and 110 mV Hysteresis at MHz, J. Zhou, J. Wu, G. Han, R. Kanyang, Y. Peng, J. Li, H. Wang1, Y. Liu*, J. Zhang*, Q.-Q. Sun*, D. W. Zhang* and Y. Hao, Xidian University, *Fudan University

We report the first investigation of frequency dependence of performance in Ge negative capacitance (NC) pFETs. Ge NC pFET without internal gate achieves sub-30mV/decade SS and 110 mV hysteresis with 1 us pulse measurement. Additionally, device exhibits the gate capacitance peak due to NC effect at frequency up to MHz.

11:35 AM

15.6 Proposal and demonstration of oxide-semiconductor/(Si, SiGe, Ge) bilayer tunneling field effect transistor with type-II energy band alignment, K. Kato, H. Matsui, H. Tabata, M. Takenaka and S. Takagi, The University of Tokyo,

A new concept of bilayer TFET with type-II energy band alignment using oxide-semiconductors and group-IV-semiconductors is proposed, and its potential is clarified by TCAD simulation. TFET operation by using n-ZnO/p-Si and n-ZnO/p-Ge with the remarkably large ON/OFF (>108) and S.S.min of 71 mV/dec have been demonstrated for the first time.

12:00 PM
15.7 Crystal-Oriented Black Phosphorus TFETs with Strong Band-to-Band-Tunneling Anisotropy and Subthreshold Slope Nearing the Thermionic Limit, M. C. Robbins and S. J. Koester, University of Minnesota

We present black phosphorus TFETs with transport directions aligned to the armchair and zigzag crystal orientation. Strong (~10^4) band-to-band- tunneling anisotropy is observed between the two orientations. Furthermore, we observe a subthreshold slope nearing the thermionic limit of 22 mV/dec at 110 K, representing progress towards realizing subthermionic SS in BP-TFETs.

Session 16: Optoelectronics, Displays and Imagers - Image Sensors and Single-Photon Detectors
Tuesday, December 5
Continental Ballroom 7-9
Co-Chairs: Lindsay Grant, Omnivision Technologies
Toshikatsu Sakai, NHK

9:05 AM
16.1 An Experimental CMOS Photon Detector with 0.5e- RMS Temporal Noise and 15µm pitch Active Sensor Pixels, *T. Nishihara, M. Matsumura, T. Imoto, K. Okumura, Y. Sakano, Y. Yorikado, Y. Tashiro, H. Wakabayashi, Y. Oike and Y. Nitta, Sony Semiconductor Solutions Corporation*

This is the first reported non-electron-multiplying CMOS Image Sensor (CIS) photon-detector for replacing Photo Multiplier Tubes (PMT). 15µm pitch active sensor pixels with complete charge transfer and readout noise of 0.5 e- RMS are arrayed and their digital outputs are summed to detect micro light pulses. Successful proof of radiation counting is demonstrated.

9:30 AM
16.2 SOI monolithic pixel technology for radiation image sensor (Invited), *Y. Arai, T. Miyoshi and I. Kurachi, High Energy Accelerator Research Organization (KEK)*

SOI pixel technology is developed to realize monolithic radiation imaging device. Issues of the back-gate effect, coupling between sensors and circuits, and the TID effect have been solved by introducing a middle Si layer. A small pixel size is achieved by using the PMOS and NMOS active merge technique.

9:55 AM
16.3 Back-side Illuminated GeSn Photodiode Array on Quartz Substrate Fabricated by Laser-induced Liquid-phase Crystallization for Monolithically-integrated NIR Imager Chip, *H. Oka, K. Inoue, T. T. Nguyen*, S. Kuroki*, T. Hosoi, T. Shimura and H. Watanabe, Osaka University, *Hiroshima University*

Back-side illuminated single-crystalline GeSn photodiode array has been demonstrated on a quartz substrate for group-IV-based NIR imager chip. Owing to high crystalline quality of GeSn array formed by laser-induced liquid-phase crystallization technique, significantly enhanced NIR photoresponse with high responsivity of 1.3 A/W was achieved operated under back-side illumination.

10:20 AM *Coffee Break*

10:45 AM
16.4 Near-infrared Sensitivity Enhancement of a Back-illuminated Complementary Metal Oxide Semiconductor Image Sensor with a Pyramid Surface for Diffraction Structure, *I. Oshiyama, S. Yokogawa, H. Ikeda, Y. Ebiko, T. Hirano, S. Saito, T. Oinoue, Y. Hagimoto, H. Iwamoto, Sony Semiconductor Solutions Corporation*

We demonstrated the near-infrared (NIR) sensitivity enhancement of back-illuminated complementary metal oxide semiconductor image sensors (BI-CIS) with a pyramid surface for diffraction (PSD) structures on crystalline silicon and deep trench isolation (DTI). The incident light diffracted on the PSD because of the strong diffraction within the substrate, resulting in a quantum efficiency of more than 30% at 850 nm. By using a special treatment process and DTI structures, without increasing the dark current, the amount of crosstalk to adjacent pixels was decreased, providing resolution equal to that of a flat structure. Testing of the prototype devices revealed that we succeeded in developing unique BI-CIS with high NIR sensitivity.

11:10 AM
16.5 Industrialised SPAD in 40 nm Technology, *S. Pellegrini, B. Rae, A. Pingault, D. Golanski*, S. Jouan*, C. Lapeyre** and B. Mamdy*, STMicroelectronics,*TR&D, *CEA-Leti, Minatec*

We present the first mature SPAD device in advanced 40 nm technology with dedicated microlenses. A high fill factor >70% is reported with a low DCR median of 50cps at room temperature and a high PDP of 5% at 840nm. This digital node is portable to a 3D stacked technology.

11:35 AM
16.6 A Back-Illuminated 3D-Stacked Single-Photon Avalanche Diode in 45nm CMOS Technology, *M.-J. Lee, A. R. Ximenes, P. Padmanabhan, T. J. Wang*, K. C. Huang*, Y. Yamashita*, D. N. Yaung* and E. Charbon, Ecole Polytechnique Fédérale de Lausanne (EPFL), *Taiwan Semiconductor Manufacturing Company (TSMC)*

We report on the world's first back-illuminated 3D-stacked single-photon avalanche diode (SPAD) in 45nm CMOS technology. This SPAD achieves a dark count rate of 55.4cps/µm2, a maximum photon detection probability of 31.8% at 600nm, over 5% in the 420-920nm wavelength range, and timing jitter of 107.7ps at 2.5V excess bias voltage and room temperature. To the best of our knowledge, these are the best results ever reported for any back-illuminated 3D-stacked SPAD technology.

Session 17: Compound Semiconductor and High Speed - 1D and 2D III-V Nanoscale MOSFETs
Tuesday, December 5
Imperial Balroom A
Co-Chairs: Erik Lind, Lund University
Alon Vardi, MIT

9:05 AM
17.1 Record Performance Top-down $In_{0.53}Ga_{0.47}As$ Vertical Nanowire FETs and Vertical Nanosheets, *S. Ramesh, Ts. Ivanov*, V. Putcha, A. Alian*, A. Sibaja-Hernandez*, R. Rooyackers*, E. Camerotto**, A. Milenin*, N. Pinna*, S. El Kazzi*, A. Veloso*, D. Lin*, P. Lagrain*, P. Favia*, N. Collaert* and K. De Meyer, KU Leuven, *IMEC, **Lam Research Belgium*

We report high performance, dry etched In0.53Ga0.47As vertical nanowire and nanosheet devices, fabricated using VLSI compatible flow. The device exhibit SSmin = 63mV/dec, ION = 397µA/ µm, GmMAX = 1.6mS/µm and Q = 21. A reliability analysis puts these vertical MOSFETs in line with other IIIV devices with similar gate stack.

9:30 AM
17.2 Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs, *X. Zhao, C. Heidelberger, E. A. Fitzgerald, W. Lu, A. Vardi, and J. A. del Alamo, Massachusetts Institute of Technology*

We present the first sub-10 nm diameter vertical nanowire transistors of any kind in any semiconductor system. These devices are InGaAs MOSFETs fabricated by a top-down approach using reactive ion etching, alcohol-based digital etch and Ni alloyed contacts. Record ON current and peak transconductance are obtained in a 7 nm diameter device. Excellent scaling behavior is observed with performance increasing as the diameter is shrunk down to 7 nm.

9:55 AM
17.3 Sub-100-nm Gate-Length Scaling of Vertical InAs/InGaAs Nanowire MOSFETs on Si, *O.-P. Kilpi, J. Svensson and L.-E. Wernersson, Lund University*

We demonstrate a process to vary the gate-length of vertical InAs/InGaAs MOSFETs on the same sample with high accuracy. The devices have gate-length ranging from 25 to 140 nm. We demonstrate a record vertical MOSFET with gm=2.4 mS/µm and a device with Ion=407 µA/µm at Ioff=100 nA/µm and VDD=0.5V.

10:20 AM
17.4 High Mobility $In_{0.30}Ga_{0.70}As$ MOSHEMTs on Low Threading Dislocation Density 200 mm Si Substrates: A Technology Enabler Towards Heterogeneous Integration of Low Noise and Medium Power Amplifiers with Si CMOS, *S. Yadav, A. Kumar, X. S. Nguyen*, K. H. Lee*, Z. Liu*, W. Xing*, S. Masudy-Panah, K. Lee*, C. S. Tan*, E. A. Fitzgerald*, D.A. Antoniadis*, Y.-C. Yeo and X. Gong, ECE, NUS, *SMART-LEES*

Heterogeneous integration of In0.30Ga0.70As MOSHEMTs and Si-CMOS in 200 mm wafer scale is proposed. HEMT epitaxial layers with threading dislocation density of lower than 2 × 107 cm-2 are demonstrated using MOCVD and an effective mobility of 4900 cm2/V·s at sheet carrier density of 3 × 1012 cm-2 is achieved.

10:45 AM Coffee Break

11:10 AM
17.5 A Scaled Replacement Metal Gate InGaAs-on-Insulator n-FinFET on Si with Record Performance, *H. Hahn, V. Deshpande, E. Caruso*, S. Sant**, E. O'Connor, Y. Baumgartner, M. Sousa, D. Caimi, A. Olziersky, P. Palestri*, L. Selmi*, A. Schenk** and L. Czornomaz, IBM Research GmbH Zürich Laboratory, *University of Udine, **ETH Zurich*

We demonstrate a scaled replacement-metal-gate InGaAs-on-Insulator n-FinFET on Si with Lg = 13 nm and record record ION of 249 µA/µm at fixed IOFF = 100 nA/µm and VD = 0.5 V. A subthreshold swing in saturation of 89 mV/dec and a Ron of 355 Ohm.µm is also achieved. We further investigate the transport mechanisms at play in order to shed light on the contribution from short-channel effects and carrier generation and recombination mechanisms on SS and IOFF, at such a short gate length, using calibrated full 3D and simplified 2D TCAD simulations.

11:35 AM
17.6 Self-Aligned InGaAs FinFETs with 5-nm Fin-Width and 5-nm Gate-Contact Separation, *A. Vardi, L. Kong, W. Lu, X. Cai, X. Zhao, J. Grajal and J. del Alamo, Massachusetts Institute of Technology*

We demonstrate self-aligned InGaAs FinFETs with fin widths down to 5 nm fabricated through a CMOS compatible front-end process. Precision dry etching of the recess cap results in metal contacts that are about 5 nm away from the intrinsic portion of the fin. The new process has allowed us to fabricate devices with undoped fins and compare them with delta-doped fins.

12:00 PM
17.7 10-nm Fin-Width InGaSb p-Channel Self-Aligned FinFETs Using Antimonide-Compatible Digital Etch, *W. Lu, I. P. Roh*, D.-M. Geum*, S.-H. Kim*, J. D. Song*, L. Kong and J. A. del Alamo, Massachusetts Institute of Technology, *Korea Institute of Science and Technology*

We demonstrate the first InGaSb p-channel FinFET with a narrowest fin width of 10 nm, a gate length of 20 nm, and a fin width/channel thickness aspect ratio > 2. To fabricate such devices, a new antimonide-compatible digital etch has been developed. 10 nm Wf transistor exhibits record gm = 160 uS/um and gm/Wf = 704 uS/um, with much improved subthreshold characteristics.

Session 18: Sensors, MEMS, BioMEMS - Bio and Chemical Sensors
Tuesday, December 5
Imperial Ballroom B
Co-Chairs: Melissa Cowan, Intel
Jin-Woo Han, NASA

9:05 AM

18.1 Lab On Skin^{TM}: 3D Monolitically Integrated Zero-Energy Micro/Nanofludics and FD SOI Ion Sensitive FETs for Wearable Multi-Sensing Sweat Applications, *F. Bellando, E. Garcia-Cordero, F. Wildhaber*, J. Longo*, H. Guérin* and A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne, *Xsensio S.A.*

We report the full integration of functionalized ISFETs, a miniaturized reference electrode and passive capillary microfluidics in a wearable, ultralow-power wearable device for continuous real-time monitoring of the wearer's sweat composition. The possibility of selectively sensing specific ions improves the diagnostic capabilities.

9:30 AM
18.2 Skin-like Nanostructured Biosensor System for Non-invasive Blood Glucose Monitoring, *Y. Chen, S. Lu and X. Feng, Tsinghua University*

We present a strategy to design and fabricate a skin-like nanostructured biosensor system. It has nanometer-deposited transducer layer and significant glucose sensitivity. In vivo clinical tests show that the biosensor's response in non- invasive blood glucose sensing is highly correlated to the clinically invasive blood-taking glucose tests.

9:55 AM
18.3 Mechanical-Field-Coupled Thin-Film Transistor for Tactile Sensing with mN Dynamic Force Detection Capability and Wearable Self-Driven Heart Rate Monitoring with µW Power Consumption, *W. Li, A. Rasheed, X. Feng, E. Iranmanesh, K. Wang, H. Ou, J. Chen, S. Deng and N. Xu, Sun Yat-sen University*

We present a mechanical-filed-coupled thin-film transistor (TFT) intended for mechanical sensor applications. We have demonstrated a tactile sensor with high sensitivity that can detect a gentle dynamic touch down to mN and a wearable piezoelectric self-driven heart rate monitoring device with only µW-range power consumption.

10:20 AM Coffee Break

10:45 AM
18.4 Energy-Efficient All Fiber-based Local Body Heat Mapping Circuitry Combining Thermistor and Memristor for Wearable Healthcare Device, *H. Bae, W.-G. Kim, H. Park, S.-B. Jeon, S.-H. Jung*, H. Moon Lee*, M.-S. Kim, I.-W. Tcho, B. C. Jang, H. Im, S.-Y. Choi, S. G. Im and Y.-K. Choi, KAIST, *KIMS*

This study demonstrated a wearable and flexible temperature sensing circuitry for a diagnosis of skin temperature. This system is based on a novel carbon nanotubes (CNTs)-based temperature sensor (CTS) array, built on cotton yarn using a mixture of multi-walled (MW)-CNTs and PDMS (polydimethylsiloxane). To divide and select the unit thermistors, a memristor which operates in the normally-off state was utilized. To construct the memristors, an Al precursor-based solution dip coating method and initiated chemical vapor deposition (iCVD) were employed for the metal electrode and resistive switching layer (RSL), respectively. Using the aforementioned processes, aluminum (Al) electrode and poly (ethylene glycol methacrylate, pEGDMA)-RSL layers were deposited on a cotton yarn backbone. A unit temperature sensor based on the proposed circuitry was fabricated by intersecting the Al/pEGDMA-coated yarns to both sides of the CTS wire, while forming a 1-thermistor and 2- memristor (1T-2M). This architecture exhibited promising performance as a sensor-array system for a fully fabric-based wearable healthcare device.

11:10 AM
18.5 3D Heterogeneous Integrated Monolayer Graphene Si-CMOS RF Gas Sensor Platform, *M. Holt, S. M. Mortazavi Zanjani, M. M. Sadeghi and D. Akinwande, The University of Texas at Austin*

We report the first monolithically integrated Si-CMOS- monolayer-graphene gas sensor, with a minimal number of post-CMOS processing steps, joining two-dimensional material with low latency, low power, low-cost silicon CMOS (Si-CMOS). Heterogeneous integration of Si-CMOS and 2D materials is a step toward enabling future mobile sensor networks for the Internet of Things.

11:35 AM
18.6 Two-Dimensional SnS_2 for Detecting Gases Causing "Sick Building Syndrome", *K. Hayashi, M. Kataoka, H. Jippo, M. Ohfuchi, T. Iwai and S. Sato, Fujitsu Laboratories Ltd. Limited*

Two-dimensional SnS2-based gas sensors were developed. The sensor can detect HCHO, a gas causing "Sick Building Syndrome," with concentrations down to 1ppb. Simulations suggest that sulfur vacancies in SnS2 play a crucial role. Actually, oxygen atoms unexpectedly detached from HCHO can fill the vacancies, lowering the Fermi level of SnS2.

Entrepreners Luncheon

Tuesday, December 5, 12:30 – 2:00 p.m.
Continental 4

Speaker: Courtney A. Gras, Executive Director for Launch League.

Jointly sponsored by IEDM and IEEE Women in Engineering, the Entrepreneurs Lunch will feature Courtney A. Gras, Executive Director for Launch League. A local nonprofit focused on developing a strong startup ecosystem in NE Ohio. The moderator will be Professor Leda Lunardi from North Caroliuna State University.

Biography

Courtney is an engineer by training and an entrepreneur by nature. After leaving her job as a power systems engineer at NASA to work for her own startup company, she discovered a passion for building startup communities and helping technology-focused companies meet their goals.

Courtney co-founded the Akron-based clean energy startup, Design Flux Technologies as an undergraduate student studying Electrical Engineering at the University of Akron. While serving as Chief Operations Officer Courtney was named a “Forbes 30 Under 30” in 2016. She has also been names to the “Top 40 Under 40” in Cleantech by Midwest Energy News and one of Crain’s “Twenty in their 20s”. She also received the Com Ed Female Founder Prize for 2015 through the Clean Energy Challenge.

After spending 7 years with Design Flux Technologies, Courtney decided to fully-commit her career to supporting startups and helping technology companies reach their goals for growth. She does this this through her work as Executive Director for Launch League, a local nonprofit focused on developing a strong startup ecosystem in NE Ohio and her work as a business development consultant for local technology companies.

Courtney loves sharing her stories of founding a cleantech company, especially with young entrepreneurs. She travels around the globe speaking on the topics of entrepreneurship, women in tech, and clean energy at venues such as TEDx Budapest, the Pioneers Festival, the IEEE WIE International Women’s Leadership Conference.

Session 19: Memory Technology - Charge Based Memories and Advanced Memories
Tuesday, December 5
Grand Ballroom A
Co-Chairs: Pei-Ying Du, Macronix International Co., Ltd.
Takeshi Yamaguchi, Toshiba Memory Corporation

2:05 PM
19.1 A 128Gb (MLC)/192Gb (TLC) Single-Gate Vertical Channel (SGVC) Architecture 3D NAND using only 16 Layers with Robust Read Disturb, Long-Retention and Excellent Scaling Capability, *H.-T. Lue, P.-Y. Du, W.-C. Chen, Y.-. Lee, T.-H. Hsu, T.-H. Yeh, K.-P. Chang, C.-C. Hsieh, C. Huang, G.-R. Lee, C.-P. Chen, C.-F. Chen, C.-J. Chiu, Y. J. Chen, W. P. Lu, T. Yang, K.-C. Chen, C.-H. Hung, K.-C. Wang and Chih-Yuan Lu, Macronix International Co., Ltd*

We have successfully developed a 128Gb MLC (or 192Gb TLC) 3D NAND Flash using 16-layer SGVC architecture. The produced memory density is 1.6 Gb/mm2 for MLC or 2.4 Gb/mm2 for TLC (including CMOS peripheral area, spared BL's and blocks). Such memory density is comparable to 48-layer 3D NAND using the popular gate-all-around (GAA) structures. SGVC has the important advantage of much smaller cell size and pitch scaling capability which allows very high-density memory at much lower stacking layer number. SGVC possesses very robust read disturb immunity (>120M read) and long-retention (> 40 years at room temperature) at fresh state that can suppress the very frequent wear-leveling and refresh operations needed for other 3D NAND Flash devices and is very suitable for read-intensive memory. With further stacking/scaling, it is possible to realize low- cost 1Tb single-chip solution at merely 48 layers.

2:30 PM

19.2 Lateral Charge Migration Suppression of 3D-NAND Flash by V_{th} Nearing for Near Data Computing, *K. Mizoguchi, S. Kotaki, Y. Deguchi and K. Takeuchi, Chuo University*

Vth Nearing is proposed to suppress the lateral charge migration and to improve the reliability of 3D TLC NAND flash. By modulating data so that Vth of adjacent cells become close, data-retention errors decrease by 40%. Data-retention time increases by 2.8-times. The proposal is implemented in the SSD controller.

2:55 PM

19.3 Reliability and Scalability of FinFET Split-Gate MONOS Array with Tight Vth Distribution for 16/14nm-node Embedded Flash, *S. Tsuda, T. Saito, H. Nagase, Y. Kawashima, A. Yoshitomi, S. Okanishi, T. Hayashi, T. Maruyama, M. Inoue, S. Muranaka, S. Kato, T. Hagiwara, H. Saito, T. Yamaguchi, M. Kadoshima, T. Maruyama, T. Mihara, H. Yanagita, K. Sonoda, T. Yamashita and Y. Yamaguchi, Renesas Electronics Corporation*

FinFET SG-MONOS array for 16/14nm-node eFlash is successfully operated and tight Vth distribution is confirmed even after retention. Fin structure enables scaling of the control gate and the memory gate, which is found to lead to the improvement of retention characteristics due to reduction of the program/erase carrier mismatch.

3:15 PM *Coffee Break*

3:40 PM

19.4 Advanced memory solutions for emerging circuits and systems (Invited), *B. Giraud, A. Makosiej, R. Boumchedda, N. Gupta, A. Levisse, E. Vianello and J.-P. Noel, University Grenoble Alpes, CEA, LETI, MINATEC*

This paper presents the most recent results of LETI memory circuit design activities to address the increasing memory demand due to emerging nomad markets. We have investigated both volatile and non-volatile memory solutions with different technologies such as 3D CoolCubeTM, TFET and ReRAM.

4:05 PM

19.5 2D Molybdenum Disulfide (MoS_2) Transistors Driving RRAMs with 1T1R Configuration, ***R****. Yang, H. Li, K. K. H. Smithe, T. R. Kim, K. Okabe, E.Pop, J. A. Fan and H.-S. P. Wong, Stanford University*

We demonstrate the first 1-transistor-1-resistor (1T1R) memory cell using the monolayer molybdenum disulfide (MoS2) field-effect transistor (FET) and resistive random access memory (RRAM). This 1T1R demonstration realizes a key milestone for tight integration of memory with logic in a monolithic 3D integrated chip.

4:30 PM

19.6 Engineering of Ferroelectric Switching Speed in Si Doped HfO_2 for High-Speed 1T-FERAM Application, ***H****. K. Yoo, J. S. Kim, Z. Zhu*, Y. S. Choi, A. Yoon*, M. R. MacDonald**, X. Lei**, T. Y. Lee***, D. Lee^, S. C. Chae***, J. Park^, D. Hemker*, J. G. Langan**, Y. Nishi^^^ and S. J. Hong, SK Hynix Inc., *Lam Research Corp., **Versum Materials, ***Seoul Nat. Univ., ^CNR, Institute for Basic Science (IBS), ^^Stanford Univ.*

We propose a control of grain size in Si:HfO2 which would lower the Ec, thereby, increase the switching speed for high speed 1T-FERAM application. We successfully demonstrated that Si:HfO2 consists of controlled nano-grains with a FE property of Ec ~0.5MV/cm, which is a half of the ordinary Si:HfO2, and the domain switching speed reaches ~3 times faster than that of ordinary grain sized Si:HfO2.

4:55 PM

19.7 A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond, *S. Dünkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic*, S. Slesazeck*, S. Müller**, J. Ocker**, M. Noack**, D.-A. Löhr***, P. Polakowski***, J. Müller***, T. Mikolajick*, J. Höntschel, B. Rice, J. Pelleri, and S. Beyer, GLOBALFOUNDRIES Fab1 LLC & Co. KG, *NaMLab gGmbH, **Ferroelectric Memory GmbH, ***Fraunhofer IPMS*

A ferroelectric field effect transistor (FeFET) based eNVM solution for a 22nm FDSOI CMOS technology is presented. Memory windows of 1.5V are demonstrated in aggressively scaled FeFET cells (0.025µm²) with endurance up to 10E5 cycles. Complex pattern are written into 32MBit arrays using ultra-fast program/erase pulses in a 10ns range at 4.2V. High temperature retention up to 300°C is achieved.

Session 20: Circuit and Device Interaction - Path-Forward for Advanced CMOS Scaling
Tuesday, December 5
Grand Ballroom B
Co-Chairs: Anda Mocuta, imec
Yanfeng Wang, Nvidia

2:05 PM
20.1 Overcoming Interconnect Scaling Challenges Using Novel Process and Design Solutions to Improve Both High-Speed and Low-Power Computing Modes, *K. Vaidyanathan, D. H. Morris, U. E. Avci, I. S. Bhati, L. Subramanian, J. Gaur, H. Liu,; S. Subramoney, T. Karnik, H. Wang and I. A. Young, Intel Corporation*

Interconnect scaling in future CMOS technologies is projected to cause an unprecedented increase in resistance, making interconnects the key performance limiter instead of transistors. We present device-circuit-architecture solutions using reconfiguration of buffered interconnects and execution architecture. Combined, these techniques improve performance by 35% and preserve energy efficiency.

2:30 PM
20.2 Impact of Aggressive Fin Width Scaling on FinFET Device Characteristics, *X. He, J. Fronheiser, P. Zhao, Z. Hu, S. Uppal, X. Wu, Y. Hu, R. Sporer, L. Qin, R. Krishnan, E. M. Bazizi, R. Carter, K. Tabakman, A. K. Jha, H. Yu, O. Hu, D. Choi, J. G. Lee, S. B. Samavedam, D.K. Sohn, GLOBALFOUNDRIES*

Fin width scaling is required to improve FinFET electrostatics for future technology nodes. This paper studies the benefits, trade-offs and limitations of aggressive fin width scaling down to 1.6nm on logic and SRAM device characteristics. AC performance boost opportunity from gate length scaling along with fin width scaling is discussed.

2:55 PM
20.3 Design Technology Co-Optimization of 3D-monolithic standard cells and SRAM exploiting dynamic back-bias for ultra-low-voltage operation, *F. Andrieu, R. Berthelon, R. Boumchedda, G. Tricaud, L. Brunet, P. Batude, B. Mathieu, E. Avelar, A. Ayres de Sousa, G. Cibrario, O. Rozeau, J. Lacord, O. Billoint, C. Fenouillet-Béranger, S. Guissi**, D. Fried**, P. Morin*, J.P. Noel*, B. Giraud, S. Thuries, F. Arnaud*, M. Vinet, CEA-Leti, *STMicroelectronics, **Coventor*

We have fabricated 3D-monolithic transistors on two tiers. We experimentally evidence the asymmetric double-gate (DG) behavior of a top-tier transistor, resulting in a better ON-state current (ION) / OFF-state current (IOFF) tradeoff than in single-gate (SG) mode. Moreover, a 3D-shared contact between a top and bottom electrode was experimentally demonstrated; paving the way for a local back gate, possibly connected with the top gate by a 3D-shared contact. Assuming such a construct, we have performed extensive layout and spice simulations of standard cells and SRAMs. We evidence that the back-gate overlap on the source and drain must be minimized to mitigate the parasitic capacitances. The best layout configurations of a loaded 1-finger inverter yields a 24% frequency gain at a given static power and VDD=0.6V supply voltage, compared to SG, or to a static power divided by 5, 2017 compared to SG under Forward Body Bias (FBB). These performance boosts may be obtained without any area penalty. Similarly, a 29% improvement of the read and write currents of 6T SRAMs is contemplated at VDD=0.8V. Such new functionality provided by 3D-monolithic even enables making 4T SRAMs that are fully functional at VDD=0.8V by improving their retention and, in turn, the maximum number of bitcells per column from 50 (SG) to 300 with a dynamic back-bias.

3:15 PM *Coffee Break*

3:40 PM
20.4 Power Aware FinFET and Lateral Nanosheet FET Targeting for 3nm CMOS Technology, *D. Yakimets, M. Garcia Bardon, D. Jang, P. Schuddinck, Y. Sherazi, P. Weckx, K. Miyaguchi, B. Parvais, P. Raghavan, A. Spessot, D. Verkest, and A. Mocuta, imec*

We show how 5.5 tracks standard cells can be enabled at gate pitch 42nm and metal pitch 21nm. A device downselection methodology driven by power and performance targets is introduced, demonstrating that three stacked nanosheets are competitive with FinFETs made with two fins while relaxing the constraints on design rules.

4:05 PM

20.5 Stacked nanosheet fork architecture for SRAM design and device co-optimization toward 3nm, *P. Weckx, J. Ryckaert, V. Putcha, A. De Keersgieter, J. Boemmels, P. Schuddinck, D. Jang, D. Yakimets, M. G. Bardon, L. -Å. Ragnarsson, P. Raghavan, R. R. Kim, A. Spessot, D. Verkest, and A. Mocuta1, imec*

This paper discusses SRAM scaling beyond the 5nm technology node and highlights the fundamental scaling limits due to FinFET and Gate all-around (GAA) technology. Therefore, a novel vertically stacked lateral nanosheet architecture using a forked gate structure is proposed showing superior performance and area scaling with limited additional processing complexity.

4:30 PM

20.6 A Novel Performance Model for State-of-the-art Processors by Modernization of Rent's Rule, *D. Prasad, S. Sinha*, B. Cline*, S. Moore* and A. Naeemi, Georgia Institute of Technology, *Arm Inc*

Faithful a priori estimation of system performance has long been the foundation for early device, circuit, and micro-architectural evaluation. For over two decades, Rent's power-law has been a popular modelling methodology for predicting interconnect characteristics of a system. However, with dimensional scaling, interconnects have become increasingly important, and the existing models do not provide accurate interconnect estimates; at worst, current Rent's-based models heavily under-estimate interconnect delay, and power. At the same time, microprocessor designs are also evolving in order to cope with the rapidly changing technology landscape, which together can drastically influence the overall performance characteristics of the designs. For the first time, this paper argues the validity of Rent's method in the era of rapid technology and, microprocessor-design advancements. A new approach to Rent's model is proposed which addresses the inability of the current Rent's approach to accurately capture standard cell level, and design characteristics that are inherent to the way we design microprocessors today. The proposed models are validated against a rich database of state-of-the-art commercial microprocessors at 14/16nm, 10nm and 7nm process nodes, and the results illustrate the importance of design-specific technology prediction.

Session 21: Characterization, Reliability and Yield - Memory Reliability
Tuesday, December 5
Continental Ballroom 1-3
Co-Chairs: Moonyoung Jeong, Samsung
Tanya Nigam, GLOBALFLOUNDRIES

2:05 PM

21.1 Impact of external magnetic field on embedded perpendicular STT-MRAM technology qualified for solder reflow, *C.-Y. Wang, M.-C. Shih, Y.-H. Lee, W. Wang, L. Thomas*, Y.-J. Lee*, H. Liu*, J. Zhu*, G. Jan*, A. Wang*, T. Zhong*, P.-K. Wang*, D. Lin, C.-H. Chen, C.-Y. Chang, C.-H. Weng, T.-W. Chiang, K.-H. Shen, W.-J Gallagher, H. Chuang, TSMC, *TDK*

External magnetic field resistance under write, read operations for perpendicular STT-MRAM qualified for 260oC solder reflow is comprehensively reported for the first time. We show that the most critical polarization direction is writing from parallel to anti-parallel state with external field opposed to both the final free layer direction and the bottom pinned layer direction. It is also found that free layer failure to switch is the major cause rather than unexpected pinned layer flipping. Furthermore, various key factors including temperature, write condition and MTJ film stack are also studied here. Finally, we demonstrate that a low chip failure rate of 0.001 ppm can be achieved with an ECC scheme for external magnetic fields up to 240 Oe at 85oC.

2:30 PM

21.2 Experimental and theoretical verification of channel conductivity degradation due to grain boundaries and defects in 3D NAND, *A. Subirats, A. Arreghini, E. Capogreco, R. Delhougne, C.-L. Tan, A. Hikavyy, L. Breuil, R. Degraeve, V. Putcha, G. Van den bosch, D. Linten and A. Furnémont, IMEC*

In this paper, Epi-Si process is used to investigate the impact of traps and grain boundaries in vertical 3D NAND. With this channel morphology, we show that the defects have a reduced impact on device performances compared to the usual poly-Si channel devices. These results are also confirmed and extrapolated to other geometry using 3D TCAD simulations.

2:55 PM
21.3 Impact of Temperature on the Amplitude of RTN Fluctuations in 3-D NAND Flash Cells, *G. Nicosia, A.Mannara, D. Resnati, G. M. Paolucci*, P. Tessariol*, A. L. Lacaita, A.S.Spinelli, A. Goda*, and C. Monzio Compagnoni, Politecnico di Milano, *Micron Technology Inc.*

We show that the average amplitude of RTN fluctuations in 3-D NAND Flash cells increases when temperature is reduced. This is explained through TCAD simulations in terms of stronger nonuniformities in the polysilicon channel inversion at lower temperatures, increasing the dVT of traps at or close to the polysilicon grain boundaries.

3:15 PM *Coffee Break*

3:40 PM
21.4 RTN based Oxygen Vacancy Probing Method for Ox-RRAM Reliability Characterization and Its Application in Tail Bits, *P. Huang, D. B. Zhu, C. Liu, Z. Zhou, Z. Dong, H. Jiang, W. S. Shen, L. F. Liu, X. Y. Liu*, and J. F. Kang, Peking University & National Key Laboratory of Science and Technology on Micro/Nano Fabrication*

Physical mechanism for Random-telegraph-noise (RTN) in oxide based resistive switching memory (Ox-RRAM) is proposed with new insight that the noticeable current fluctuation is attributed to the activation and deactivation of oxygen vacancy (VO) in the filament gap region. Based on the mechanism, RTN based VO probing method is first proposed to analyze properties of each VO and detect the VO count in the filament gap region. The proposed method can establish a connection between the microcosmic VO properties and the Ox-RRAM reliability. Using the proposed VO probing method, we revealed that the tail bits of high resistance state originate from the redundant VO generation in the filament gap region in the ineffective RESET phase. Furthermore, an optimized operation scheme is presented to suppress the tail bits.

4:05 PM
21.5 Fundamental limitations of existing models and future solutions for dielectric reliability and RRAM applications (Invited), *E. Wu, A. Kim, T. Ando, R. Muralidhar, B. Li, R. Southwick, P. Jamison, T. Shaw, J. Stathis, and G. Bonilla IBM Research Div.*

Two important engines lie at the heart of dielectric reliability assessment and prediction methodologies: a statistical distribution model and a field/voltage accelera-tion model for data parameter extraction and reliability projection. The Weibull/ Poisson model and constant field-acceleration E-model are useful for more-or-less ideal situations, but new applications and experimental findings have challenged and exposed the fundamental limitations of these decades-old models. The time-dependent clustering model and power-law field/voltage models have emerged as promising solutions to meet these new challenges in a wide range of applications from dielectric breakdown (BD) statistics in BEOL/ MOL/FEOL cases to Reset/Set statistics of RRAM opera-tions. Recent advances in atomistic simulation and mi-croscopic modeling provide fresh insights for the correct choice of field/voltage acceleration models.

4:30 PM
21.6 Overcoming the Reliability Limitation in the Ultimately Scaled DRAM Using Silicon Migration Technique by Hydrogen Annealing, *S.-W. Ryu, K. Min, J. Shin, H. Kwon, D. Nam, T. Oh, T.-S. Jang, M. Yoo, Y. Kim, S. Hong, SK Hynix Semiconductor Inc.*

We demonstrated a highly reliable buried-gate saddle-fin cell-transistor using silicon migration technique of hydrogen annealing after a dry etch to form the saddle-fin structure in a fully integrated 2y-nm 4Gb DRAM. It clearly shows a reduction in interface trap density with highly enhanced variable-retention-time and Row-Hammering immunity.

Session 22: Process and Manufacturing Technology - Advanced Metal Gate and Contact Technology
Tuesday, December 5
Continental Ballroom 5
Co-Chairs: Qi Xie, ASM
Guilhem Larrieu, LAAS CNRS

2:05 PM
22.1 High-k Metal Gate Fundamental Learning and Multi-V_T Options for Stacked Nanosheet Gate-All-Around Transistor, *J. Zhang, T. Ando, C. W. Yeung, M. Wang, O. Kwon*, R. Galatage**, R. Chao, N. Loubet, B. K. Moon**, R. Bao, Reinaldo A. Vega, J. Li, C. Zhang, Z. Liu, M. Kang*, X. Miao1, J. Wang, S. Kanakasabapathy, V. S Basker, H. Jagannathan, T. Yamashita1, IBM, *SAMSUNG ELECTRONICS, **GLOBALFOUNDRIES*

In this paper, we report multi-threshold-voltage (multi-VT) options for stacked Nanosheet gate-all-around (GAA) transistors. VT can be modulated through workfunction metal (WFM) thickness as well as the inter-nanosheet spacing (Tsus), the combination of which may be leveraged to increase the number of undoped VT offerings within a CMOS device menu relative to a FinFET CMOS device menu, which fundamentally does not have Tsus as a VT tuning option. Hence we propose our multi-VT scheme by taking advantage of the unique structure of stacked GAA transistor.

2:30 PM
22.2 Highly Conductive Metal Gate Fill Integration Solution for Extremely Scaled RMG Stack for 5 nm & Beyond, *N. Yoshida, S. Hassan, W. Tang, Y. Yang, W. Zhang, S. C. Chen, L. Dong, H. Zhou, M. Jin, M. Okazaki, J. Park, N. Bekiaris, R. Hung, J. Zhou, Y. Lei, P. Ma, X. Tang, T. Miyashita, N. Kim and E. Yieh, Applied Materials Inc.*

This paper describes replacement-metal-gate fill integration solutions with a cobalt-reflow process combined with a thin barrier layer for future node FinFET and gate-all-around technology. A unique Co-fill process combined with scaled barrier thickness is proposed as a new RMG solution for gate conductance extendibility and VT control.

2:55 PM
22.3 Integrated Dual SPE Processes with Low Contact Resistivity for Future CMOS Technologies, *Heng Wu, S.-C. Seo, C. Niu*, W. Wang, G. Tsutsui, O. Gluschenkov, Z. Liu, A. Petrescu, A. Carr, S. Choi, S. Tsai*, C. Park*, I. Seshadri, A. Desilva, A. Arceo, G. Yang*, M. Sankarapandian, C. Prindle*, K. Akarvardar*, C. Durfee*, J. Yang, P. Adusumilli, B. Miao, J. Strane, W. Kleemeier*, M. Raymond*, K. Choi, F.-l. Lie, T. Yamashita, A. Knorr*, D. Gupta, D. Guo, R. Divakaruni, H. Bu, and M. Khare, IBM Semiconductor Technology Research, *GLOBALFOUNDRIES Inc*

In this study, a manufacturable CMOS dual solid phase epitaxy (SPE) process with Rhocc < 2.2×10-9 ohm*cm2 on both NFET and PFET is demonstrated on the hardware with 7nm ground rule. Contact resistivity reduction strategies of both the conventional approach of high in-situ doped epi and the novel SPE processes are systematically studied on device and ring oscillator (RO) level. Clear improvement in the RO delay is accomplished by the novel dual SPE process on the CMOS flow. Stronger performance benefit is demonstrated with smaller contact sizes towards future CMOS technology nodes.

3:15 PM *Coffee Break*

3:40 PM
22.4 Comprehensive study of Ga Activation in Si, SiGe and Ge with 5×10^{-10} Ω cm^2 Contact Resistivity Achieved on Ga doped Ge using Nanosecond Laser Activation, *L.-L. Wang, H. Yu, M. Schaekers, J.-L. Everaert, A. Franquet, B. Douhard, L. Date**, J. del Agua Borniquel**, K. Hollar**, F. A. Khaja**, W. Aderhold**, A. J. Mayur**, J.Y. Lee**, H. van Meer**, D. Mocuta, N. Horiguchi, N. Collaert, K. De Meyer, Y.-L. Jiang*, imec, *Fudan University, **Applied Materials*

Ga activation in Si, SiGe and Ge are studied comprehensively. A low Ti/p-Ge contact resistivity of 1.2×10-9 ohmic·cm2 is approached using Ga doping and low temperature activation, while a record-low contact resistivity for p-Ge down to 5×10-10 ohmic·cm2 with high activation level of 5×1020cm-3 is achieved using nanosecond laser activation.

4:05 PM

22.5 Cluster-Preforming-Deposited Amorphous WSi_n (n = 12) Insertion Film of Low SBH and High Diffusion Barrier for Direct Cu Contact, *N. Okada, N. Uchida, S. Ogawa, K. Endo, T. Kanayama, National Institute of Advanced Industrial Science and Technology (AIST)*

The insertion of WSi12 films reduces the SBH to 0.32 eV at W/n-Si and to 0.51 eV at W/Ge/p-Si junctions, and extends a TDDB lifetime > 10 years at 100ºC under 5 MV/cm stress for Cu MOS capacitors, thus enabling the direct Cu contact at S/D in advanced CMOS.

Session 23: Nano Device Technology - Negative Capacitance and Other Steep-Slope Devices 2
Tuesday, December 5
Continental Ballroom 6
Co-Chairs: Deji Akinwande, University of Texas - Austin
Bill Taylor, GLOBALFOUNDRIES

2:05 PM
23.1 Negative Capacitance Enables FinFET and FDSOI Scaling to 2 nm Node, *V. Pi-Ho Hu, P.-C. Chiu, A.B. Sachid*, and C. Hu*, National Central University, *University of California, Berkeley*

The scaling potential of negative capacitance FinFET and FDSOI (NC-FinFET and NC-FDSOI) are studied for technology nodes down to 2nm. According to ITRS 2.0, FinFET scaling ends at 6/5nm node due to the scaling limits of fin width (6 nm Wfin) and FDSOI scaling ends at 11/10 nm due to scaling limit of the channel thickness (3 nm Tch). We present TCAD simulation evidence that using these Wfin and Tch, and negative capacitance enables FinFET and FDSOI scaling to 2 nm node. NC-FinFET and NC-FDSOI at 2 nm node show Ioff < 100nA/um and 10%~29% higher Ion compared with 2nm FinFET(97uA/um Ioff) and FDSOI(46uA/um Ioff). NC-FDSOI exhibits similarly strong back-gate bias effects on Ioff and Ion compared with FDSOI.

2:30 PM
23.2 Energy-Efficient $HfAlO_x$ NCFET: Using Gate Strain and Defect Passivation to Realize Nearly Hysteresis-Free Sub-25mV/dec Switch with Ultralow Leakage, *C.-C.Fan, C.-H. Cheng*, Y.-R. Chen, C. Liu*, and C.-Y. Chang, National Chiao-Tung University, *National Taiwan Normal University*

HfAlOx NCFETs achieve the 8 orders-of-magnitude current ratio. HfAlOx NCFETs with gate strain exhibits 66% Ion enhancement and 27% Vt reduction. The additional defect passivation can mitigate interface depolarization field and help to reinforce surface potential amplification effect.

2:55 PM
23.3 Ferroelectric Al:HfO_2 Negative Capacitance FETs, *M. H. Lee, P.-G. Chen, S.-T. Fan*, Y.-C. Chou, C.-Y. Kuo, C.-H. Tang, H.-H. Chen, S.-S. Gu, R.-C. Hong, Z.-Y. Wang, S.-Y. Chen, C.-Y. Liao, K.-T. Chen**, S. T. Chang**, M.-H. Liao*, K.-S. Li***, and C. W. Liu*, National Taiwan Normal University, *National Taiwan University, **National Chung Hsing University, ***National Nano Device Laboratories*

The first experimental demonstration of ferroelectric Al:HfO2 (FE- HAO) FETs is proceeded with negative capacitance (NC) effect. The SS of 40 mV/dec and 39 mV/dec for forward and reverse sweep, respectively, as well as almost hysteresis-free are achieved. The partial orthorhombic phase of FE-HAO is confirmed both with (PMA) and without (PDA) a capping layer. A gradual transition of polarization after 1000°C annealing is obtained with increasing Al concentration for large remanent polarization (Pr), coercive field (Ec), and high dielectric constant. The similar physical thickness (~7nm) of ferroelectric-HfZrOx (FE-HZO) FET is discussed for comparison. The transient behavior is performed at room temperature and low temperature, and the dynamical NC model is discussed.

3:15 PM *Coffee Break*

3:40 PM
23.4 Physics and Technology of Electronic Insulator-to-Metal Transition (E-IMT) for High On/Off Ratio and Low Voltage in Device Applications, *J. Lin, K. Alam, L. Ocola, Z. Zhang*, S. Data**, S. Ramanathan*, S. Guha, Argonne National Laboratory, *Purdue University, **University of Notre Dame*

We investigate the physics and technology toward realizing both high ON/OFF and low-voltage electronic insulator-to-metal transition (E-IMT) devices. We show that, the ON/OFF ratio, critical E-IMT voltage, and device reliability are closely coupled. A predictive model is developed and shows that, for reliable operation, the maximum ON/OFF ratio of an E-IMT device should follow a square root relation with the strength of the thermally driven insulator-to-metal transition (T-IMT). This new design rule is verified by systematic experiments using prototypical VO2 E-IMT devices. Through this study, we achieve a record value of reliable E-IMT with an ON/OFF ratio of 3.5E3 – greater than 10x improvement over the previous state-of-the-art. A record low voltage of IMT switching at 0.3 V (ON/OFF ratio =20) is also demonstrated. The proposed universal design rule is widely applicable for a range of emerging applications based on E-IMT devices – we demonstrate this with an experimental example of reliable E-IMT based transistors with an ultra- steep subthreshold swing (1E3.

4:05 PM
23.5 Sub-60 mV/dec Ferroelectric HZO MoS_2 Negative Capacitance Field-effect Transistor with Internal Metal Gate: the Role of Parasitic Capacitance, *M. Si, C. Jiang, C.-J. Su*, Y.-T. Tang*, L. Yang, W. Chung, M. A. Alam and P. D. Ye, Purdue University, *National Nano Device Laboratories,*

Steep-slope MoS2 NC-FETs with ferroelectric HZO and IMG are demonstrated. SS less than 50 mV/dec is obtained for both forward and reverse gate voltage sweeps, with minimum SSFor=37.6 mV/dec and SSRev=42.2 mV/dec. The impact of parasitic capacitance on SS and dynamic hysteresis is systematically studied by both experiment and simulation.

4:30 PM
23.6 Negative Capacitance 2D MoS_2 Transistors with Sub-60mV/dec Subthreshold Swing over 6 Orders, 250 µA/µm current density, and Nearly-Hysteresis-Free, *Z. Yu, H. Wang, W. Li, S. Xu, X. Song*, S. Wang, P. Wang, Peng Zhou*, Y. Shi, Y. Chai** and Xinran Wang, Nanjing University, Fudan University, *The Hong Kong **Polytechnic University*

A high-performance and low-power MoS2 NCFET is demonstrated in this work, with ultra-low subthreshold swing (SS) of 23 mV/dec, sub-60 mV/dec over 6 orders of ID, nearly hysteresis-free, small |Vth|

4:55 PM
23.7 NbO_2 based threshold switch device with high operating temperature (>85°C) for steep-slope MOSFET (~2mV/dec) with ultra-low voltage operation and improved delay time, *J. Park, D. Lee, J.M. Yoo and H. Hwang, Pohang University of Science and Technology*

To realize a steep slope field-effect transistor (FET) with low leakage current and controllable operating bias, NbO2 threshold switching (TS) device is connected in series with the gate side of a MOSFET. Thanks to the TS device showing abrupt transition between the OFF and ON states at threshold voltage (Vth), the implemented transistor exhibits extremely low leakage current (10-7µA/ µm), high ION/IOFF ratio (>106), sub-2 mV/dec subthreshold swing, drift-free characteristic and high temperature operation (>85°C). Furthermore, since the Vth is tunable by controlling thickness of the NbO2 TS device, the new NbO2-MOSFET can fulfill various demands of operating bias conditions. In addition, we confirmed through a simulation that the CMOS inverter with NbO2 connected to the gate side showed fast inverting speed of over 300 MHz at ultra-low voltage (200mV).

Session 24: Optoelectronics, Displays and Imagers - Silicon Technology Based Optoelectronics
Tuesday, December 5
Continental Ballroom 7-9
Co-Chairs: Lars Zimmermann, IHP
Boon Ooi, KAUST

2:05 PM
24.1 Hybrid III-V/Si DFB laser integration on a 200 mm fully CMOS-compatible silicon photonics platform, *B. Szelag, K. Hassan, L. Adelmini, E. Ghegin, Ph. Rodriguez, S. Bensalem, F. Nemouchi, T. Bria, M. Brihoum, P. Brianceau, E. Vermande, O. Pesenti, A. Schembri, R. Crochemore, S. Dominguez*, M.C. Roure, B. Montmayeul, L. Sanchez, C. Jany, University Grenoble Alpes, *STMicroelectronics*

We demonstrate the first integration of a hybrid III-V/Si laser in a fully CMOS compatible 200mm technology. Device with SMSR up to 50 dB and a maximum output power of 4mW coupled in the waveguide have been measured. The fabrication flow is fully planar and compatible with large scale integration silicon photonics circuit.

2:30 PM
24.2 Quantum Confinement Effects in GeSn/SiGeSn Heterostructure Lasers (Invited), *D. Stange, N. von den Driesch, D. Rainko, T. Zabel*, B. Marzban**, Z. Ikonic^, P. Zaumseil, G. Capellini, S. Mantl, J. Witzens**, H. Sigg*, D. Grützmacher and D. Buca, Forschungszentrum Jülich GmbH, *Paul Scherrer Institute, **RWTH Aachen, ***University of Leeds, ^IHP*

We discuss direct bandgap group IV materials, GeSn/SiGeSn heterostructures and resulting quantum confinement effects for laser implementation. After material characterization, optical properties, including lasing, are probed via photoluminescence spectrometry. The quantum confinement effect in GeSn wells of different thicknesses is investigated. Theoretical calculations show strong quantum confinement to be undesirable past a certain level, as the very different effective masses of Γ and L electrons lead to a decrease of the L- to Γ-valley energy difference. A main limiting factor for lasing devices turns out to be the defective region at the interface to the Ge substrate due to the high lattice mismatch to GeSn. The use of buffer technology and subsequent pseudomorphic growth of multi-quantum-wells structures offers confinement of carriers in the active material, far from the misfit dislocations region. Performance is strongly boosted, as a reduction of lasing thresholds from 300 kW/cm2 for bulk devices to below 45 kW/cm2 in multi-quantum-well lasers is observed at low temperatures, with the reduction in threshold far outpacing the reduction in active gain material volume.

2:55 PM
24.3 Monolithic Integration of O-band Photonic Transceivers in a "Zero-change" 32nm SOI CMOS, *S. Moazeni, A. Atabaki*, D. Cheian*, S. Lin, R. J. Ram*, and V. Stojanović, University of California, *Massachusetts Institute of Technology*

We demonstrate a monolithic silicon photonic platform in an unmodified 32nm SOI CMOS process. This platform provides the fastest transistors ever monolithically integrated with photonics. We demonstrate 12 Gb/s O-band optical transceivers by resonant-based modulators/detectors with analog front-end circuits. This scheme provides the electro-photonic performances needed for HPC applications.

3:15 PM *Coffee Break*

3:40 PM
24.4 Tunnel-Modulated Ge LED/Laser Light Source and a Sub-Thermal Voltage Switching Detector for the Monolithic On-Chip Optical Transceiver, *R. Koerner, I. A. Fischer, R. Soref *, D. Schwarz, C. J. Clausen, L. Hänel, M. Oehme, J. Schulze, University of Stuttgart, *University of Massachusetts*

We report the first demonstration of a Ge based, steep switching (114 mV/dec), directly tunnel-modulated LED/laser light source (Germanium Zener-Emitter) and sub-thermal voltage-switching (31 mV/dec) photodetector (Germanium Esaki-Collector), for the monolithic integration of an optical transceiver on Silicon (100).

4:05 PM
24.5 A novel 25 Gbps electro-optic Pockels modulator integrated on an advanced Si photonic platform, *F. Eltes, M. Kroh*, D. Caimi, C. Mai*, Y. Popoff, G. Winzer*, D. Petousi*, S. Lischke*, J. E. Ortmann**, L. Czornomaz, L. Zimmermann*, J. Fompeyrine, S. Abel, IBM Research – Zurich, *IHP, **The University of Texas at Austin*

We demonstrate the first electro-optic modulator exploiting the Pockels effect monolithically integrated on an advanced silicon photonics platform. The devices, based on barium titanate thin films on 200 mm, show excellent VpiL (0.3 Vcm) and VpiLa (1.7 VdB), high-speed operation (25 Gbps), and low static power tuning (100 nW).

Session 25: Power and High-Speed Devices – Novel Device Concepts
Tuesday, December 5
Imperial Ballroom A
Co-Chairs: Florin Udrea, Cambridge University
Shyh-Chiang Shen, Georgia Institute of Technology

2:05 PM

25.1 Fast Switching Performance by 20 A / 730 V AlGaN/GaN MIS-HFET Using AlON Gate Insulator, *S. Nakazawa, H.-A. Shih, N. Tsurumi, Y. Anda, T. Hatsuda, T. Ueda, M. Nozaki*, T. Yamada*, T. Hosoi*, T. Shimura*, H. Watanabe*, and T. Hashizume**, Panasonic Corp., *Osaka University, **Hokkaido University*

In this paper, high current and high voltage AlGaN/GaN metal-insulator-semiconductor (MIS) heterojunction field-effect transistors (HFETs) on Si are demonstrated. The devices exhibit a drain current of 20 A as well as a breakdown voltage of 730 V, serving normally-off operations. Stable interfacial characteristics free from the hysteresis in the transfer characteristics are enabled by the introduction of AlON gate insulator. Recessed gate formed by epitaxial regrowth of AlGaN/GaN heterojunction successfully reduces the on-state resistance and eliminates the processing damage on the surface of the grooved structure. Note that an oxygen annealing followed by the deposition of AlON shifts the threshold voltage to positive side. The resultant switching performance by the 20 A / 730 V AlGaN/GaN MIS-HFET is very fast with dV/dt of 78 V/ns and 169 V/ns for turn-on and turn-off operations, respectively. The performances indicate that the proposed MIS-HFETs are very promising for practical power switching applications.

2:30 PM

25.2 An Interdigitated GaN MIS-HEMT/SBD Normally-Off Power Switching Device with Low ON-resistance and Low Reverse Conduction Loss, *J. Lei, J. Wei, G. Tang, Q. Qian, M. Hua, Z. Zhang, Z. Zheng, and K. J. Chen, The Hong Kong University of Science and Technology*

A normally-off GaN power switching device with low-loss reverse conduction was demonstrated. This device features interdigitated MIS-HEMT and lateral-SBD sharing common ohmic contacts and access regions. The device exhibits a Vth of 1.7 V, RON of 12.1 Ω•mm, BV of 698 V, and reverse turn-on voltage of 0.6 V.

2:55 PM

25.3 Large Signal Linearity Enhancement of AlGaN/GaN High Electron Mobility Transistors by Device-level V_T Engineering for Transconductance Compensation, *S. Joglekar, U. Radhakrishna, D. Piedra, D. Antoniadis, T. Palacios, Massachusetts Institute of Technology*

This work is demonstrates new device-technology to improve the linearity of GaN-based high electron mobility transistors (HEMTs) through device-level transconductance (gm)-compensation through VT- engineering and self-alignment through channel- fin-formation. The technique is used to achieve GaN-RF-HEMTs that can yield superior output power(Pout), power-added-efficiency(PAE), while also providing low IMD, reduced sidebands and signal-distortion

3:15 PM *Coffee Break*

3:40 PM

25.4 200V, 4MV/cm Lateral Diamond MOSFET, *T.T. Pham, J. Pernot, C. Masante, D. Eon, E. Gheeraert, G. Chicot, F. Udrea* and N. Rouger**, Univ. Grenoble Alpes, *The University of Cambridge, **Université de Toulouse*

Lateral diamond MOSFETs operating in the deep depletion regime have been experimentally demonstrated, exhibiting already impressive features: 200 V breakdown with 0.6 nA/mm gate and drain leakage, 4 MV/cm peak electric field at breakdown even without the use of field plates, carrier mobility between 1000 and 1700 $cm^2/V.s$.

4:05 PM

25.5 Novel 5V-EDMOS transistor with a record f_{MAX} of 450 GHz in a baseline 40nm CMOS technology, *T. V. Dinh, J. Sonsky, J. Claes, O. Dieball*, Guido T. Sasse and C. Detcheverry, NXP Semiconductors, *RWTH Aachen*

A new 5V-EDMOS device (BV ~ 10V) comprising a stepped gate oxide and a dummy gate, which boosts the RF performance to a record fMAX (~ 450 GHz), very high fT (~ 90GHz) and small device degradation, has been designed and fabricated in a baseline 40nm CMOS technology.

4:30 PM

25.6 High Rejection UNII 5.2GHz Wideband Bulk Acoustic Wave Filters Using Undoped Single Crystal AlN-on-SiC Resonators, *M. D. Hodge, R. Vetury, S. R. Gibb, M. Winters, P. Patel, M. A. McLain, Y. Shen, D. H. Kim, J. Jech, K. Fallon, R. Houlden, D. M. Aichele and J. B. Shealy, Akoustis Technologies Inc.*

5.24GHz bulk acoustic wave filters, utilizing undoped single crystal aluminum nitride, are reported. The filters had an absolute 4dB bandwidth of 151 MHz, a minimum insertion loss of 2.82 dB and rejection >40 dB. Resonators show k2eff of 6.32%, Q of 1523, and FOM of 96.

Session 26: Sensors, MEMS, BioMEMS - Technologies for Neural Activity Monitoring and DNA Analysis
Tuesday, December 5
Imperial Ballroom B
Co-Chairs: Duygu Kuzum, University of California, San Diego
Bernard Legrand, LAAS-CNRS, University of Toulouse

2:05 PM
26.1 Transparent Artifact-free Graphene Electrodes for Compact Closed-loop Optogenetics Systems, *X. Liu, Y. Lu, E. Iseri, C. Ren, H. Liu, T. Komiyama, and D. Kuzum, University of California San Diego*

In this work, we fabricated low impedance transparent graphene microelectrode arrays for artifact-free electrophysiological recordings. We demonstrated that transparent graphene electrodes eliminate light-induced artifacts during optical imaging and optogenetic stimulation. Finally, we designed a compact system incorporating both the graphene microelectrode array and fiber-coupled µLEDs for closed-loop optogenetic stimulation.

2:30 PM
26.2 High-yield passive Si photodiode array towards optical neural recording, *D*. *Mao, J. Morley, Z. Zhang, M. Donnelly, and G. Xu, *University of Massachusetts Amherst*

We demonstrate a high yield, passive Si photodiode array, aiming to establish a miniaturized optical recording device for in-vivo use. Our fabricated array features high yield (>90%), high sensitivity (down to 32 µW/cm2), high speed (1000 frame per second by scanning over up to 100 pixels), and sub-10uW power.

2:55 PM
26.3 Interactions of nanowires with cells and tissue (Invited), *C. Prinz, Lund University*

We report that arrays of vertical gallium phosphide nanowires are promising materials for biosensing in membranes and cells. Moreover, due to the exceptional control one can achieve over their geometrical and optic properties, we use nanowires to investigate the interactions of high aspect ratio nanoparticles with living cells and tissue.

3:15 PM *Coffee Break*

3:40 PM
26.4 Integration of FinFETs and 3D nanoprobes devices on a common bio- platform for monitoring electrical activity of single neurons., *A. Casanova, M.-C. Blatche, F. Mathieu, L. Bettamin, H. Martin, D. Gonzalez-Dunia, L. Nicu, and G. Larrieu, Université de Toulouse*

We propose to co-integrate high surface-to-volume ratio active (Fin-FETs) and passive devices (vertical nanowire-probes) on the same platform to monitor activity of single mammalian neurons. High signal-to-noise ratio were demonstrated (SNR=80 for intracellular configuration). The bio-platform was used to examine the effect of bio-chemical and electrical stimulations on neuronal activity.

4:05 PM
26.5 Direct characterization of circulating DNA in blood plasma using µLAS technology, *R. Malbec, B. Chami, H. H. T. Ngo, A. Didelot*, F. Garlan*, S. Garrigou*, V. Taly*, L. Aeschbach***, E. Trofimenko***, V. Dion***, A. Boutonnet-Rodat**, F. Ginot** and A. Bancaud, Université de Toulouse, *Paris Descartes University, **Picometrics Technologies, ***University of Lausanne*

Circulating cell-free DNA (cfDNA) is a powerful cancer biomarker for establishing targeted therapies or monitoring patients' treatment. However, current cfDNA characterization is severely limited by its low concentration, requiring the extensive use of amplification techniques. Here we report that the µLAS technology allows us to quantitatively characterize the size distribution of purified cfDNA in a few minutes, even when its concentration is as low as 1 pg/µL. Moreover, we show that DNA profiles can be directly measured in blood plasma with a minimal conditioning process to speed up considerably speed up the cfDNA analytical chain.

4:30 PM
26.6 Nanopores incorporating ITO electrodes for electrical gating of DNA at different folding states, *X. Zhu, X. Wang, Z. Cao, Z. Ye, C. Gu, C. H. Jin, Y. Liu, Zhejiang University*

Nanopore devices integrated with ITO gate electrodes are fabricated, producing pore diameters <10nm and lengths ~30nm. Translocation signals of λ-DNA reveal detailed signatures of various DNA folding states. The gate bias VG modulates the translocation events. As VG rises from - 0.5V to 0.5V, the count of folded-once events increases by ~5.5X relative to that of unfolded ones, indicating capability of electrically modulating the effective pore cross-section.

IEDM Panel
Tuesday, December 5
Continental 1-5
Moderator: H.S. Philip Wong, Stanford University

Title: **Where will the next Intel be headquartered?**

Dennard scaling has fulfilled its historic mission and traditional Moore's Law is coming to an end. Who will drive and lead innovation in the semiconductor industry in the coming decades? We have assembled a panel of experts and industry veterans to address this important question. Who – foundry, IDM, fabless, application developers (the FAMGA) – will drive newer generations of technologies? Are foundries and IDMs becoming the "Home Depot" of architects and application developers who will drive all the value propositions? Can fabless without a system product still survive? Will system houses reach down to invest and develop the chip technologies? Who – U.S., Europe, Japan, Korea, Taiwan, China – will become the dominant chip supplier? Can R&D investments by sovereign countries change the landscape? Will countries reap benefits by investing in R&D specifically within the country? Who – material scientists, device technologists, circuit designers, system architects, application developers – will be the source of technology innovations and advances? Which region – US, Europe, Japan, China, Taiwan, Korea – will present the most innovative papers at the IEDM in a decade? Who – logic companies, memory companies, analog companies – will be the next Intel? And where will that company do research, development, and manufacturing?

Panelists:
1. Kaizad Mistry, Intel
2. Kevin Zhang, TSMC
3. Jong Shik Yoon, Samsung
4. Chidi Chidambaram, Qualcomm
5. Kazu Ishimaru, Toshiba
6. TY Chiu, SMIC

Session 28: Memory Technology - In-memory Computing
Wednesday, December 6
Grand Ballroom A
Co-Chairs: Ming Liu, Institute of Microelectronics, CAS
Daniele Ielmini, Politecnico di Milano

9:05 AM
28.1 Modeling-based design of brain-inspired spiking neural networks with RRAM learning synapses, *G. Pedretti, S. Bianchi, V. Milo, A. Calderoni*, N. Ramaswamy*, and D. Ielmini, Politecnico di Milano, *Micron Technology*

Brain-inspired computing is currently gaining momentum as a viable technology for artificial intelligence enabling recognition, language processing and online unsupervised learning. Brain-inspired circuit design is currently hindered by 2 fundamental limits: (i) understanding the event-driven spike processing in the human brain, and (ii) developing predictive models to design and optimize cognitive circuits. Here we present a comprehensive model for spiking neural networks based on spike-timing dependent plasticity (STDP) in resistive switching memory (RRAM) synapses. Both a Monte Carlo (MC) model and an analytical model are presented to describe experimental data from a state-of- the-art neuromorphic hardware. The model can predict the learning efficiency and time as a function of the input noise and pattern size, thus paving the way for model-based design of cognitive brain-like circuits.

9:30 AM
28.2 A 16Mb Dual-Mode ReRAM Macro with Sub-14ns Computing-In-Memory and Memory Functions Enabled by Self-Write Termination Scheme, *W.-H. Chen, W.-J. Lin, L.-Y. Lai, S. Li*, C.-H. Hsu**, H.-T. Lin, H.-Y. Lee**, J.-W. Su**, Y. Xie*, S.-S. Sheu**, and M.-F. Chang, National Tsing Hua University, *UC Santa Barbara, **ITRI*

Recent ReRAM devices enable the development of computing-in-memory (CIM) for beyond von Neumann structure. However, wide distribution in ReRAM resistance (R) causes low yield for CIM operations. This work proposes a dual-mode computing (DMc) ReRAM macro structure with a dual- function voltage-mode self-write termination (DV- SWT) scheme to achieve both memory and fundamental CIM functions (AND, OR and XOR operations) with high yield. The DV-SWT increases the read margin for CIM operations by suppressing the R-variations caused by macro-level IR-drop and process variations. A 16Mb DMc-ReRAM full-function macro was fabricated using 1T1R HfO ReRAM devices and 0.15um CMOS process. The measured delay of the CIM operations is less than 14ns, which is 86+x faster than previous ReRAM-based CIM works. This work also represents the first CIM ReRAM macro with ReRAM device and CIM-peripheral circuits fully integrated on the same die.

9:55 AM
28.3 Compressed Sensing Recovery using Computational Memory, *M. Le Gallo, A. Sebastian, G. Cherubini, H. Giefers, and E. Eleftheriou, IBM Research-Zurich*

Computational memory (CM) is a promising non-von Neumann approach where certain computational tasks are performed within resistive memory units by exploiting their physical attributes. We propose a new method for fast and robust compressed sensing (CS) recovery of sparse signals using CM. For a signal of size N, this method achieves a potential O(N)-fold complexity reduction compared with a standard software approach. Large-scale experimental demonstrations using more than 256k phase-change memory (PCM) devices are presented along with an in-depth device analysis and array-level considerations.

10:20 AM
28.4 Data-Aware NAND Flash Memory for Intelligent Computing with Deep Neural Network (Invited), *K. Takeuchi, Chuo University*

This paper presents data-aware NAND flash memories. By recognizing the data value, sophisticated data management such as storing important data in reliable memory cells or adaptively optimizing read voltage are realized. Consequently, intelligent computing such as image recognition with deep neural network, data compression and disaggregated hybrid storage are achieved.

10:45 AM
28.5 Reconfigurable NAND/NOR logic gates in 28 nm HKMG and 22 nm FD-SOI FeFET technology, *E. T. Breyer, H. Mulaosmanovic,; T. Mikolajick, and S. Slesazeck, NaMLab gGmbH*

We present for the first time a reconfigurable NAND/NOR logic gate based on a single ferroelectric FET (FeFET), having hafnium oxide as the ferroelectric material and a pull-up device connected in series. Electrical results and SPICE simulations reveal the feasibility of the concept for 28nm HKMG and 22nm FD-SOI FeFET technology.

Session 29: Circuit and Device Interaction - Advanced Platform Technologies
Wednesday, December 6
Grand Ballroom B

Co-Chairs: Chung-Hsun Lin, GLOBALFOUNDRIES
Kang-ill Seo, Samsung

9:05 AM
29.1 A 10nm High Performance and Low-Power CMOS Technology Featuring 3rd Generation FinFET Transistors, Self-Aligned Quad Patterning, Contact over Active Gate and Cobalt Local Interconnects, *C. Auth, A. Aliyarukunju, M. Asoro, D. Bergstrom, V. Bhagwat, J. Birdsall, N. Bisnik, M. Buehler, V. Chikarmane, G. Ding, Q. Fu, H. Gomez, W. Han, D. Hanken, M. Haran, M. Hattendorf, R. Heussner, H. Hiramatsu, B. Ho, S. Jaloviar, I. Jin, S. Joshi, S. Kirby, S. Kosaraju, H. Kothari, G. Leatherman, K. Lee, J. Leib, A. Madhavan, K. Marla, H. Meyer, T. Mule, C. Parker, S. Parthasarathy, C. Pelto, L. Pipes, I.Post, M. Prince, A. Rahman, S. Rajamani, A. Saha, J. Dacuna Santos, M. Sharma, V. Sharma, J. Shin, P. Sinha, P. Smith, M. Sprinkle, A. St. Amour, C. Staus, R. Suri, D. Towner, A. Tripathi, A. Tura, C. Ward, A. Yeoh, Intel Corporation*

A 10nm logic technology using 3rd-generation FinFET transistors with Self-Aligned Quad Patterning (SAQP) for critical patterning layers, and cobalt local interconnects at three local interconnect layers is described. For high density, a novel self-aligned contact over active gate process and elimination of the dummy gate at cell boundaries are introduced. The transistors feature rectangular fins with 7nm fin width and 46nm fin height, 5th generation high-k metal gate, and 7th-generation strained silicon. Four or six workfunction metal stacks are used to enable undoped fins for low Vt, standard Vt and optional high Vt devices. Interconnects feature 12 metal layers with ultra-low-k dielectrics throughout the interconnect stack. The highest drive currents with the highest cell densities are reported for a 10nm technology.

9:30 AM
29.2 Performance and Design Considerations for Gate-All-Around Stacked-NanoWires FETs (Invited), *S. Barraud, V. Lapras, B. Previtali, M.P. Samson*, J. Lacord, S. Martinie, M.-A. Jaud, S. Athanasiou, F. Triozon, O. Rozeau, J.M. Hartmann, C. Vizioz, C. Comboroure*, F. Andrieu, J.C. Barbé, M. Vinet, and T. Ernst, CEA, LETI, MINATEC campus and Univ. Grenoble Alpes, *STMicroelectronics*

This paper presents recent progress on Gate-All- Around (GAA) stacked-NanoWire (NW) / NanoSheet (NS) MOSFETs. Key technological challenges will be discussed and recent research results presented. Width-dependent carrier mobility in Si NW/NS and FinFET will be analyzed, and intrinsic performance and design considerations of GAA structures will be discussed and compared to FinFET devices with a focus on electrostatics, parasitic capacitances and different layout options. The results show that more flexibility can be achieved with stacked-NS transistors in order to manage power- performance optimization.

9:55 AM
29.3 Accurate Performance Evaluation for the Horizontal Nanosheet Standard-Cell Design Space Beyond 7nm Technology, *Y.M. Lee, M.H. Na, A. Chu, A. Young, T. Hook, L. Liebmann**, E.J. Nowak, S.H. Baek*, R. Sengupta*, H. Trombley, and X. Miao, IBM Research, *Samsung Electronics, **GLOBALFOUNDRIES*

Vertically-stacked horizontal gate-all-around Nanosheet structures have been recognized as good candidates to achieve improved power-performance and area scaling for beyond the 7nm node. We present a quantitative performance evaluation of horizontal Nanosheet structures across a wide range of sub-7nm design space, including key design styles and unique Nanosheet challenges.

10:20 AM
29.4 22FFL: A High Performance and Ultra Low Power FinFET Technology for Mobile and RF Applications, *B. Sell, B. Bigwood, S. Cha, Z. Chen, P. Dhage, P. Fan, M. Giraud-Carrier, A. Kar, E. Karl, C.-J. Ku, R. Kumar, T. Lajoie, H.-J. Lee, G. Liu, S. Liu, Y. Ma, S. Mudanai, L. Nguyen, L. Paulson, K. Phoa, K. Pierce, A. Roy, R. Russell, J. Sandford, J. Stoeger, N. Stojanovic, A. Sultana, J. Waldemer, J. Wan, W. Xu, D. Young, J. Zhang, Y. Zhang, and P. Bai, Intel Corporation*

A FinFET technology named 22FFL has been developed that combines high-performance, ultra-low power logic and RF transistors as well as single-pattern backend flow for the first time. High performance transistors exhibit 57%/87% higher NMOS/PMOS drive current compared to the previously reported 22nm technology. New ultra-low power logic devices are introduced that reduce bit cell leakage by 28x compared to a regular SRAM cell enabling a new 6T low-leakage SRAM with bit cell leakage of sub 1pA/cell. An RF device with optimized layout has been developed and shows excellent fT/fMAX of (230GHz/284GHz) and (238GHz/242GHz) for NMOS and PMOS respectively.

10:45 AM

29.5 A 7nm CMOS Technology Platform for Mobile and High Performance Compute Application (Late News), *S. Narasimha, B. Jagannathan, A. Ogino, D. Jaeger, B. Greene, C. Sheraw, K. Zhao, B. Haran, U. Kwon, A.K.M. Mahalingam, B. Kannan, B. Morganfeld, J. Dechene, C. Radens, A. Tessier, A. Hassan, H. Narisetty, I. Ahsan, M. Aminpur, C. An, M. Aquilino, A. Arya, R. Augur, N. Baliga, R. Bhelkar, G. Biery, A. Blauberg, N. Borjemscaia, A. Bryant, L. Cao, V. Chauhan, M. Chen, L. Cheng, J. Choo, C. Christiansen, T. Chu, B. Cohen, R. Coleman, D. Conklin, S. Crown, A. da Silva, D. Dechene, G. Derderian, S. Deshpande, G. Dilliway, K. Donegan, M. Eller, Y. Fan, Q. Fang, A. Gassaria, R. Gauthier, S. Ghosh, G. Gifford, T. Gordon, M. Gribelyuk, G. Han, J.H. Han, K. Han, M. Hasan, J. Higman, J. Holt, L. Hu, L. Huang, C. Huang, T. Hung, Y. Jin, J. Johnson, S. Johnson, V. Joshi, M. Joshi, P. Justison, S. Kalaga, T. Kim, W. Kim, R. Krishnan, B. Krishnan, Anil K., M. Kumar, J. Lee, R. Lee, J. Lemon, S.L. Liew, P. Lindo, M. Lingalugari, M. Lipinski, P. Liu, J. Liu, S. Lucarini, W. Ma, E. Maciejewski, S. Madisetti, A. Malinowski, J. Mehta, C. Meng, S. Mitra, C. Montgomery, H. Nayfeh, T. Nigam, G. Northrop, K. Onishi, C. Ordonio, M. Ozbek, R. Pal, S. Parihar, O. Patterson, E. Ramanathan, I. Ramirez, R. Ranjan, J. Sarad, V. Sardesai, S. Saudari, C. Schiller, B. Senapati, C. Serrau, N. Shah, T. Shen, H. Sheng, J. Shepard, Y. Shi, M.C. Silvestre, D. Singh, Z. Song, J. Sporre, P. Srinivasan, Z. Sun, A. Sutton, R. Sweeney, K. Tabakman, M. Tan, X. Wang, E. Woodard, G. Xu, D. Xu, T. Xuan, Y. Yan, J. Yang, K.B. Yeap, M. Yu, A. Zainuddin, J. Zeng, K. Zhang, M. Zhao, Y. Zhong, R. Carter,C-H. Lin, S. Grunow, C. Child, M. Lagus, R. Fox, E. Kaste, G. Gomba, S. Samavedam, P. Agnello, and DK Sohn, GLOBALFOUNDRIES*

We present a fully integrated 7nm CMOS platform featuring a 3rd generation finFET architecture, SAQP for fin formation, and SADP for BEOL metallization. This technology reflects an improvement of 2.8X routed logic density and >40% performance over the 14nm reference technology described in [1-3]. A full range of Vts is enabled on-chip through a unique multiworkfunction process. This enables both excellent low voltage SRAM response and highly scaled memory area simultaneously. The HD 6-T bitcell size is 0.0269um2. This 7nm technology is fully enabled by immersion lithography and advanced optical patterning techniques (like SAQP and SADP). However, the technology platform is also designed to leverage EUV insertion for specific multi-patterned (MP) levels for cycle time benefit and manufacturing efficiency. A complete set of foundation and complex IP is available in this advanced CMOS platform to enable both High performance Compute (HPC) and mobile applications.

Session 30: Plenary Session II
Wednesday, December 6
Grand Ballroom B

11:10 AM
IEEE Awards
General Chair: Stefan De Gendt, imec

2017 IEEE Cledo Brunetti Award

To: Guido Groeseneken

“For contributions to the characterization and understanding of the reliability physics of advanced MOSFET nanodevices.”

2017 IEEE Andrew S. Grove Award

To: Sorin Cristoloveanu

“For contributions to silicon-on-insulator technology and thin body devices.”

2017 IEEE Frederik Philips Award

To: Gary L. Patton

“For industry influence and leadership in the development of leading-edge microelectronics technology and collaborative research.”

Plenary Paper
Technical Program Chair: Ken Rim, Qualcomm

11:30 AM

30.1 Development of Sustainable Smart Society based on Transformative Electronics (Invited), *M. Ogura, Y. Ando, S. Usami, K. Nagamatsu, M. Kushimoto, M. Deki, A. Tanaka, S. Nitta, Y. Honda, M. Pristovsek, H. Kawai*, S. Yagi*, and H. Amano, Nagoya University, *POWDEC K.K.5, 2017 National Institute for Materials Science*

Defects which cause leakage under a high-voltage reverse-biased condition were identified in GaN pin diodes grown on freestanding GaN substrates. The performances of GaN-based horizontal-heterostructure superjunction high-electron mobility transistor and a GaN-nanorod-based vertical pnsuperjunction diode were simulated. A vertical pnsuperjunction was fabricated using GaN nanorod growth technology.

Session 31: Modeling and Simulation - Simulations of Nano-devices

Wednesday, December 6

Continental Ballroom 1-3

Co-Chairs: Mathieu Luisier, ETH Zurich

Viktor Sverdlov, TU Wien

9:05 AM

31.1 Time-resolved quantum transport for optoelectronics (Invited), *F. Michelini, K. Beltako, M. Bescond, N. Cavassilas and L. Raymond, Aix Marseille University, University Toulon, IM2NP*

We investigate time-resolved energy currents in a molecular optoelectronic junction made of two donors and an acceptor sandwiched between two electrodes and excited by a Gaussian femtosecond laser pulse. Features of the direct energy currents are thus correlated to the intra-molecular structure.

9:30 AM

31.2 Computational Study of Gate-Induced Drain Leakage in 2D-Semiconductor Field-Effect Transistors, *J. Kang, W. Cao, A. Pal, S. Pandey*, S. Kramer*, R. Hill*, G. Sandhu*, and K. Banerjee, University of California, Santa Barbara, *Micron Technology, Inc.*

Gate-induced-drain-leakage (GIDL) in 2D FETs is evaluated for the first time using a novel quantum transport methodology. GIDL is a key issue in access transistors, and our results establish the advantages of certain 2D semiconductors in greatly reducing GIDL and thereby support use of such materials in future memory technologies.

9:55 AM

31.3 How to Derive the Highest Mobility from 2D FETs – A First-Principle Study, *A. Pal, W. Cao, J. Kang, and K. Banerjee, University of California Santa Barbara*

A comprehensive mobility modeling framework for 2D-semiconductor FETs is developed for the first time. The framework is applied to study the impact of synthesis technology, defect concentration, electric field, and channel/dielectric materials on the mobility and guidelines are provided to both process and device engineers on designing FETs with maximized mobility.

10:20 AM

31.4 A Unified Surface Potential Based Physical Compact Model for Both Unipolar and Ambipolar 2D-FET: Experimental Verification and Circuit Demonstration, *L. Wang, Y. Li, X. Feng, K.-W. Ang, X. Gong, A. Thean, G. Liang, National University of Singapore*

A unified surface potential based physical compact model for both unipolar and ambipolar 2D-FET is developed and verified by device measurements. It included the influence of extensive disorder effects on transport. This compact model is implemented in Verilog-A for evaluating the possibility of digital and RF applications with 2D-FETs.

10:45 AM

31.5 Quantitative Model for Switching Asymmetry in Perpendicular MTJ: A Material-Device-Circuit Co-Design, ***D***. *Datta, H. Dixit, S. Agarwal, A. Dasgupta*, M. Tran**, D. Houssameddine**, Y. S. Chauhan*, D. Shum**, and F.*

*Benistant**, GLOBALFOUNDRIES Engineering Pvt. Ltd., *Indian Institute of Technology, **GLOBALFOUNDRIES Singapore Pte. Ltd.*

A physics based switching model for p-MTJ device is presented by combining 4x4 tunnelling conductance matrix derived using NEGF formalism and 4x4 ferromagnetic conductance matrix derived from Valet-Fert equation. It provides qualitative and quantitative agreement with switching voltages in spin torque experiments observed in IBM, Everspin and GLOBALFOUNDRIES hardware data.

Session 32: Process and Manufacturing Technology - 3D Integration
Wednesday, December 6
Continental Ballroom 4
Co-Chairs: Bich-Yen Nguyen, Soitec
Mitsuhiro Togo, GLOBALFOUNDRIES

9:05 AM
32.1 The impact of Sequential-3D integration on semiconductor scaling roadmap, *A. Mallik, A. Vandooren, L. Witters, A. Walke, J. Franco, Y. Sherazi, P. Weckx, D. Yakimets, M. Bardon, B. Parvais, P. Debacker, B. W. Ku*, S. K. Lim*, A. Mocuta, D. Mocuta, J. Ryckaert, N. Collaert, P. Raghavan, imec, *Georgia Institute of Technology, **Vrije Universiteit Brussel*

The continued physical feature size scaling of CMOS transistors is experiencing asperities due to several factors (physical, technological, and economical), and it is expected to reach its boundary in the coming years. Sequential-3D (S3D) integration has been perceived as a promising alternative to continue the benefits offered by semiconductor scaling. This paper addresses the different variants of S3D integration and potential challenges to achieve a realizable solution. We analyze and quantify the benefits observed due to sequential scaling at a die level.

9:30 AM
32.2 High performance low temperature FinFET with DPSER, gate last and Self Aligned Contact for 3D sequential integration, *J. Micout, V. Lapras, P. Batude, C. Fenouillet-Beranger, J. Lacord, B. Sklenard, B. Mathieu, Q. Rafhay*, V. Mazzocchi, J-P. Colinge, L. Lachal, X. Garros, M. Casse, A. Toffoli, G. Romano**, F. Allain, L. Brunet, J.-M. Hartmann, R. Bortolin, F. Mazen, S. Barraud, N. Rambal, C. Tabone, M-P. Samson**, P. Besombes, V. Delaye, Z. Saghi, V.Loup, C.Comboroure, V. Balan, L. Desvoivres, C. Vizioz, G. Ghibaudo*, and M. Vinet, CEA, LETI, MINATEC, *IMEP-LAHC, MINATEC, **ST Microelectronics*

For the first time, a low temperature (LT) FinFET process is demonstrated, using Solid Phase Epitaxy Regrowth (SPER), gate last integration and Self Aligned Contact (SAC). The LT devices exhibit performances close to those of the High Temperature Process Of Reference (HT POR). Several techniques of SPER doping are investigated and an innovative Double SPER (DSPER) process using two amorphization/recrystallization steps, is demonstrated. This DSPER process has the advantage of doping the bulk of the S/D junctions. This work opens the door to the fabrication of high- performance LT FinFETs for 3D sequential integration.

9:55 AM
32.3 Material Innovation for MOL, BEOL, and 3D Integration (Invited), *J. Koike, M. Hosseini, H. T. Hai, D. Ando, and Y. Sutou, Tohoku University*

This paper presents new materials and processes for advanced technology node of Si semiconductor devices. For MOL, Co contact plug and amorphous Co-Ti barrier showed a good adhesion, limited growth of Co silicide, and a low contact resistivity of the order of 10-9 Ωcm2 on both n+ and p+ Si. For BEOL, a CVD-MnOx layer could be formed conformally in high-aspect ratio contact holes. The ALD-MnOx layer of 1.2 nm thick showed a good diffusion barrier property at 400 oC. For 3D integration, TSV of 10 µm diameter and 80 µm depth could be filled with low resistivity sintered Cu paste without voids.

10:20 AM
32.4 Scalable, sub 2µm Pitch, Cu/SiCN to Cu/SiCN Hybrid Wafer-to-Wafer Bonding Technology, *E. Beyne, S.-W. Kim, L. Peng, N. Heylen, J. De Messemaeker, O. O. Okudur, A. Phommahaxay, T.-G. Kim, M. Stucchi, D. Velenis, A. Miller, and G. Beyer, imec*

We present a novel approach to wafer-to-wafer hybrid bonding, using SiCN in combination with Cu pads of unequal size and surface topography, generated through novel CMP processing. Combining all three enabled a first-time demonstration of electrically yielding 300 mm-bonded wafers with pad pitches of 1.44 µm down to 0.72 µm.

10:45 AM
32.5 High efficiency direct liquid jet impingement cooling of high power devices using a 3D-shaped polymer cooler, *T. Tiwei, H. Oprins, V. Cherman, G. Van der Plas, I. De Wolf, E. Beyne and M. Baelmans*, imec, *KU Leuven*

A novel 3D-shaped polymer multi-jet impingement cooler based on low cost fabrication techniques is introduced for high performance applications. This paper presents the modeling study, design, fabrication, experimental characterization and benchmarking of this cooling concept, showing a very good thermal performance with low required pumping power.

Session 33: Power Devices - Development of GaN Power Devices Technologies
Wednesday, December 6
Imperial Ballroom A
Co-Chairs: Martin Kuball, University of Bristol
Gaudenzio Meneghesso, University of Padova

9:05 AM
33.1 Smart GaN Platform: Performance & Challenges (Invited), *C.-L. Tsai, Y.-H. Wang, M.-H. Kwan, P.-C. Chen, F.-W. Yao, S-C. Liu, J.-L. Yu, C-L Yeh, R.-Y. Su, W. Wang, W.-C. Yang, K.-Y. Wong, Y.-S. Lin, M.-C. Lin, H.-Y. Wu, C.-M. Chen, C.-Y. Yu, C.-B. Wu, M.-H., Chang, J.-S. You, T.-M. Huang, S.-P. Wang, L.Y. Tsai, Chan-Hong Chern, H.C. Tuan and A. Kalnitsky, Taiwan Semiconductor Manufacturing Company*

This paper explores the next stage of GaN power devices with 2 levels integration of peripheral low voltage active and passive devices. The 1st level consists of protection/control/driving circuits, which potentially improve the performance and overcome the challenges to the power devices. (The 2nd level integration has proposed high-low side on-chip integration on 100V technology platform). The challenge of channel modulation due to substrate bias sharing is effectively eliminated by the invented new scheme. The system efficiency of DC-DC buck converter using such scheme is enhanced with lower on-state resistance and good stability.

9:30 AM
33.2 Reverse-Bias Stability and Reliability of Hole-Barrier-Free E-mode LPCVD-SiN_x/GaN MIS-FETs, *M. Hua, J. Wei, Q. Bao, J. He, Z. Zhang, Z. Zheng, J. Lei and K. J. Chen, The Hong Kong University of Science and Technology*

With limited hole-generation, E-mode n-channel LPCVD-SiNx/GaN MIS-FET delivers small NBTI even without a hole-barrier. In reverse-bias stress, the SiNx gate dielectric, while exhibiting a negative valance-band-offset with GaN, acts as a plug to holes. The hole-induced degradation can be greatly contained by limiting gate-bias to a few volts below VTH.

9:55 AM
33.3 Improvement of Positive Bias Temperature Instability Characteristic in GaN MOSFETs by Control of Impurity Density in SiO_2 Gate Dielectric, *T. Yonehara, Y. Kajiwara, D. Kato, K. Uesugi, T. Shimizu, Y. Nishida, H. Ono, A. Shindome, A. Mukai, A. Yoshioka and M. Kuraguchi, Toshiba Corporation*

Positive bias temperature instability in GaN MOSFET was drastically suppressed by reducing certain impurity densities in SiO2 gate dielectric. Impurities, which formed the electron traps in SiO2, were controlled by heat treatment after SiO2 deposition, and the threshold voltage shift characteristic was improved by the reduction of the impurity densities.

10:20 AM
33.4 Evidence of defect band in carbon-doped GaN controlling leakage current and trapping dynamics, *C. Koller, G. Pobegen, C. Ostermaier**, and D. Pogany*, KAI GmbH, *Vienna University of Technology, **Infineon Technologies*

Carbon-doped GaN layers, crucial for GaN HEMT buffers, show in a wide temperature range non- Arrhenius thermal behavior of capacitance transients related to trapping/detrapping dynamics and of leakage current. Our model indicates that conduction via defect band controls both processes, redefining the way III-N:C containing layers should be investigated.

10:45 AM

33.5 Total Suppression of Dynamic-Ron in AlGaN/GaN-HEMTs Through Proton Irradiation, *M. Meneghini, A. Tajalli, P. Moens*, A. Banerjee*, A. Stockman*, M. Tack*, S. Gerardin, M. Bagatin, A. Paccagnella, E. Zanoni, and G. Meneghesso, University of Padova, Onsemiconductor*, CMST imec/Ghent University***

For the first time, we demonstrate that proton irradiation can be an effective tool for achieving zero dynamic-Ron in GaN-based power HEMTs. Based on combined pulsed characterization, transient measurements and hard switching analysis on untreated and irradiated devices we demonstrate the following relevant results: (i) the devices under analysis show an outstanding robustness against 3 MeV proton irradiation, up to a fluence of 1.5x1014 cm-2. (ii) For fluences higher than 1013 cm-2, the devices show a substantial reduction of dynamic-Ron. At the highest analyzed fluence (1.5x1014 cm-2), dynamic Ron is completely suppressed at 600 V/150 °C, without measurable changes in the gate and sub- threshold leakage and in the threshold voltage. (iii) transient and hard switching analysis indicate the total suppression of the trap-related transients identified before radiation testing. The results are explained by considering that proton irradiation increases the leakage through the uid-GaN channel layer. This increases the detrapping rate, and leads to the suppression of dynamic-Ron at high VDS

Session 34: Focus Session - Optoelectronics, Displays and Imagers - Silicon Photonics
Wednesday, December 6
Imperial Ballroom B
Co-Chairs: Zhiping Zhou, Peking University
Edoardo Charbon, EPFL

9:05 AM

34.1 Advanced Silicon Photonics Technology Platform Leveraging a Semiconductor Supply Chain (Invited), *P. De Dobbelaere, A. Dahl, A. Mekis, B. Chase, B. Weber, B. Welch, D. Foltz, G. Armijo, G. Masini, G. McGee, G. Wong, J. Balardeta, J. Dotson, J. Schramm, K. Hon, K. Khauv, K. Robertson, K. Stechschulte, K. Yokoyama, L. Planchon, L. Tullgren, M. Eker, M. Mack, M. Peterson, N. Rudnick, P. Milton, P. Sun, R. Bruck, R. Zhou, S. Denton, S. Fathpour, S. Gloeckner, S. Jackson, S. Pang, S. Sahni, S. Wang, S. Yu, T. Pinguet, Y. De Koninck, Y. Chi, Y. Liang, Luxtera Inc.*

This paper covers a silicon photonics technology platform that leverages a commercial semiconductor supply chain for the manufacturing of high performance optical trans-ceivers for high performance computing and hyper-scale data-center applications.

9:30 AM

34.2 Reliable 50Gb/s Silicon Photonics Platform for Next-Generation Data Center Optical Interconnects (Invited), *P. Absil, K. Croes, A. Lesniewska, P. De Heyn, Y. Ban, B. Snyder, J. De Coster, F. Fodor, V. Simons, S. Balakrishnan, G. Lepage, N. Golshani, S. Lardenois, S.A. Srinivasan, H. Chen, W. Vanherle, R. Loo, R. Boufadil, M. Detalle, A. Miller, P. Verheyen, M. Pantouvaki and J. Van Campenhout, imec vzw*

The next generations of data centers require a scalable optical transceiver technology. In this paper we present a silicon photonics platform supporting single-channel data rates of 50Gb/s and above. Advanced process options include 50GHz GeSi electro-absorption modulators, high efficiency thermo-optic phase shifters with Ppi

9:55 AM

34.3 Developments in 300mm silicon photonics using traditional CMOS fabrication methods and materials (Invited), *C. Baudot, M. Douix, S. Guerber, S. Crémer, N. Vulliet, J. Planchot, R. Blanc, L. Babaud, C. Alonso-Ramos*, D. Benedikovich*, D. Pérez-Galacho*, S. Messaoudène**, S. Kerdiles**, P. Acosta-Alba**, C. Euvrard-Colnat**, E. Cassan*, D. Marris-Morini*, L. Vivien*, and F. Boeuf, STMicroelectronics, *Université Paris Saclay, **Université Grenoble Alpes*

Silicon photonics technological platforms are meant to generate derivative products and concurrently to benefit from the main advantages associated with CMOS platforms namely: high yield, system robustness, product reliability and large volume, low cost production. Nevertheless, a simultaneous innovative approach is to analogously take advantage from state-of-the-art fabrication methods and tools available in CMOS to develop new solutions and propose better performing devices to the platform.

10:20 AM

34.4 Advanced devices and packaging of Si-photonics based optical transceiver for optical interconnection (Invited), *K. Kurata, K. Yashiki, J. Fujikata, T. Horikawa, K. Kinoshita, J. Ushida, M. Tokushima, Y. Suzuki, D. Okamoto, S. Takahashi, A. Ukita, K. Takemura, Y. Ibusuki, T. Shimizu, M. Kurihara, Y. Hagihara, T. Mogami, and T. Nakamura Photonics Electronics Technology Research Association (PETRA)*

High integration of photonics circuits and electronic circuits is expected in Si photonics technology. The small size of integrated photonics circuits is expected to lead to low costs and high-density optical interconnection. On the other hand, reduction in packaging costs will become vital toward lowering costs because of the demand for highly accurate assembly processes in optical coupling. Harmony between integrated devices and packaging design should be consider to realize miniature size and low cost transceiver. We propose advanced devices and Packaging of an Si-photonics-based optical transceiver for optical interconnection.

10:45 AM

34.5 Femto-joule-per-bit integrated nanophotonics and challenge for optical computation (Invited), *M. Notomi, K. Nozaki, A. Shinya, and M. Takiguchi, NTT Corporation*

We review our recent achievements in various energy-efficient nanophotonic devices based on photonic crystals. Strong light confinement enables large enhancement of light-matter interactions and ultrasmall capacitance for OE/EO conversion devices. Owing to these two features, we have demonstrated that the energy consumption can be reduced down to fJ/bit or less, suggesting energy-efficient optical link in processor chips, and even opportunity for ultrasmall latency optoelectronic computations.

Session 35: Modeling and Simulation - Progress in Modeling Methodology and Approaches

Wednesday, December 6

Continental Ballroom 1-3

Co-Chairs: Dragica Vasileska, Arizona State University

Stephen Cea, Intel Corp.

1:35 PM

35.1 NEGF based transport modelling with a full-band, pseudopotential Hamiltonian: Theory, Implementation and Full Device Simulations, *M. G. Pala, O. Badami*, and D. Esseni*, Université Paris-Saclay, *University of Udine*

This paper presents the theory, implementation and application of a new quantum transport, NEGF based modelling approach employing a full-band Empirical Pseudopotential (EP) Hamiltonian. The use of a hybrid real-space$/$plane-waves basis results in a remarkable reduction of the computational burden compared to a full plane waves basis, which allowed us to obtain complete, self-consistent simulations for both FETs and Tunnel FETs in Si or in Ge, and with geometrical features in line with forthcoming CMOS technologies.

2:00 PM

35.2 First-principles based quantum transport simulations of nanoscale field effect transistors (Invited), *M. Shin, H.-E. Jung, and S. Jung, Korea Advanced Institute of Science and Technology*

We present first-principles density functional theory (DFT) based quantum transport simulations of nanoscale field effect transistors made of Ge, Si, strained-Si, and few-layer black phosphorus channels. The effects of atomistically modeled, crystalline/amorphous SiO2 gate dielectrics on device performance are investigated. A spectral adjustment technique is developed to overcome the band gap underestimation problem of DFT and applied to simulations of tunnel field effect transistors.

2:25 PM

35.3 Dopant diffusion in Si, SiGe and Ge : TCAD model parameters determined with density functional theory, *Y. Park, C. Zechner*, Y. Oh**, H. Kim,; I. Martin-Bragado**, E. M. Bazizi, and F. Benistant, GLOBALFOUNDRIES, *Synopsys GmbH, **Synopsys Inc.*

We used density functional theory (DFT) to calculate TCAD parameters to describe dopant diffusion in Si, SiGe and Ge. The dopant profile simulated in TCAD with calculated parameters is in good agreement with experiment. It is demonstrated that DFT could help to get unknown TCAD parameters and provide valuable insights on the parameter relations supporting experimental data.

2:50 PM
35.4 First Topography Simulation of SiC-Chemical-Vapor-Deposition Trench Filling, Demonstrating the Essential Impact of the Gibbs-Thomson Effect, *K. Mochizuki, S. Ji, R. Kosugi, Y. Yonezawa, and H. Okumura, National Institute of Advanced Industrial Science and Technology*

A technology-computer-aided-design-based topography-simulation model is proposed to simulate chemical-vapor-deposition trench filling for SiC superjunction devices. Experimental observations, concerning void formation and mesa overetching, are reproduced for the first time by including the Gibbs-Thomson effect (i.e., the effect of curvature of a growing surface on equilibrium vapor-phase concentration of growing species).

3:15 PM
35.5 A Physics-Based Investigation of Pt-Salt Doped Carbon Nanotubes for Local Interconnects, *J. Liang, R. Ramos*, J. Dijon*, H. Okuno**, D. Kalita**, D. Renaud*, J. Lee***, V. P. Georgiev***, S. Berrada***, T. Sadi***, A. Asenov***, B. Uhlig^, K. Lilienthal^, A. Dhavamani^, F. Könemann^^, B. Gotsmann^^, G. Goncalves^^^, B. Chen^^^, K. Teo^^^, R. R. Pandey, and A. Todri-Sanial, CNRS/LIRMM-University of Montpellier, *University Grenoble Alpes/CEA-LITEN, **University Grenoble Alpes/CEA-INAC, ***University of Glasgow, ^Fraunhofer IPMS, ^^IBM Research Zurich, ^^^Aixtron Ltd.*

We investigate, by combining physical and electrical measurements together with an atomistic-to-circuit modeling approach, the conductance of doped carbon nanotubes (CNTs) and their eligibility as possible candidate for next generation back-end-of-line (BEOL) interconnects. Ab-initio simulations predict a doping-related shift of the Fermi level, which reduces shell chirality variability and improves electrical conductance up to 90% by converting semiconducting shells to metallic. Circuit-level simulations predict up to 88% signal delay improvement with doped vs. pristine CNT. Electrical measurements of Pt-salt doped CNTs provide up to 50% of resistance reduction which is a milestone result for future CNT interconnect technology.

Session 36: Nano Device Technology - Device Technologies for Disruptive Computing
Wednesday, December 6
Continental Ballroom 4
Co-Chairs: Heike Riel, IBM Research
Iuliana Radu, imec

1:35 PM
36.1 MoS_2/VO_2 vdW heterojunction devices: tunable rectifiers, photodiodes and field effect transistors, *N. Oliva, E. A. Casu, C. Yan*, A. Krammer**, A. Magrez***, A. Schueler**, O. J. F. Martin* and A. M. Ionescu, Nanoelectronic Device Laboratory (Nanolab), *Nanophotonics and Metrology Laboratory (NAM), **Solar Energy and Building Physics Laboratory and ***Istitut de Physique, EPFL*

In this work we report a new class of ultra-thin film devices based on n-n van der Waals (vdW) heterojunctions of MoS2 and VO2, which show remarkable tunable characteristics. The favorable band alignment combined with the sharp and clean vdW interface determines a tunable diode-like characteristic with a rectification ratio larger than 103. Moreover, the heterojunction can be turned into a Schottky rectifier with higher on- current by triggering the VO2 insulator to metal transition (IMT), by either applying a sufficiently large voltage or increasing the temperature above 68 °C. The proposed devices are photosensitive with linear photoresponse and temperature tunable photoresponsivity values larger than 1 in the 500/650 nm wavelength range. We finally report the first ever field-effect transistor based on gated MoS2/VO2 heterojunctions, which is a true low power FET exploiting a phase change material where the electrostatic doping effect of the gate on the junction results in a subthreshold slope (SS) of 130 mV/dec at room temperature, ION/IOFF > 103 and IOFF < 5 pA/µm at VD=1.5V.

2:00 PM

36.2 A Single Magnetic-Tunnel-Junction Stochastic Computing Unit, *Y. Lv and J.-P. Wang, University of Minnesota*

We propose and experimentally demonstrate a stochastic computing unit with a single magnetic tunnel junction. It performs addition and multiplication operations and requires no additional logic gates. This scheme benefits from high energy efficiency of magnetic tunnel junction operated by spin-transfer torque or other future switching mechanisms, and error tolerance, low complexity and low area cost of stochastic computing.

2:25 PM
36.3 Neuromorphic Computing through Time-Multiplexing with a Spin-Torque Nano-Oscillator (Invited), *M. Riou, F. Abreu Araujo, J. Torrejon, S. Tsunegi*, G. Khalsa**, D. Querlioz**, P. Bortolotti, V. Cros, K. Yakushiji*, A. Fukushima*, H. Kubota*, S. Yuasa*, M. D. Stiles**, and J. Grollier, CNRS, Univ. Paris-Sud, Université Paris-Saclay, *National Institute of Advanced Industrial Science and Technology (AIST), **National Institute of Standards and Technology*

Fabricating powerful neuromorphic chips the size of a thumb requires miniaturizing their basic units: synapses and neurons. The challenge for neurons is to scale them down to submicrometer diameters while maintaining the properties that allow for reliable information processing: high signal to noise ratio, endurance, stability, reproducibility. In this work, we show that compact spin-torque nano-oscillators can naturally implement such neurons, and quantify their ability to realize an actual cognitive task. In particular, we show that they can naturally implement reservoir computing with high performance and detail the recipes for this capability.

2:50 PM
36.4 STDP synapse with outstanding stability based on a novel insulator-to-metal transition FET, *P. Stoliar, A. Schulman, A. Kitoh, A. Sawa and I. H. Inoue, 1National Institute of Advanced Science and Technology (AIST)*

We have developed an ultra-stable STDP synapse based on a gate-controlled insulator-to-metal- transition FET. Since a metallic channel is used, stochastic phenomena have little effect; therefore, the distinguished stability with a large dynamic range and with a very low power consumption is realized.

3:15 PM
36.5 All-electrical universal control of a double quantum dot qubit in silicon MOS, *P. Harvey-Collard, R. M. Jock*, N. T. Jacobson*, A. D. Baczewski*, A. M. Mounce*,M. J. Curry*, D. R. Ward*, J. M. Anderson*, R. P. Manginell*, J. R. Wendt*, M. Rudolph*, T. Pluym*, M. P. Lilly*, M. Pioro-Ladrière and M. S. Carroll*, Université de Sherbrooke, *Sandia National Laboratories*

Qubits based on transistor-like Si MOS nanodevices are promising for quantum computing. In this work, we demonstrate a double quantum dot spin qubit that is all-electrically controlled without the need for any external components, like micromagnets, that could complicate integration. Universal control of the qubit is achieved through spin-orbit-like and exchange interactions. Using single shot readout, we show both DC- and AC-control techniques. The fabrication technology used is completely compatible with CMOS.

Session 37: Process and Manufacturing Technology - Advanced Transistor Technologies
Wednesday, December 6
Continental Ballroom 5
Co-Chairs: Han-Su Oh, Samsung
Sandy Liao, Intel

1:35 PM
37.1 Sub-nm EOT Ferroelectric HfO_2 on p^+Ge with Highly Reliable Field Cycling Properties, *X. Tian, L. Xu, S. Shibayama, T. Nishimura, T. Yajima, S. Migita* and A. Toriumi, The University of Tokyo, *National Institute of Advanced Industrial Science & Technology (AIST)*

5-nm-thick ferroelectric Y-doped HfO2 was intensively studied. The thickness dependence of ferroelectric properties indicates that stable ferroelectric characteristics are maintained down to 5-nm-thick by taking care of doping and capping effects. Furthermore, the cycling performance shows no wake-up behavior, no obvious degradation after 108 cycles. These

results not only enable us to use ferroelectric HfO2 for practical application, but also point out intrinsic properties in ultrathin ferroelectric HfO2 film from materials science point of view.

2:00 PM
37.2 A Comparative Study of Strain and Ge Content in $Si_{1-x}Ge_x$ Channel using Planar FETs, FinFETs, and Strained Relaxed Buffer Layer FinFETs, *C. H. Lee, S. Mochizuki, R. G. Southwick III, J. Li, X. Miao, R. Bao, T. Ando, R. Galatage*, S. Siddiqui*, C. Labelle*, A. Knorr*, J. H. Stathis, D. Guo, V. Narayanan, B. Haran, and H. Jagannathan, IBM Research and *GLOBALFOUNDRIES Inc.*

Strained Si1-xGex channel pFinFETs and planar pFETs are fabricated on a strain relaxed buffer virtual substrate to comparatively study the electrical impact of strain and Ge content in the Si1-xGex channel. By comparing the transistor electrical properties of Si1-xGex pFETs on SRB with Si1-xGex pFETs on Si substrate, we successfully decouple the influence of strain and Ge content in the Si1-xGex channel on device performance such as gate stack quality, reliability, and carrier transport. Based on these understandings, dual channel Si/Si1-xGex FinFETs on the SRB with the optimized surface orientation is proposed to further improve the device performance.

2:25 PM
37.3 High Performance and Reliable Strained SiGe PMOS FinFETs Enabled by Advanced Gate Stack Engineering (Invited), *P. Hashemi, T. Ando, E. A. Cartier, K.-L. Lee, J. Bruley, C.-H. Lee, and V. Narayanan, IBM T.J. Watson Research Center*

Gate-stack engineering is critical to enable high- performance high-Ge-content strained-SiGe FinFETs. In this paper, key process details to achieve optimized gate-first and RMG gate-stacks are disclosed and devices with near-ideal SS, excellent NBTI, mobility and transconductance at scaled-EOTs are presented. Aggressively-scaled Fins with WFIN=6.4nm and excellent short-channel characteristics are also demonstrated.

2:50 PM
37.4 Vertically Stacked Gate-All-Around Si Nanowire Transistors: Key Process Optimizations and Ring Oscillator Demonstration, *H. Mertens, R. Ritzenthaler, V. Pena*, G. Santoro1, K. Kenis, A. Schulze, E. D. Litta, S. A. Chew, K. Devriendt, T. Chiarella, S. Demuynck, D. Yakimets, D. Jang, A. Spessot, G. Eneman, A. Dangol, P. Lagrain, H. Bender, S. Sun*, M. Korolik*, D. Kioussis*, M. Kim*, K-.H. Bu*, S. C. Chen*, M. Cogorno*, J. Devrajan*, J. Machillot*, N. Yoshida*, N. Kim*, K. Barla, D. Mocuta, N. Horiguchi, imec, *Applied Materials*

We report on CMOS-integrated vertically stacked gate-all-around Si nanowire MOSFETs with in-situ doped source-drain stressors and dual work function metal gates. We describe process improvements for shallow trench isolation, source-drain epitaxy, nanowire/nanosheet release, and NMOS VTH tuning. In addition, we report functional ring oscillators.

3:15 PM
37.5 First Vertically Stacked GeSn Nanowire pGAAFETs with I_{on}=1850µA/µm (V_{OV}=V_{DS}=-1V) on Si by GeSn/Ge CVD Epitaxial Growth and Optimum Selective Etching, *Y.-S. Huang, F.-L. Lu, Y.-J. Tsou, C.-E. Tsai,; C.-Y. Lin, C.-H. Huang, and C.W. Liu, National Taiwan University*

We demonstrate the first stacked GeSn pGAAFETs. Good crystalline quality and strong PL are achieved from CVD-grown stacked GeSn layers. With Ge barriers as sacrificial layers and optimum ultrasonic-assisted H2O2 etching technique, the stacked Ge0.9Sn0.1 channel with LCH=60nm has record high Ion=1850uA/um among all published GeSn pFETs with SS=88mV/dec.

Session 38: Memory Technology - STT-MRAM
Wednesday, December 6
Continental Ballroom 6
Co-Chairs: Luc Thomas, TDK-Headway Technologies
Gwan-Hyeob Koh, Samsung Electronics

1:35 PM

38.1 Threshold Switching Selector and 1S1R Integration Development for 3D Cross-point STT-MRAM, *H. Yang, X. Hao, Z. Wang, R. Malmhall, H. Gan, K. Satoh, J. Zhang, D. H. Jung, X. Wang, Y. Zhou, B. K. Yen and Y. Huai, Avalanche Technology*

We present a bi-directional threshold switching selector and integrated one selector/one perpendicular MTJ (1S1R) device. The selector shows above 1E+7 On/Off ratio, 1 pA leakage current, 0.3 V threshold voltage, and fast speed (10 ns). Switching operations between "AP" and "P" state have been demonstrated for the 1S1R STT-MRAM device.

2:00 PM
38.2 MRAM: Enabling a Sustainable Device for Pervasive System Architectures and Applications (Invited), *S. Kang and C. Park, Qualcomm Technologies, Inc.*

MRAM, specifically, perpendicular spin-transfer-torque (STT) MRAM, has reached a stage to serve early adopters. With its unique attributes and tunability, MRAM can create desirable system differentiations which were not possible due to inherent limitations of various memories. MRAM is poised for a unified memory subsystem that can revamp the archi-tectures of emerging ultra-low-energy systems such as Inter-net-of-Things (IOT) and wearable devices. Furthermore, MRAM has a potential to transform computing-centric archi-tectures at more advanced nodes.

2:25 PM
38.3 Key Parameters Affecting STT-MRAM Switching Efficiency and Improved Device Performance of 400ºC-Compatible p-MTJs, *G. Hu, M. G. Gottwald, Q. He, J. H. Park, G. Lauer, J. J. Nowak, S. L. Brown, B. Doris, D. Edelstein, E. R. Evarts, P. Hashemi, B. Khan, Y. H. Kim, C. Kothandaraman, N. Marchack, E. J. O'Sullivan, M. Reuter, R. P. Robertazzi, J. Z. Sun, T. Suwannasiri, P. L. Trouilloud, Y. Zhu and D. C. Worledge, IBM-Samsung MRAM Alliance, IBM TJ Watson Research Center*

We report the impact of four key parameters on switching efficiency of STT-MRAM devices with perpendicular magnetic anisotropy: device size, device resistance-area product (RA), blanket film Gilbert damping constant (α), and process temperature. Performance degradation observed in 400ºC-processed devices was eliminated by optimizing the perpendicular magnetic tunnel junction (p-MTJ) materials. Furthermore, 400ºC-compatible double MTJs were developed for the first time and showed 1.5x improvement in switching efficiency compared to single MTJs with identical free layers.

2:50 PM
38.4 Probing magnetic properties of STT-MRAM devices down to sub-20 nm using Spin-Torque FMR, *L. Thomas, G. Jan, S. Le, S. Serrano-Guisan, Y.-J. Lee, H. Liu, J. Zhu, J. Iwata-Harms, R.-Y. Tong, S. Patel, V. Sundar, D. Shen, Y. Yang, R. He, J. Haq, Z. Teng, V. Lam, P. Liu, Y.-J. Wang, T. Zhong, and P.-K. Wang*
TDK- Headway Technologies, Inc.

Scaling STT-MRAM cells beyond 1X technology node will require MTJ devices smaller than 30 nm. For such small sizes, process-induced damage becomes a primary factor of device performance. A robust method of assessing magnetic properties of sub-30 nm devices is thus needed. Here we report measurements of the anisotropy field HK down to 20 nm devices using ST-FMR. We show that HK increases for decreasing sizes. The interfacial anisotropy field exceeds 23 kOe, leading to HK larger than 13 kOe for 20 nm devices under optimal process conditions. Using insight from micromagnetic simulations, we develop a simple model to fit HK size dependence, allowing us to quantify magnetic edge damage for various process conditions.

3:15 PM
38.5 Novel approach for nano-patterning magnetic tunnel junctions stacks at narrow pitch: A route towards high density STT-MRAM applications, *V. D. Nguyen, P. Sabon, J. Chatterjee, L. Tille , P. Veloso Coelho, S. Auffret, R. Sousa, L. Prejbeanu, E. Gautier, L. Vila and B. Dieny, Grenoble Alpes University*

Etching magnetic tunnel junction (MTJ) cells at low dimension and very dense pitch remains challenging for high density STT-MRAM. This paper demonstrates a novel scalable approach for MTJ nano-patterning at very narrow pitch (pitch=1.5F, F=MTJ dot diameter) by growing the MTJ material on pre-patterned conducting non-magnetic pillars without post-deposition etching.

3:40 PM

38.6 Solving the BEOL compatibility challenge of top-pinned magnetic tunnel junction stacks, *J. Swerts, E. Liu, S. Couet, S. Mertens, S. Rao, W. Kim, K. Garello, L. Souriau, S. Kundu, D. Crotti, F. Yasin, N. Jossart, S. Sakhare, T. Devolder*, S. Van Beek, B. O'Sullivan, S. Van Elshocht, A. Furnemont, G.S. Kar, imec, * Univ. Paris-Sud, Univ. Paris-Saclay*

We report for the first time 400°C compatible top- pinned perpendicular magnetic tunnel junction stacks. High TMR of 180% at RA 9 Ohm.µm2 is demonstrated. A new synthetic ferromagnetic stack pinning layer design is used to demonstrate free layer off-set control and low current switching in 30nm CD devices.

Session 39: Characterization, Reliability and Yield - Advanced Reliability Characterization and Circuits
Wednesday, December 6
Imperial Ballroom A
Co-Chairs: Miaomiao Wang, IBM
Dimitri Linten, imec

1:35 PM
39.1 Non-filamentary (VMCO) memory: a two- and three-dimensional study on switching and failure modes, *U. Celano, C. Gastaldi, S. Subhechha, B. Govoreanu, G. Donadio, A. Franquet, T. Ahmad*, C. Detavernier*, O. Richard, H. Bender, L. Goux, G. S. Kar, P. van der Heide and W. Vandervorst, imec, *University of Ghent*

In this work, for the first time, a set of two- and three-dimensional (3D) analysis techniques are combined to clarify the nature of resistive switching (RS) in state-of-the-art TiO2-based vacancy modulated conductive oxide (VMCO) memory.

2:00 PM
39.2 Ultra Fast (<1 ns) Electrical Characterization of Self-heating Effect and Its Impact on Hot Carrier Injection in 14nm FinFETs, *Y. Qu, X. Lin, J. Li, R. Cheng, X. Yu, Z. Zheng, J. Lu*, B. Chen and Y. Zhao, Zhejiang University, *Hunan University*

We demonstrate electrical characterizations within sub- 1 ns to investigate the self-heating effect (SHE) in 14 nm FinFETs, for the first time. Thanks to the extremely fast I-V measurement speed (~500 ps), the heat generation and dissipation process in the transistor channel are precisely captured.

2:25 PM
39.3 An Ultra-Dense Irradiation Test Structure with a NAND/NOR Readout Chain for Characterizing Soft Error Rates of 14nm Combinational Logic Circuits, *S. Kumar, M. Cho*, L. Everson, H. Kim, Q. Tang, P. Mazanec, P. Meinerzhagen*, A. Malavasi*, D. Lake*, C. Tokunaga*, M. Khellah*, J. Tschanz*, S. Borkar*, V. De* and C. H. Kim, University of Minnesota, *Intel Corporation*

This paper describes a 14nm test chip employing a novel NAND/NOR readout chain for characterizing soft error rate (SER) in combinational logic gates. The proposed circuit is compact, has a scalable architecture and incurs minimal area overhead. Different gate configurations (device size, threshold voltage, fan-out and chain length) were implemented in the 14nm test-chip and irradiated under a neutron beam to collect a massive amount of statistical data. Radiation data captures, for the first time, the impact of various circuit parameters on combinational logic SER in 14nm tri-gate technology.

2:50 PM
39.4 Investigation of Statistical Retention of Filamentary Analog RRAM for Neuromophic Computing, *M. Zhao, H. Wu, B. Gao, Q. Zhang, W. Wu, S. Wang, Y. Xi, D. Wu, N. Deng, S. Yu*, H.-Y. Chen**, and H. Qian, Tsinghua University, *Arizona State University, **GigaDevice Semiconductor Inc.*

The retention requirements of analog RRAM for neuromorphic computing applications are quite different from conventional RRAM for memory applications. Meanwhile, filamentary analog RRAM exhibits different retention behavior in comparison to strong-filament RRAM. For the first time, the statistical behaviors of read current noise and retention in a 1Kb filamentary analog RRAM array are investigated in this work. The conductance distribution of different levels is found to change with time, and the physical mechanism of the retention degradation is elucidated. From the experimental data, a compact model is developed in order to predict the statistical conductance evolution, which can effectively evaluate the impact of read noise and retention degradation in neuromorphic computing systems.

3:15 PM

39.5 Combatting IC Counterfeiting Using Secure Chip Odometers (Invited), *N. E. Can Akkaya, B. Erbagci, and K. Mai, Carnegie Mellon University*

To combat IC counterfeiting, a secure chip odometer was designed to provide ICs with both a secure gauge of use/age and an authentication of provenance enabling simple, secure, robust differentiation between genuine and counterfeit parts. The secure chip odometers employ chained one-shot binary aging elements (BAEs) that use intentional accelerated device aging to measure use and age of the chip. A prototype secure odometer was taped out on a 1.2mm x 1.7mm testchip in a 65nm bulk CMOS process as a proof-of-concept.

Session 40: Sensors, MEMS, BioMEMS - MEMS for Internet-of-Things (IoT)

Wednesday, December 6
Imperial Ballroom B
Co-Chairs: Jun-Bo Yoon, KAIST
Songbin Gong, University of Illinois at Urbana Champaign

1:35 PM

40.1 High-*Q* Silicon Fin Bulk Acoustic Resonators for Signal Processing Beyond the UHF, *M. Ramezani, M.Ghatge, and R. Tabrizian, University of Florida*

This paper reports, for the first time, on the silicon Fin Bulk Acoustic Resonator (FinBAR) technology that enables extreme scaling of integrated signal processing beyond the ultra- high-frequency (UHF) regime. High-aspect-ratio fins are etched in silicon substrate and covered by aluminum nitride films to enable efficient electromechanical transduction of bulk acoustic resonance modes with large coupling coefficient (kt2). The low phononic dissipation of single crystal silicon, along with suppression of piezoelectric charge redistribution loss in the sidewall transduction result in unprecedentedly high quality-factors (Q) in ultra- and super-high- frequency (SHF) regimes. A prototype FinBAR is presented operating in 3rd and 9th width- extensional modes at 2 GHz and 6 GHz, with Q of 4, 2017800 and 2,300, and kt2 of %1.2 and %0.5, 2017 respectively. The resulting record f×Q of 1.4×1013, the large kt2×Q of 58, and lithographical frequency scalability demonstrate the potential of FinBARs to realize SHF acoustic processors for emerging 5G multi-frequency systems.

2:00 PM

40.2 Monolithically 3D-Printed Pressure Sensors for Application in Electronic Skin and Healthcare Monitoring, *J. Yoon, B. Choi, Y. Lee, J. Han, J. Lee, J. Park, Y. Kim, D. M. Kim, D. H. Kim, M.-H. Kang*, S. Kim**, and S.-J. Choi, Kookmin University, *National Nanofab Center (NNFC), **Sejong University*

The monolithically 3D-printed pressure sensor with excellent sensing performance was demonstrated. The porous-structured dielectric was formed by casting an elastomer prepolymer into 3D-printed water-soluble templates. The flexible electrodes were monolithically 3D-printed using a conductive thermoplastic as well. Finally, our sensors were applied to the e-skin and wearable healthcare monitoring system.

2:25 PM

40.3 A Novel Triboelectric Nanogenerator with High Performance and Long Duration Time of Sinusoidal Current Generation, *W.-G. Kim, D. Kim*, S.-B. Jeon, S.-J. Park, I.-W. Tcho, H. Im, and Y.-K. Choi, KAIST, *Kyung Hee University*

A triboelectric nanogenerator composed of porous conductive-polymer and PTFE wrapping wires, is demonstrated. The proposed TENG generated a short- circuit current for a long duration and great output performance. Modeling based on parallel connection of the finite capacitors was accomplished. Proposed modeling is validated by comparison between experiment and calculated results.

2:50 PM

40.4 MEMS Heterogeneous Packaged Broadband Electromagnetic Induction Vibration Sensor and Remote Temperature Sensor for Industrial Intelligent Manufacturing, *Y.-S. Lai, S.-H. Hsu, C.-C. Chen, M. Li, J.-M. Lu, H.-C. Cheng, J.-M. Liu, Y.-C. Chen, Y.-T. Tuan, C.-S. Wu, J.-M. Shieh, and W.-K. Yeh, National Nano Device Laboratories, National Applied Research Laboratories*

In this work, heterogeneous integration the self- powered broadband (20 Hz ~ 2000 Hz) electromagnetic-induced vibration sensor and the remote temperature sensor possessing ultra-low power consumption (< 1 uWatt) with the first stage read-out circuit by MEMS compact packaging for continual investigation in industrial intelligent manufacturing is provided and demonstrated first time.

3:15 PM
40.5 An Integrated Plasmonic Refractive Index Sensor: Al nanohole arrays on Ge PIN photodiodes, *L Augel, S. Bechler, R. Körner, M. Oehme, J. Schulze, and I. A. Fischer, University of Stuttgart*

Collinear refractive index sensors offer highest sensitivities at smallest device foot-print. Using a complementary metal-oxide-semiconductor compatible process for fabrication paves the way to cheap devices enabling integrated biosensors. We present a vertical Ge PIN photodiode equipped with Al nanohole arrays placed directly on top of the diode. The interaction of plasmonic resonances and thin-film reflection within the PIN layer stack enables sensitivities comparable to Au sensing systems showing FOM* up to 14.

Standing from left to right: Rihito Kuroda, Optoelectronics, Displays, and Imagers Chair, Meng-Fan (Marvin) Chang, Memory Technology Chair, Curtis Tsai, Circuit and Device Interaction Chair, Masao Inoue, Process and Manufacturing Technology Chair, Jungwoo Joh, Characterization, Reliability and Yield Chair, Ken Rim, Technical Program Chair, Stefan De Gendt, General Chair, Mariko Takayanagi, Technical Program Vice Chair, Suman Banerjee, Publicity Vice Chair, Suman Datta, Short Course Chair, Jan Hoentschel, European Arrangements Vice Chair, Merlyne de Souza, Focus Session Chair, Polly Hocking, Conference Planner

Second row standing from left to right: Martin Giles, Publications Chair, Clemens Ostermaier, Power Devices / Compound Semiconductor and High Speed Devices Chair, Kirsten Moselund, European Arrangements Chair, Tibor Grasser, Exhibits Chair, Denis Rideau, Modeling and Simulation Chair, Shyh-Horng Yang, Asian Arrangements Chair, Barbara De Salvo, Publicity Chair, Séverine Le Gac, Sensors, MEMS, and BioMEMS Chair, Dina Triyoso, Short Course Vice Chair, Phyllis Mahoney, Conference Manager, Su Jin Ahn, Tutorial Chair, Yoosang Hwang, Asian Arrangements Chair

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