



2016 IEDM Conference Proceedings



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Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

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- YouTube: <https://www.youtube.com/channel/UC9X-8YPHtsy3SMQwU0yZdTg>
- Wikipedia: https://en.wikipedia.org/wiki/International_Electron_Devices_Meeting

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Topics of Interest

CIRCUIT AND DEVICE INTERACTION (CDI)

Papers are solicited in all areas of semiconductor platform technologies, and circuit, design, and device technology interactions. Platform technologies include CMOS and compound semiconductors, and other novel underlying technologies. Topics include digital, analog device, and circuit performance and scaling issues, technology-design co-optimization, power performance-area analysis, impact of future device structures on circuit design, implication of circuit and architecture on interconnects, and issues such as design for manufacturability and process control as well as concepts for future circuit design and technology including neuromorphic and non-von Neumann circuit approaches. Submission of papers covering advanced device technology and design interactions such as variability, power constraints, physical layout effects in memory, logic, analog, and mixed-signal circuit issues and design complexity are encouraged.

CHARACTERIZATION, RELIABILITY and YIELD (CRY)

Papers are solicited in all areas of characterization, yield, and reliability, at both the front-end and back-end of the process. Topics include hot carriers, high-k and low-k dielectric wear-out and breakdown, process charging damage, latch-up, ESD, soft errors, noise and mismatch behavior, variability/reliability interaction and time dependent variability, bias temperature instabilities, and thermal modeling at the device, circuit, and packaging level. Other topics include interconnect reliability, electromigration, the impact of back-end processing on devices, chip-package interaction, physics of failure analysis, reliability issues for memory, logic, and 3D technologies, and novel characterization techniques.

Compound Semiconductor and High Speed Devices (CHS)

Papers are solicited in the areas of compound semiconductor (GaAs, InGaAs, InP, GaN, SiC, SiGe, Antimonides and their related alloys, etc.) electronic devices and high-speed device technologies. Topics include III-V MOS devices and device physics, high speed devices, ballistic devices, and RF passives. Devices of interest include HBTs (III-V and group IV) and HEMTs, RF/microwave/millimeter-wave devices, SAW/BAW devices, and active and passive electron devices for analog applications.

MEMORY TECHNOLOGY (MT)

Papers are solicited covering all memory related technology topics, including devices for neuromorphic computing applications. Topics span the full range from novel cell concepts to fully integrated memories and manufacturing issues. Areas of interest include cell design and scaling, processing, reliability, and modeling for both volatile and nonvolatile memories, as well as conventional and novel memory cells including ReRAM, STT-MRAM, PCRAM, crosspoint and selectors, organic memory and NEMS-based devices. Devices and physics of memristors and other device concepts that support neural computing paradigms are also of interest. Higher level topics include array optimization, 3D architectures, novel read/program/erase schemes, solid state drive (SSD) applications, novel hierarchies and architectures for memory-centric systems, and disruptive non-volatile memory-enabled emerging logic applications.

MODELING and SIMULATION (MS)

Papers are solicited on analytical, numerical, and statistical approaches to modeling of electronic, optical, organic, and hybrid devices (including sensors), and their isolation and interconnection. Topics include physical and compact models for devices (including high voltage and power), materials modeling, modeling of fabrication processes and equipment, process characterization, parameter extraction, compact models for advanced technologies and novel devices, performance evaluation, design for manufacturing, reliability, variability, and technology benchmarking methodologies. Other topics include modeling of interactions between process, device, and circuit design. Submissions should advance the art of modeling and simulation or apply existing techniques to gain new insights into devices.

NANO DEVICE TECHNOLOGY (NDT)

Papers are solicited on novel solid state and nanoelectronic devices and concepts. This includes devices based on novel transport mechanisms such as tunnel FETs and other steep-slope devices, molecular devices, and emerging concepts for devices based on topological insulators, phase transitions, quantum effects, and non-von Neumann devices. Non-charge based logic, magnetic logic, spintronics, plasmonics, and quantum computing are also of interest. Furthermore, nanoelectronic devices based on low-dimensional systems are encouraged, including 2D materials, nanowires, nanotubes, and quantum dots. Papers in NDT focus primarily on device physics and novel concepts; more mature “platform candidate” papers should be submitted to CDI.

OPTOELECTRONICS, DISPLAYS, and IMAGERS (ODI)

Papers are solicited on devices, structures, and integration for optoelectronics, photonics, displays, and imaging systems. Optoelectronic devices include photovoltaics, photonic bandgap structures and crystals, LEDs and lasers, as well as optoelectronic and photonic integrated circuits and optical interconnects. Papers on quantum photonics and photonic qubits for quantum computation are also of interest. Displays and imaging area topics include CMOS imagers, high-speed imagers, optoelectronic devices, CCDs, TFTs, organic, amorphous, and polycrystalline devices, as well as emissive and reflective displays. Submission of papers addressing flexible and/or stretchable electronics, printed electronics, fundamental performance differences between CMOS and CCD imagers, organic and inorganic displays, and covering new technology trends in imagers and displays are encouraged. Other relevant subjects include device/circuit design, fabrication, reliability, theory, and modeling.

POWER DEVICES (PD)

Papers are solicited on discrete and integrated power devices and modules using Si, diamond, and compound semiconductors. Papers exploring the system-level impact of power devices are also of interest. Topics of interest include power devices (FETs, superjunction devices, IGBTs, etc.), and materials (Si, SiC, GaN, Diamond, GaAs, AlN, Ga₂O₃, etc.), manufacturing processes, device design, modeling, and physics. Devices targeting the full range of power and power conversion applications, including hybrid vehicles, power supplies for computer and telecom, motor drives, utility and grid control, and wireless power transfer, are of interest.

PROCESS and MANUFACTURING TECHNOLOGY (PMT)

Papers are solicited on innovations in individual process modules, process integration schemes, and process control and manufacturing techniques that improve device or circuit performance or enable new product functionality. Examples of front-end process topics include substrates and isolation technologies, new transistor materials, integration of heterogeneous channel materials, multi-patterning and EUV lithography, self-assembly techniques, deposition and etch techniques, novel dielectrics and metal electrodes for transistor gate stacks and MIM capacitors, shallow junctions, and silicides. Examples of back-end process topics include conductor and barrier materials, low dielectric constant materials, contact and via processes, planarization, photonics-electronics integration on CMOS, and advanced packaging. Also of interest are topics such as emerging process modules, 3D integration, additive manufacturing for microelectronics, process and tool design to reduce variation, defect reduction in heterogeneous material systems, and process control strategies.

SENSORS, MEMS, and BioMEMS (SMB)

Papers are solicited in the area of sensors, sensor networks, micro electromechanical systems (MEMS), BioMEMS as well as NEMS-based logic devices. The sensors area includes TFT-based sensors and sensors for chemical, molecular, and biological detection including integrated biomedical sensing. Topics of interest in the MEMS and BioMEMS area include resonators and resonant sensors, RF MEMS, integrated inertial measurement units, integrated sensors and actuators, micro-optical devices, micro-fluidic and bio-electronic devices inspired or enabled by biomimetic structures, micro power generators, mechanical energy harvesting devices, optofluidic devices, and organic-inorganic hybrid-devices, with particular emphasis on new device concepts, integrated implementations, and complete sensor systems and networks.

Program

See the Program Download for all abstracts and speaker bios.

Tutorials

The tutorials are in their sixth year and are 90 minute stand alone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields, and facilitate understanding of the technical sessions. In contrast, the traditional short courses are intensive full-day events focused on a single technical topic.

The tutorial sessions will take place on Saturday, December 3rd. Three tutorials are given in parallel in two time slots, at 2:45 p.m. and 4:30 p.m. respectively.

Topics presented at 2:45 – 4:15 p.m.:

- The Struggle to Keep Scaling BEOL, and What We Can Do Next, Rod Augur, Distinguished Member of the Technical Staff, GlobalFoundries
- Physical Characterization of Advanced Devices, Robert Wallace, Univ. Texas at Dallas
- Spinelectronics: From Basic Phenomena to Magnetoresistive Memory (MRAM) Applications, Bernard Dieny, Chief Scientist, Spintec CEA

Topics presented at 4:30 p.m.-6:00 p.m.:

- Electronic Circuits and Architectures for Neuromorphic Computing Platforms, Giacomo Indiveri, Univ. of Zurich and ETH Zurich
- Present and Future of FEOL Reliability—from Dielectric Trap Properties to Reliable Circuit Operation, Ben Kaczer, Principal Scientist, Imec
- Embedded Systems and Innovative Technologies for IoT Applications, Ali Keshavarzi, Vice President of R&D, Cypress Semiconductor

Short Courses

Short Courses provide the opportunity to learn about important areas and developments, and to benefit from direct contact with world experts. Advance registration is recommended.

Short Course #1: Technology Options at the 5-Nanometer Node

Organizers: An Steegen, Sr. Vice President of Technology Development, imec and Dan Mocuta, Director of Logic Device and Integration, imec

Short Course #2: Design/Technology Enablers for Computing Applications

Organizer: John Chen, Vice President of Technology and Foundry Management, NVIDIA

Plenary Session

The IEDM plenary session on Monday, December 5th is an opportunity to recognize several individuals for their outstanding work and contributions to the field of electron devices. In 2016 the awardees include:

IEDM Awards

2015 Roger A. Haken Best Student Paper Award presented to Xiao Yu of the University of Tokyo, for the paper entitled, "Experimental Study on Carrier Transport Properties in Extremely-Thin Body Ge-on-Insulator (GOI) p-MOSFETs with GOI Thickness down to 2nm".

IEEE EDS Awards

EDS Paul Rappaport Award To: Stefano Ambrogio, Simone Balatti, Vincent McCaffrey, Daniel C. Wang, Daniele Ielmini For the paper entitled: "Noise-Induced Resistance Broadening in Resistive Switching Memory—Part I: Intrinsic Cell Behavior / Part II: Array Statistics"

EDS George E. Smith Award To: Xiaobing Mei, Wayne Yoshida, Mike Lange, Jane Lee, Joe Zhou, PoHsin Liu, Kevin Leong, Alex Zamora, Jose Padilla, Stephen Sarkozy, Richard Lai, William R. Deal For the paper entitled: "First Demonstration of Amplification at 1 THz Using 25nm InP High Electron Mobility Transistor Process"

2016 EDS Distinguished Service Award To: Renuka P. Jindal "To recognize and honor outstanding service to the Electron Devices Society"

2016 EDS Education Award To: Hiroshi Iwai "For providing high-quality engineering education for industry and academics worldwide"

2016 EDS J.J. Ebers Award To: Jaroslav Hynccek "For the pioneering work and advancement of CCD and CMOS image sensor technologies"

EDS Celebrated Members Award To: Mildred Dresselhaus "For fundamental contributions to the field of electron devices for the benefit of humanity"

2016 EDS PhD Fellowship To: Jiahao Kang, Hagyoul Bae, Chao-Yang (Michael) Chen "To promote, recognize and support PhD level study and research within the Electron Devices Society's field of interest"

2016 EDS Early Career Award To: Nagarajan Raghavan "To promote, recognize and support early career technical development within the Electron Devices Society's field of interest"

2016 IEEE/EDS Fellows

*This is a complete listing of the 2016 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2016 IEDM.

- Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, Netherlands
- Chong-Ping Chang, Applied Materials, Inc., Santa Clara, CA, USA
- Gilles Dambrine, IEMN- Institute of Electronic, CNRS, France
- Ananth Dodabalapur, University of Texas at Austin, Austin, TX, USA
- Ravindranath Droopad, Texas State University, San Marcos, TX, USA
- Mukta Farooq, IBM Corporation, Hopewell Jct, NY, USA
- Patrick Fay, University of Notre Dame, Notre Dame, IN, USA
- Patrick French, TU Delft- Delft University of Technology, Delft, Netherlands
- Tibor Grasser, Technische Universität Wien: TU Wien, Vienna, Austria
- Mark Hersam, Northwestern University, Evanston, IL, USA
- Qing-An Huang, Southeast University, Nanjing, China
- Adrian Ionescu, EPFL – École polytechnique fédérale de Lausanne, Lausanne, Switzerland
- Alvin Joseph, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA
- Jong Ho Lee, Seoul National University, Seoul, Korea
- Victor Lubecke, University of Hawaii at Manoa, Honolulu, HI, USA
- Jian-Guo Ma, Tianjin University, Tianjin, China
- Souvik Mahapatra, IIT- Indian Institute of Technology Bombay, Mumbai, India
- Sudip Mazumder, University of Illinois at Chicago, Chicago, IL, USA
- Ellis Meng, University of Southern California, Los Angeles, CA, USA
- Ajay Poddar, Synergy Microwave Corporation, Paterson, NJ, USA
- Leonard Register, The University Of Texas At Austin, Austin, TX, USA
- Akira Toriumi, University of Tokyo, Tokyo, Japan
- Ernest Wu, IBM Microelectronics- Avent, Inc., Essex Junction, VT, USA
- Xin Zhang, Boston University, Boston, Massachusetts, USA

Focus Sessions

IEDM 2016 will have special Focus sessions on

System-level impact of power devices – While there are forums that serve circuit experts for the exchange of ideas and the reporting of breakthroughs, there hasn't been a suitable forum for bringing device and circuit experts together to consider impacts at the system level, even though that would be fruitful due to the interactions of circuits and devices. IEDM aims to serve as the forum for their dialogue, and so this Special Focus Session has been organized. Papers are expected to explore the system-level impact of power devices, and also to describe various types of power devices targeting the full range of power/power conversion applications such as hybrid vehicles, utility and grid control, computing/telecom power supplies, motor drives, and wireless power transfer.

Wearable electronics and Internet of Things – Wearable technology offers great promise for communications, fitness tracking, health monitoring, speech therapy, elder care/assisted living and many other applications. This Special Focus Session has been organized to benchmark wearable electronics technologies, to address applications with comprehensive system demonstrations, and to learn industrial perspectives about the gaps, challenges and opportunities for wider uses of wearable and IoT technologies. Papers on flexible/stretchable electronics, MEMs, display devices, sensors, printed electronics, organic devices and 2-D material devices enabling wearables/IoT devices also will be featured.

Ultra high speed electronics – There have been many advances and breakthroughs in ultra-high-speed electronics for communications, security and imaging applications, but technology gaps continue to prevent spectrum above millimeter-wave frequencies from being fully used. This Special Focus Session has been organized to discuss, showcase and benchmark advanced ultra-high speed devices and circuits based on high-electron-mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs) and conventional CMOS devices; high-speed interconnect; antennas for ultra-high-speed systems; ultra-high-frequency oscillators; and to discuss other possible applications.

Quantum computing – As traditional CMOS scaling enters the post-Moore's Law era, quantum computing has emerged as a possible candidate for further device scaling because it exploits the laws of quantum physics and may make much more powerful computers possible. This Special Focus Session will explore relevant semiconductor-related fabrication issues and will brainstorm R&D directions for new materials, devices, circuits, and manufacturing approaches for the scalable integration of a large number of qubits with CMOS technology, operating at cryogenic temperatures for the realization of quantum computers.

MRAM Posters & Forum

With the rising interest of the microelectronics industry for STT-MRAM and spintronics in general, it is very important to strengthen the links between the IEEE Magnetics Society and the IEEE Electron Devices Society. The purpose is to contribute to reducing the cultural gap which still exists between the magnetism and microelectronics communities and thereby ease the penetration of magnetism based technology into the microelectronics industry. IEDM is the main annual conference of the EDS Society. After discussions with the IEDM organizers, it was agreed for the first time to organize a special poster session during IEDM 2016 which will be entirely dedicated to MRAM (MRAM materials/phenomena/ technology/testing, hybrid CMOS/MTJ technology and circuits, spin-logic). This session is technically organized by the IEEE Magnetics Society and is embedded in the IEDM conference. It appears as a special poster session on MRAM in the IEDM program. About 30 posters will be presented. This event will be a great opportunity to bring together experts in magnetism and in microelectronics. The list of accepted posters can be downloaded at the following address: <http://ieeemagnetics.org/>

Bernard DIENY and Bruce TERRIS, IEEE Magnetics Society

Technical Program

See the Program Download for all abstracts and speaker bios.

Monday — 9:00 a.m. - Noon

- Session 1 — Plenary Session

Monday - 1:30pm - 5:00pm

- Session 2: Circuit and Device Interaction — Advanced Platform Technologies
- Session 3: Compound Semiconductor and High Speed Devices — Compound Semiconductors for High Speed RF and Low Power Logic Applications
- Session 4: Memory Technology — RRAM, PRAM and Applications
- Session 5: Nano Device Technology — 1D and 2D Devices
- Session 6: Sensors, MEMS, and BioMEMS — Focus Session: Wearables for the Internet-of-Things (IoT)
- Session 7: Modeling and Simulation — Advanced Numerical and Compact Models

- Session 8: Optoelectronics, Displays, and Imagers — Imaging and Photon Counting Sensors
Monday 6:30 pm – 8:00 pm

- Grand Ballroom — RECEPTION

Tuesday - 9:00 am - 12:00 pm

- Session 9: Process and Manufacturing Technology — 3D Integration and BEOL
- Session 10: Power Devices — Power Semiconductor Device Technologies
- Session 11: Memory Technology — Charge Based Memories and Scaling
- Session 12: Nano Device Technology — Negative Capacitance and New Material MOSFETs
- Session 13: Optoelectronics, Displays, and Imagers — Focus Session: Quantum Computing
- Session 14: Modeling and Simulation — 2D Materials and Organic Electronics
- Session 15: Characterization, Reliability and Yield — FINFET and Nanowire Device Reliability
- Session 16: Circuit and Device Interaction — Resistive Device Designs for von-Neumann Computing and Beyond

Tuesday - 12:20 PM

- Grand Ballroom B — IEDM General Luncheon

Tuesday - 2:15 pm - 5:30 pm

- Session 17: Process and Manufacturing Technology — Silicon Based Advanced CMOS
- Session 18: Sensors, MEMS, and BioMEMS — Enhanced Sensing, Heterogeneous Integration and Wearables
- Session 19: Nano Device Technology — Tunnel and Nanowire FETs
- Session 20: Power Devices — Focus Session: System-level Impact of Power Devices
- Session 21: Characterization, Reliability and Yield — Reliability and Characterization of Memory Devices, Contacts and Interfaces
- Session 22: Optoelectronics, Displays, and Imagers — Optoelectronic Integration

Tuesday - 8:00 pm - 10:00 pm

- Continental 1-4 and 6-9 — 23 / 24 IEDM Evening Panel Session

Wednesday - 9:00 am - 12:00 pm

- Session 25: Process and Manufacturing Technology — Beyond Conventional CMOS
- Session 26: Sensors, MEMS, and BioMEMS — N/MEMS for Physical, Chemical, and Bio-sensing
- Session 27: Memory Technology — MRAM
- Session 28: Circuit and Device Interaction — Technology Elements for 5nm Logic Platform and Advanced Automotive/ IoT Applications
- Session 29: Compound Semiconductor and High Speed Devices — Focus Session: Ultra-High Speed Electronics
- Session 30: Modeling and Simulation — Steep Slope Devices and Nanowires
- Session 31: Characterization, Reliability and Yield — Reliability Modeling and Characterization of Dielectrics and Interfaces
- Session 32: Optoelectronics, Displays, and Imagers — Thin Film Transistors for Imaging and Displays

Wednesday - 12:30 p.m.

- Plaza A&B — Entrepreneurs Lunch at IEDM
- Session 33: Process and Manufacturing Technology — Ge Channel Devices
- Session 34: Nano Device Technology — Devices Based on Quantum and Resistive Switching Phenomena
- Session 35: Circuit Device Interaction — 3D Systems, Enabling Technologies and Characterizations
- Session 36: Modeling and Simulation — Materials and Interfaces

IEDM Luncheon

This year's distinguished speaker is Prof. Roberto Cingolani from the Istituto Italiano di Tecnologia, Genoa, Italy who will give a presentation titled "Translating evolution into technology: from biochemical robots to autonomous anthropomorphic machines".

Nature has developed a number of smart solutions to make very efficient living machines over billions of years: from antibodies, to plants to humans. Reproducing the characteristics of these systems in a machine is the way of choice to create robots which integrate perfectly inside our body and/or around ourselves, up to the ultimate challenge of reproducing the unique mind-body nexus of humans.

In this frame, the discussion will preliminarily address a general comparison between living and artificial systems today. Artificial antibodies, plantoid robots, animaloids and humanoids will be presented, addressing the main technological topics, namely: New materials and biodegradability, Sensing, Power Sources, Manufacturing, Mind and Computation and Human-robot interaction.

Awards to be Presented:

2016 IEEE Cleo Brunetti Award To: Akira Toriumi "For contributions to CMOS device design from materials engineering to device physics."

2016 IEEE Andrew S. Grove Award To: Carlos H. Díaz "For sustained contributions to and leadership in foundry advanced CMOS logic transistor technology."

2016 IEEE Frederik Philips Award To: Kelin J. Kuhn "For technical leadership in the development and implementation of breakthrough CMOS technology."

2016 IEEE David Sarnoff Award To: Hiroyuki Matsunami "For contributions to the development of silicon carbide (SiC) crystals and devices for advanced power electronics."

Evening Panel Discussion

The IEDM offers attendees two evening sessions where experts give their views on important industry topics. Audience participation is encouraged to foster an open and vigorous exchange of ideas.

How Will the Semiconductor Industry Change to Enable 50 Billion Connected Devices?

Moderator: Prof. Aaron Thean, University of Singapore

Challenges and Opportunities for Neuromorphic and Machine Learning,

Moderator: Marc Duranton, Sr. Member of the Embedded Computing Lab, CEA

Entrepreneurs Luncheon

Jointly sponsored by IEDM and IEEE Women in Engineering, the Entrepreneurs Lunch will feature Vamsee Pamula, co-founder of Baebies, Inc. a company developing digital microfluidics technology for newborn screening and pediatric testing. Pamula co-founded Baebies in 2014, following the sale of a predecessor microfluidics company that he also co-founded – Advanced Liquid Logic – to Illumina, Inc.

Vamsee has years of experience with digital microfluidics. He has served as Principal Investigator on several National Institutes of Health-funded projects, and has led many talks and published more than 60 articles, five book chapters and a book on the topic. He has more than 200 issued and pending patents, a PhD in Electrical and Computer Engineering from Duke University, and also serves as Adjunct Professor there.

Exhibits & Exhibit Events

For the first time, IEDM 2016 will host an Exhibits area during the conference where you can learn more about the latest products and publications. This will be open in the Yosemite Ballroom during the conference from Monday 12:00 pm, through Wednesday 12:00 pm. Stop by any time during the exhibition open hours to browse the booths and enjoy complementary coffee. The Exhibition will be open to all IEDM attendees as well as qualified Exhibit Only participants.



GLOBAL TCAD SOLUTIONS



Appendix - Abstracts, Bios & Technical Program

WELCOME FROM THE GENERAL CHAIR

On behalf of the entire IEDM committee, I would like to welcome you to the 2016 IEEE International Electron Devices Meeting to be held December 3-7, 2016 in San Francisco, CA. This will be the 62nd annual IEDM, and promises to continue the long tradition of being the world's premier venue for presenting the latest breakthroughs in electron device technologies.

This year's edition of IEDM will feature outstanding contributed and invited papers presented by industrial and academic leaders as well as students from around the world. An outline of the technical program and short summaries of all the papers are available on the IEDM web site, which we encourage everyone to visit – <http://www.ieee-iedm.org/>. We will continue to distribute an abbreviated digest at the meeting, along with the full digest in electronic format. An IEDM smartphone and tablet app that supports iPhone, iPad and Android platforms is also available. The full digest will also be available through IEEE Xplore after the conference.

The meeting's technical activities begin on Saturday afternoon, December 3, when we will continue to offer our highly successful tutorials. Now in their 6th year, these tutorials are targeted at students, engineers, or anyone who wants an introduction to, or review of, the basics of key electron device technologies. Three tracks run in parallel, for a total of six tutorial topics; see the [ieeedm.org](http://www.ieee-iedm.org/) website for full information. On Sunday, two comprehensive short courses will be offered: "Technology Options at the 5 nm Node", and "Design/Technology Enablers for Computing Applications." These full-day courses are organized and presented by internationally recognized researchers active in their respective areas of technology. The topics and instructors have been carefully chosen to have broad appeal to IEDM participants, and will include material suitable for both newcomers as well as experts.

The Plenary Session on Monday morning will feature three invited talks. Dr. Seok-Hee Lee from Hynix will give us his perspectives in a talk entitled "Technology Scaling Challenges and Opportunities of Memory Devices," followed by Dr. Dharmendra S. Mohda from IBM who will describe efforts to go beyond conventional computing paradigms in his talk "Brain-Inspired Computing." The final plenary talk, "Symbiotic Low-Power, Smart and Secure Technologies in the age of Hyperconnectivity" will be given by Dr. Marie-Noëlle Semeria from CEA-LETI.

In addition to the excellent contributed paper sessions, four special "Focus Sessions" will feature talks from leading experts in exciting new and rapidly-advancing areas. The topics of the focus sessions this year include the system-level impact of power devices, wearable electronics and the internet of things, ultra-high speed electronics, and quantum computing.

On Tuesday night, we will feature two interactive panel sessions that promise to be both relevant and engaging. The first panel: "How will the semiconductor industry change to enable 50 billion connected devices?" will be moderated by Aaron Thean from the Univ. of Singapore, while Marc Duranton from CEA will moderate the second panel: "Challenges and opportunities for neuromorphic and machine learning." I encourage you to check these out on Tuesday evening.

IEDM will also feature two informative and entertaining luncheons on Tuesday and Wednesday. The formal IEDM Luncheon on Tuesday will be given by Prof. Roberto Cingolani, from the Istituto Italiano di Tecnologia. Prof. Cingolani is well known for his work in robotics for a wide range of applications, and he will give a talk entitled "Translating evolution into technology: from biochemical robots to autonomous anthropomorphic machines" that promises to be both entertaining and extremely thought-provoking. Our highly successful Entrepreneurs Lunch Series held on Wednesday will feature Vamsee Pamula, who has founded several technology startup companies. His current role is as a founder of Baebies, Inc.—a startup based on using digital microfluidics for newborn and pediatric medical screening. He will share his thoughts and experiences in starting and running successful technology companies.

On behalf of Stefan De Gendt, Technical Program Chair, and Ken Rim, Technical Program Vice-Chair, as well as the entire IEDM committee, I want to express my sincere appreciation to all of the authors and speakers who contributed to the technical program. Your efforts are the engine that continues to make IEDM the premier conference in electron devices and related technologies. I also wish to thank each of the members of the IEDM executive and technical subcommittees whose dedication and efforts were critical in planning and organizing the 2016 conference.

IEDM is sponsored by the IEEE Electron Devices Society. If you are not already an IEEE member, please consider joining this great institution that has played such an important role globally for over 120 years. More detailed information regarding the IEEE is available at the conference and on their website – <http://www.ieee.org>.

It is again my great honor and pleasure to extend a warm welcome to everyone attending the 2016 IEEE International Electron Devices Meeting, and helping to celebrate our 62nd year.



Patrick Fay
General Chair



Stefan De Gendt
Technical
Program Chair



Ken Rim
Technical Program
Vice Chair

AWARD PRESENTATIONS

PLENARY SESSION AWARD

Monday, December 5

2015 Roger A. Haken Best Student Paper Award

To: Xiao Yu, The University of Tokyo

For the paper entitled: "Experimental Study on Carrier Transport Properties in Extremely-Thin Body Ge-on-Insulator (GOI) p-MOSFETs with GOI Thickness down to 2nm"

EDS Paul Rappaport Award

To: Stefano Ambrogio, Simone Balatti, Vincent McCaffrey, Daniel C. Wang, Daniele Ielmini

For the paper entitled: "Noise-Induced Resistance Broadening in Resistive Switching Memory—Part I: Intrinsic Cell Behavior / Part II: Array Statistics"

EDS George E. Smith Award

To: Xiaobing Mei, Wayne Yoshida, Mike Lange, Jane Lee, Joe Zhou, PoHsin Liu, Kevin Leong, Alex Zamora, Jose Padilla, Stephen Sarkozy, Richard Lai, William R. Deal

For the paper entitled: "First Demonstration of Amplification at 1 THz Using 25nm InP High Electron Mobility Transistor Process"

2016 EDS Distinguished Service Award

To: Renuka P. Jindal

"To recognize and honor outstanding service to the Electron Devices Society"

2016 EDS Education Award

To: Hiroshi Iwai

"For providing high-quality engineering education for industry and academics worldwide"

2016 EDS J.J. Ebers Award

To: Jaroslav Hynccek

"For the pioneering work and advancement of CCD and CMOS image sensor technologies"

EDS Celebrated Members Award

To: Mildred Dresselhaus

"For fundamental contributions to the field of electron devices for the benefit of humanity"

2016 IEEE/EDS Fellows

**This is a complete listing of the 2016 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2016 IEDM.*

Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, Netherlands

Chorng-Ping Chang, Applied Materials, Inc., Santa Clara, CA, USA

Gilles Dambrine, IEMN- Institute of Electronic, CNRS, France

Ananth Dodabalapur, University of Texas at Austin, Austin, TX, USA

Ravindranath Droopad, Texas State University, San Marcos, TX, USA

Mukta Farooq, IBM Corporation, Hopewell Jct, NY, USA

Patrick Fay, University of Notre Dame, Notre Dame, IN, USA
Patrick French, TU Delft- Delft University of Technology, Delft, Netherlands
Tibor Grasser, Technische Universität Wien: TU Wien, Vienna, Austria
Mark Hersam, Northwestern University, Evanston, IL, USA
Qing-An Huang, Southeast University, Nanjing, China
Adrian Ionescu, EPFL - École polytechnique fédérale de Lausanne, Lausanne, Switzerland
Alvin Joseph, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA
Jong Ho Lee, Seoul National University, Seoul, Korea
Victor Lubecke, University of Hawaii at Manoa, Honolulu, HI, USA
Jian-Guo Ma, Tianjin University, Tianjin, China
Souvik Mahapatra, IIT- Indian Institute of Technology Bombay, Mumbai, India
Sudip Mazumder, University of Illinois at Chicago, Chicago, IL, USA
Ellis Meng, University of Southern California, Los Angeles, CA, USA
Ajay Poddar, Synergy Microwave Corporation, Paterson, NJ, USA
Leonard Register, The University Of Texas At Austin, Austin, TX, USA
Akira Toriumi, University of Tokyo, Tokyo, Japan
Ernest Wu, IBM Microelectronics- Avent, Inc., Essex Junction, VT, USA

IEDM LUNCHEON

Tuesday, December 6

2016 IEEE Cleo Brunetti Award

To: Akira Toriumi

"For contributions to CMOS device design from materials engineering to device physics."

2016 IEEE Andrew S. Grove Award

To: Carlos H. Díaz

"For sustained contributions to and leadership in foundry advanced CMOS logic transistor technology."

2016 IEEE Frederik Philips Award

To: Kelin J. Kuhn

"For technical leadership in the development and implementation of breakthrough CMOS technology."

2016 IEEE David Sarnoff Award

To: Hiroyuki Matsunami

"For contributions to the development of silicon carbide (SiC) crystals and devices for advanced power electronics."

Tutorials
Saturday, December 3, 2016
2:45 – 6:00 p.m.

Topics Presented at 2:45 – 4:15 p.m.
Imperial A // Imperial B // Franciscan

The Struggle to Keep Scaling BEOL, and What We Can Do Next

Rod Augur, Distinguished Member of the Technical Staff, GlobalFoundries

Looking ahead, it's the interconnect that threatens further cost-effective scaling. The tutorial will cover challenges and trade-offs in back-end-of-the-line (BEOL) scaling, and will evaluate emerging devices from a scaled-BEOL viewpoint.

Physical Characterization of Advanced Devices

Robert Wallace, Univ. Texas at Dallas

This tutorial will cover the hardware, physics, and chemistry that enable modern physical characterization of novel electronic materials, and will explore how these techniques can shed light on electronic materials research and development, and on the resultant devices. In addition to introducing examples of novel electronic materials for device applications, example techniques discussed will include high-resolution electron microscopy, scanning tunneling microscopy and spectroscopy, dynamic x-ray photoelectron spectroscopy, and ion mass spectrometry. The detection limits of these techniques and how they relate to device behavior also will be discussed.

Spinelectronics: From Basic Phenomena to Magnetoresistive Memory (MRAM) Applications

Bernard Dieny, Chief Scientist, Spintec CEA

This tutorial will cover spintronics phenomena, magnetic tunnel junctions (growth, magnetic and transport properties), field-written MRAM (toggle and thermally assisted MRAM), STT-MRAM (principle and status of development), 3-terminal MRAM and innovative architectures that benefit from these high-endurance non-volatile memories.

Topics Presented at 4:30 – 6:00 p.m.
Imperial A // Imperial B // Franciscan

Electronic Circuits and Architectures for Neuromorphic Computing Platforms

Giacomo Indiveri, Univ. of Zurich and ETH Zurich

This tutorial will cover the principles and origins of neuromorphic (i.e., brain-inspired) engineering, examples of neuromorphic circuits, how neural network architectures can be used to build large-scale multi-core neuromorphic processors, and some specific application areas well-suited for neuromorphic computing technologies.

Present and Future of FEOL Reliability—from Dielectric Trap Properties to Reliable Circuit Operation

Ben Kaczer, Principal Scientist, imec

This tutorial will introduce the main degradation mechanisms occurring in present-day CMOS. The reliability of novel devices (SiGe, III-V, gate-all-around nanowires, junctionless FETs, tunnel FETs), of deeply-scaled devices, and of circuits (e.g., “reliability-aware” designs) will be covered in detail. The tutorial will give attendees an overview and background in this area sufficient to allow them to follow and participate in any discussion on reliability in general, and on front-end-of-the-line (FEOL) reliability in particular.

Embedded Systems and Innovative Technologies for IoT Applications

Ali Keshavarzi, Vice President of R&D, Cypress Semiconductor

Pervasive IoT systems are making our lives easier with an enhanced user experience in a variety of widely deployed applications. Sub-systems and features of IoT embedded microsystems and their key technical requirements will be described. Energy efficiency of the future intelligent IoT systems require balancing of computing and communication locally at the IoT node calling upon both Moore’s Law and Shannon’s Law in concert. Innovative technologies to create power-differentiated and cost-effective solutions for future IoT applications will be explained; including differentiated SONOS eNVM, low-power radios and small form-factor system-in-package technologies. We compare them with alternative competitive technologies and explore how participants’ future innovations can be integrated in IoT systems. eNVM is critical in enabling autonomous IoT systems that rely on intermittent source of energy for program, data, security and advanced networking protocols. Finally, we will demonstrate a low-energy IoT system for agriculture that uses solar energy harvesting and conclude by describing a vision of future IoT systems.

Short Course

Technology Options at the 5-Nanometer Node

Sunday, December 4, 2016, Continental 1-5
9:00 a.m. – 5:45 p.m.

Course Organizers: An Steegen and Dan Mocuta of imec (Sr. Vice President of Technology Development/Director of Logic Device and Integration, respectively)

This course will describe the complex technological challenges at the 5nm node and explore innovative potential solutions. It begins with an in-depth discussion of patterning strategies being pursued to print critical features. Then, a pair of lectures will provide an overview of current transistor technologies and their relative strengths/weaknesses in the context of various applications such as mobility, data centers and IoT. Strategies for effective mitigation of performance-limiting parasitic resistance and capacitance will be discussed, and advanced interconnect technologies including post-copper materials options for BEOL and MEOL applications will be addressed. Lastly, metrology challenges for in-line and end-of-line process technologies will be discussed. The intent of the course is to provide a thorough understanding in process technology targets at the 5nm node and their potential solutions. Attendees will have the opportunity to learn about advanced technology options that are being actively pursued in the industry from leading technologists.

The course consists of lectures from six distinguished speakers:

- **Patterning Technology for 5nm Node**, Akihisa Sekiguchi, VP & Deputy GM, SPE Marketing and Process Development Division, Tokyo Electron, Japan
- **Extending FinFETs to 5nm Node**, Nadine Collaert, Distinguished Member of the Technical Staff, imec, Belgium
- **Options Beyond FinFETs at 5nm Node**, Aaron Thean, Professor of Electrical & Computer Engineering, National University of Singapore
- **Front-End Parasitic Resistance Capacitance**, Reza Arghavani, Managing Director, Lam Research, USA
- **Back-End Parasitic Resistance and Capacitance Mitigation**, Theodorus Standaert, Sr. Engineering Mgr., Manager, Process Integration, IBM, USA
- **Advanced Metrology**, Ofer Adan, Technologist and Global Product Manager, Member of the Technical Staff, Applied Materials, Israel

Short Course

Design/Technology Enablers for Computing Applications

Sunday, December 4, 2016, Continental 6-9
9:00 a.m. – 5:30 p.m.

Course Organizers: John Chen, Vice President of Technology and Foundry Management, NVIDIA

This course will describe how various design techniques and process technologies can enable computing applications, beginning with the relative advantages and disadvantages of processors such as CPU, GPU and FPGA with regard to today's high data demands. It then will cover how memory becomes a bottleneck, and will discuss various emerging memory technologies to mitigate the problem. Because managing power dissipation has become critical, it also will offer a broad perspective on power efficiency in computing and how interconnect plays a pivotal role in both performance and energy efficiency. Finally, 2.5-D and 3-D advanced packaging technology is discussed for system integration.

The course consists of lectures from five distinguished speakers:

- **The Rise of Massively Parallel Processing: Why the Demands of Big Data and Power Efficiency are Changing the Computing Landscape**, Liam Madden, Corporate VP, Hardware & Systems Development, Xilinx, USA
- **Interconnect Challenges for Future Computing**, William J. Dally, Chief Scientist and Sr. VP of Research, NVIDIA, and Stanford Professor, USA
- **Breaking the Memory Bottleneck in Computing Applications with Emerging Memory Technologies: A Design Perspective (Circuit Level)**, Michael Harrand, Leti, France
- **Breaking the Memory Bottleneck in Computing Applications with Emerging Memory Technologies: A Technology Perspective (Device Level)**, Gabriel Molas, PhD Engineer, Leti, France
- **Power Management with Integrated Power Devices...and how GaN Changes the Story**, Alberto Doronzo, Power System/Apps Engineer, Texas Instruments, USA
- **Advanced Packaging Technologies for System Integration**, Douglas Yu, Sr. Director, TSMC, Taiwan

Plenary Session

Welcome and Awards

Monday, December 5, 9:00 a.m. Grand Ballroom B
General Chair: Patrick Fay, University of Notre Dame

Plenary Papers

Technical Program Chair: Stefan De Gendt, imec

1.1 Technology Scaling Challenges and Opportunities of Memory Devices

Seok-Hee Lee, SK hynix

Challenges in scaling of semiconductor memory technologies are reviewed with the focus on DRAM and NAND Flash while demands for memory improvement in the ICT industry are increasing. This paper introduces evolutionary and revolutionary paths to overcome scaling challenges and emerging memory technologies along with some promising solutions.

1.2 Brain-Inspired Computing

Dharmendra S. Modha, IBM

We present a comprehensive novel brain-inspired computing ecosystem consisting of scalable systems and software based on TrueNorth – a 70mW reconfigurable processor with 1 million neurons, 256 million synapses, and 4096 parallel and distributed neural cores; designed for homogeneous scaling via native chip-to-chip communication. For systems, we present: a scale-out system loosely coupling 16 single-chip boards and a scale-up system tightly integrating 16 chips in a 4×4 configuration by exploiting TrueNorth's native tiling. For software, we present an end-to-end ecosystem consisting of a simulator; a programming language; an integrated programming environment; a library of algorithms and applications; firmware; tools for deep learning; a teaching curriculum; and cloud enablement. The ecosystem is in use at over 40 universities, government agencies, and national/corporate labs. Our platform is a substrate for a spectrum of applications from mobile to embedded computing to cloud and could be a powerful complement in the development of next-generation exascale supercomputers. Our long-term goal is to build a "brain-in-a-box" with ten billion neurons, while consuming merely one kilowatt of power and occupying less than two liters of volume.

1.3 Symbiotic Low-Power, Smart and Secure Technologies in the Age of Hyperconnectivity

Marie-Noëlle Semeria, CEA – Leti

In the hyperconnectivity era, the relational-self, whose identity is based on the condition of plurality, becomes the symbolic representation of humanness in the world. Enabled by the convergence of miniaturization, wireless connectivity, increased data storage and data analytics, the Internet-of-Things is at the epicenter of this profound revolution. In this paper, we will present the disruptive technologies that build the hyperconnectivity value chain (i.e. sensing, communication, computing and storage, energy harvesting, security, services). We will focus on the need for energy efficiency, added-value to the users, simplicity in new services, and trustworthiness. We will show that a human-centered research approach and symbiotic development strategies along different technological axes lead to key innovations, able to respond to both growing individual needs and global societal challenges. Finally, biomimicry will be introduced as a possible new inspirational paradigm to design future cyber-physical systems.

Session 2: Circuit and Device Interaction - Advanced Platform Technologies

Monday, December 5, 1:30 p.m.

Grand Ballroom B

Co-Chairs: Jun Yuan, Qualcomm

Maarten Vertregt, NXP Semiconductors

1:35 PM

2.1 FPGA Design and System Optimizations with New Technologies (Invited), *N. Chong, J. Jing, H. Liu, G. Refai-Ahmed, S. Wu and X. Wu, Xilinx Inc.*

Recent new technologies, such as HK/MG, multi-patterning, 3D-IC, FinFET and SADP/SAQP, etc. have significant impacts to designs and architectures. Xilinx has been aware of these impacts, and actively improving its FPGA designs and

architectures, in order to take the benefits of these technologies while avoiding negative impacts. Several examples will be provided in this article.

2:00 PM

2.2 22nm FDSOI Technology for Emerging Mobile, Internet-of-Things, and RF Applications, R. Carter, J. Mazurier*, L. Pirro*, J.-U. Sachse, P. Baars, J. Faul, C. Grass, G. Grasshoff, P. Javorka, T. Kammler, A. Preusse, S. Nielsen, T. Heller, J. Schmid, H. Niebojewski*, P.-Y. Chou, E. Smith, E. Erben, C. Metze, C. Bao, Y. Andee*, I. Aydin*, S. Morvan*, J. Bernard*, E. Bourjot*, T. Feudel, D. Harame, R. Nelluri, H.-J. Thees, L. M. Meskamp, J. Kluth, R. Mulfinger, M. Rashed, R. Taylor, C. Weintraub, J. Hoentschel, M. Vinet*, J. Schaeffer and B. Rice, Globalfoundries, *CEA-LETI

22FDXTM is the industry's first FDSOI technology architected to meet the requirements of emerging mobile, Internet-of-Things (IoT), and RF applications. This platform achieves the power and performance efficiency of a 16/14nm FinFET technology in a cost effective, planar device architecture that can be implemented with ~30% fewer masks.

2:25 PM

2.3 First Fully Functionalized Monolithic 3D⁺ IoT Chip with 0.5 V Light-electricity Power Management, 6.8 GHz Wireless-communication VCO, and 4-layer Vertical ReRAM, F.-K. Hsueh, C.-H. Shen, J.-M. Shieh, K.-S. Li, H.-C. Chen, W.-H. Huang, H.-H. Wang, C.-C. Yang, T.-Y. Hsieh, C.-H. Lin, B.-Y. Chen, Y.-S. Shiao, G.W. Huang, O.-Y. Wong*, P.-H. Chen* and W.-K. Yeh, National Nano Device Laboratories, *National Chiao Tung University

For the first time, we report low-cost heterogeneously integrated sub-40nm epi-like Si monolithic internet of things (IoT) 3D⁺-IC with wireless communication, light-electricity power management and vertical ReRAM (VRRAM) modules. High current driving multi-channel 3D⁺ UTB-MOSFETs (2.7/1.5 mA/μm for N/P FETs) was fabricated by low thermal budget super-CMP-planarized visible laser-crystallized epi-like Si channel and CO₂ far-infrared laser annealing (CO₂-FIR-LA) activation technologies that support a 6.8GHz high frequency VCO circuits, 0.5V low-voltage power management circuit and drives 20nm 4-layer VRRAM (Set/Reset <1.2V/1.8V, 3-bits/cell). This unique TSV-free monolithic 3D⁺IC process provides the superiority in 3D hetero-integration; we successfully integrate these circuits in a low cost, small footprint, fully functionalized 3D⁺ IoT chip.

2:50 PM

2.4 A 300mm Foundry HRSOI Technology with Variable Silicon Thickness for Integrated FEM Applications, R. T. Toh, S. Parthasarathy, T. Sun, S. Zhang, R. V. Purakh, C. S. Zhu, V. S. Nune, J. S. Wong, M. Govindarajan, Y. K. Yoo, K. W. Chew and D. S. Ang*, GLOBALFOUNDRIES, *Nanyang Technological University

A novel approach to technology integration of system-on-chip RF Front-End Module (FEM) is presented. Device design to achieve best-in-class extended drain power mosfet (EDNMOS) with Ron of 1.6Ohm-mm and fT >39GHz is discussed. This is followed by an analysis of a high performance switch device integrated via selective silicon thinning.

3:15 PM

2.5 A 14nm Finfet Transistor-Level 3D Partitioning Design to Enable High-Performance and Low-Cost Monolithic 3D IC, J. Shi*, D. Nayak*, S. Banna*, R. Fox, S. Samavedam, S. Samal** and S. K. Lim**, University of Massachusetts at Amherst, *GLOBALFOUNDRIES, **Georgia Institute of Technology

The conventional monolithic 3D IC (M3D) shows performance degradation compared to 2D IC due to limited thermal budget in fabrication. A transistor-level (TR-L) partitioning design based M3D is used to mitigate this performance degradation and also enable lower cost compared to the conventional M3D that uses the gate-level partitioning scheme.

3:40 PM

2.6 A 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors with a 0.027μm² High Density 6-T SRAM Cell for Mobile SoC Applications (Late News), S.-Y. Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, S.H. Yang, C.H. Tsai, P.N. Chen, T. Miyashita, C.H. Chang, V.S. Chang, K.H. Pan, J.H. Chen, Y.S. Mor, K.T. Lai, C.S. Liang, H.F. Chen, S.Y. Chang, C.J. Lin, C.H. Hsieh, R.F. Tsui, C.H. Yao, C.C. Chen, R. Chen, C.H. Lee, H.J. Lin, C.W. Chang, K.W. Chen, M.H. Tsai, K.S. Chen, Y. Ku and S.M. Jang, TSMC

4:05 PM

2.7 A 7nm FinFET Technology Featuring EUV Patterning and Dual Strained High Mobility Channels (Late News), R. Xie, P. Montanini*, K. Akarvardar, N. Tripathi, B. Haran*, S. Johnson, T. Hook*, B. Hamieh*, D. Corliss*, J. Wang*, X. Miao*, J. Sporre*, J. Fronheiser, N. Loubet*, M. G. Sung, S. Sieg*, S. Mochizuki*, C. Prindle, S.-C. Seo*, A.

Greene*, J. Shearer*, A. Labonte, S. C. Fan*, L. Liebmann, R. Chao*, A. Arceo*, K. Chung*, K. Y. Cheon**, P. Adusumilli*, H. Amanapu*, Z. Bi*, J. Cha**, H.-C. Chen*, R. Conti*, R. Galatage, O. Gluschenkov*, V. Kamineni, K. Kim**, C. Lee*, F. L. Lie*, Z. Liu*, S. Mehta*, E. Miller*, H. Niimi, C. Niu, C. Park, D.-H. Park**, M. Raymond, B. Sahu, M. Sankarapandian*, S. Siddiqui, R. Southwick*, L. Sun, C. Surisetty*, S. Tsai, S. Whang**, P. Xu*, Y. Xu*, C.-C. Yeh*, P. Zeitzoff, J. Zhang, J. Li*, J. Demarest*, J. Arnold*, D. Canaperi*, D. Dunn*, N. Felix*, H. Jagannathan*, S. Kanakasabapathy*, W. Kleemeier, C. Labelle, M. Mottura, P. Oldiges*, S. Skordas*, T. Standaert*, T. Yamashita*, M. Colburn*, M.-H. Na*, V. Paruchuri*, S. Lian**, R. Divakaruni*, T. Gow*, S. Lee**, A. Knorr, H. Bu* and M. Khare*, GLOBALFOUNDRIES, *IBM, **Samsung

Session 3: Compound Semiconductor and High Speed Devices - Compound Semiconductors for High Speed RF and Low Power Logic Applications

Monday, December 5, 1:30 p.m.

Continental Ballroom 1-3

Co-Chairs: Lukas Czornomaz, IBM

Han Wui Then, Intel

1:35 PM

3.1 SiGe HBT with f_T/f_{max} of 505 GHz/720 GHz, B. Heinemann, H. Rücker, R. Barth, F. Bärwolf, J. Drews, G. Fischer, A. Fox, O. Fursenko, T. Grabolla, F. Herzel, J. Katzer, J. Korn, A. Krüger, P. Kulse, T. Lenke, M. Lisker, S. Marschmeyer, A. Scheit, D. Schmidt, J. Schmidt, M. A. Schubert, A. Trusch, C. Wipf, D. Wolansky, IHP

SiGe HBTs featuring $f_T/f_{max}/BV_{CEO} = 505 \text{ GHz}/720 \text{ GHz}/1.6 \text{ V}$ and a minimum CML ring oscillator gate delay of 1.34 ps are presented. The improved speed originates from an optimized vertical profile, the combined application of millisecond annealing and a backend with low thermal budget, as well as lateral device scaling.

2:00 PM

3.2 InGaAs Tri-gate MOSFETs with Record On-Current, C. Zota, F. Lindelow, L.-E. Wernersson, and E. Lind, Lund University

We demonstrate InGaAs tri-gate MOSFETs with an on-current of $I_{ON} = 650 \mu\text{A}/\mu\text{m}$ at $V_{DD} = 0.5 \text{ V}$ and $I_{OFF} = 100 \text{ nA}/\mu\text{m}$, enabled by an inverse subthreshold slope of $SS = 66 \text{ mV}/\text{decade}$ and transconductance of $g_m = 3 \text{ mS}/\mu\text{m}$, a Q-factor of 45. This is the highest reported I_{ON} for both Si-based and III-V MOSFETs. These results continue to push III-V MOSFET experimental performance towards its theoretical limit. We find an improvement in SS from 81 to 75 mV/dec. as the effective oxide thickness (EOT) is scaled down from 1.4 to 1 nm, as well as improvements in SS , g_d and DIBL from reducing the nanowire width. We also find that electron mobility remains constant as the width is scaled to 18 nm.

2:25 PM

3.3 High Frequency GaN HEMTs for RF MMIC Applications (Invited), M. Micovic, D. Brown, D. Regan, J. Wong, F. Herrault, Y. Tang, D. Santos, S. Burnham, J. Tai, E. Prophet, I. Khalaf, C. McGuire, H. Bracamontes, H. Fung, A. Kurdoghlian and A. Schmitz, HRL Laboratories LLC

We provide an overview of key challenges and technical breakthroughs that led to development of highly scaled GaN HEMT's having $f_T > 400 \text{ GHz}$ and $f_{max} > 550 \text{ GHz}$ and the corresponding IC process. These highly scaled GaN devices have 5 times higher breakdown voltage than transistors with similar high frequency RF power gain in other semiconductor systems (Si, SiGe, InP, GaAs). We also report performance of the first generation of MMIC power amplifiers (PAs) that utilize these highly scaled devices. The power added efficiency (PAE) of 59% measured at a frequency of 32 GHz, bias of 3 V and output power of 24.3 dBm of the first generation Ka-band MMIC PAs that were built using these highly scaled GaN devices, represent a significant improvement in PAE over values reported for other semiconductor technologies at this frequency band as well as for Ka-band MMICs built in lower frequency GaN nodes. Presented data suggest that highly scaled GaN transistors are excellent candidates for MMIC PAs for next generation 28 GHz, 39 GHz, and higher frequency 5G mobile bands, because they would greatly extend battery lifetime in mobile handsets, due to their superior PAE compared to competing semiconductor technologies.

2:50 PM

3.4 Electric-Field Induced F⁻ Migration in Self-Aligned InGaAs MOSFETs and Mitigation, X. Cai, J. Lin, D. Antoniadis and J. del Alamo, Massachusetts Institute of Technology

We have identified and studied a new instability mechanism in self-aligned InGaAs MOSFETs due to F- migration and passivation/depassivation of Si dopants in n-InAlAs cap layer. We successfully eliminate this instability by eliminating n-InAlAs from the device structure. The new device design achieves improved stability and record device performance.

3:15 PM

3.5 W-Band N-Polar GaN MISHEMTs with High Power and Record 27.8% Efficiency at 94 GHz, *B. Romanczyk, M. Guidry, S. Wienecke, H. Li, E. Ahmadi, X. Zheng, S. Keller and U. Mishra, University of California, Santa Barbara*

The W-band power performance of N-polar GaN MISHEMTs fabricated using a novel device design to mitigate dispersion is presented. A record power-added efficiency of 27.8% is achieved while maintaining an excellent associated output power density of 3.0 W/mm and peak gain of 7.4 dB at 94 GHz.

3:40 PM

3.6 Monolithic Integration of Multiple III-V Semiconductors on Si for MOSFETs and TFETs (Invited), *H. Schmid, D. Cutaia, J. Gooth, S. Wirths, N. Bologna*, K. Moselund and H. Riel, IBM Research – Zurich, *EMPA, Electron Microscopy Center*

In this paper we report on our work on the monolithic integration of various III-V compounds on Si using template-assisted selective epitaxy (TASE) and its application for electronic devices. Nanowires, crossbar nanostructures, and micron-sized sheets are epitaxially grown on Si via metal-organic chemical vapor deposition and form the basis for III-V MOSFETs and Tunnel FETs. Epitaxy conditions specific to TASE are discussed and material quality assessed. Here, we focus on InAs and GaSb as a potential all-III-V alternative to complementary group IV technology. Scaled n-FETs as well as both n- and p-channel TFETs are fabricated on Si and illustrate the potential of TASE.

4:05 PM

3.7 Study of RF-Circuit Linearity Performance of GaN HEMT Technology using the MVSG Compact Device Model, *U. Radhakrishna, P. Choi, J. Grajal, L.-S. Peh, T. Palacios and D. Antoniadis, Massachusetts Institute of Technology*

This study is a first demonstration of the use of a physical compact model as a tool to identify technology bottlenecks to the linearity performance of emerging devices such as GaN HEMTs and to provide solutions to improve linearity both through device-design and circuit-design techniques. This work investigates the linearity performance of the emergent GaN-HEMT technology targeted for RF-applications, by making use of a physics-based GaN HEMT compact model: MIT Virtual Source GaNFET (MVSG) model to identify the various causes for device-non-linearity and their impact on circuit linearity performance. The model is calibrated and verified against a complete suite of device- measurements in order to identify the impact of device-technology parameters on the non-linear device-behavior as a function of operating class. Well-known non-ideal effects prevalent in GaN technology such as charge-trapping, access-region behavior, and thermal effects are calibrated and the model is used to evaluate the extent of non- linearity (so called 'soft-compression') contributed by each of them. Designed using the model, circuit-level linearity improvement techniques such as 'gm-compensation' demonstrate improvements in linearity (lower harmonic content and IMD) in medium power-levels with fabricated power amplifiers (PAs).

Session 4: Memory Technology - RRAM, PRAM and Applications

Monday, December 5, 1:30 p.m.

Continental Ballroom 4

Co-Chairs: Fabio Pellizer, Micron

John Paul Strachan, Hewlett Packard Labs

1:35 PM

4.1 Towards Ultimate Scaling Limits of Phase-Change Memory (Invited), *F. Xiong, E. Yalon, A. Behnam*, C.M. Neumann, K.L. Grosse*, S. Deshmukh and E. Pop, Stanford University, *University of Illinois Urbana-Champaign*

Data storage based on a reversible material phase transition (e.g. amorphous to crystalline) has been studied for nearly five decades. Yet, it was only during the past five years that some phase-change memory technologies (e.g. GeSbTe) have been approaching the physical scaling limits of the smallest possible memory cell. Here we review recent results from our group and others, which have achieved sub-10 nm scale PCM with switching energy approaching single femtojoules per bit.

Fundamental limits could be as low as single attojoules per cubic nanometer of the memory material, although approaching such limits in practice appears strongly limited by electrical and thermal parasitics, i.e. contacts and interfaces.

2:00 PM

4.2 ALD-based Confined PCM with a Metallic Liner toward Unlimited Endurance, *W. Kim, M. Brightsky, T. Masuda**, *N. Sosa, S. Kim, R. Bruce, F. Carta, G. Fraczak, H.-Y. Cheng***, *A. Ray, Y. Zhu, H.-L. Lung***, *K. Suu* and C. Lam, IBM T.J. Watson Research, *ULVAC, Inc., **Macronix International Company LTD.*

We present for the first time in-depth analysis of the outstanding endurance characteristics of an ALD-based confined phase change memory with a thin metallic liner. This confined PCM with a metallic liner exhibits a new record endurance ($2e12$ cycles) and is found to be immune to classic endurance failure mechanisms.

2:25 PM

4.3 SiO_x-based Resistive Switching Memory (RRAM) for Crossbar Storage/select Elements with High on/off Ratio, *A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro**, *R. Rodriguez** and *D. Ielmini, Politecnico di Milano, *Universitat Autònoma de Barcelona*

Resistive switching memory (RRAM) is among the most promising technologies for storage class memory (SCM) and embedded nonvolatile memory (eNVM). Feasibility of RRAM as SCM and/or embedded memory requires large on/off ratio, good endurance, high retention, and the availability of a robust select element for crossbar array integration. This work presents Ti/SiO_x RRAM with high on/off ratio ($>10^4$), good endurance ($>10^7$), high uniformity and strong retention (260°C for 1 hour), thanks to the high SiO_x band gap. Ag/SiO_x devices show volatile switching with high on/off ratio ($> 10^7$) and bidirectional operation applicable to select devices in crossbar arrays.

2:50 PM

4.4 Forming-Free Metal-Oxide ReRAM by Oxygen Ion Implantation Process, *W. Kim, A. Hardtdegen, C. Rodenbücher, S. Menzel, D. Wouters**, *S. Hoffmann-Eifert, D. Buca, R. Waser and V. Rana, Forschungszentrum Jülich GmbH, *RHTH Aachen University*

We propose a new method for obtaining formingfree ReRAM devices by oxygen ion implantation (O₂ IIP) in the metal oxide film during the device fabrication process. By tuning the implantation dose, as-fabricated devices can be transformed into the ON state. Subsequent standard RESET and SET switching cycles reveal that the forming-free devices switch in a similar way to reference (formed) devices. The devices also show good ROFF/RON >200 , retention ($1E^4$ sec@ 125°C) and endurance reliability ($1E^6$ cycles), showing the absence of any device degradation caused by the O₂ IIP process. This method is applied on both (PVD) Ta₂O₅ and (ALD) HfO₂ nanoscale ReRAM devices, demonstrating the versatile applications of the technique.

3:15 PM

4.5 Understanding RRAM Endurance, Retention and Window Margin Trade-off using Experimental Results and Simulations, *C. Nail, G. Molas, P. Blaise, G. Piccolboni, B. Sklenard, C. Cagli, M. Bernard, A. Roule, M. Azzaz, E. Vianello, C. Carabasse, R. Berthier, D. Cooper, T. Magis, C. Pelissier, G. Ghibaudo**, *C. Vallée****, *B. De Salvo, L. Perniola, D. Bedeau** and O. Mosendz***, *CEA/LETI, *IMEP/LAHC/CNRS, **WD San Jose Research Center, ***LTM/CNRS*

In this paper we clarify for the first time the correlation between endurance, window margin and retention of Resistive RAM. To this aim, various classes of RRAM (OXRAM and CBRAM) are investigated, showing high window margin up to 10^{10} cycles or high 300°C retention. From first principle calculations, we analyze the conducting filament composition for the various RRAM technologies, and extract the key filament features. We then propose an analytical model to calculate the dependence between endurance, window margin and retention, linking material parameters to memory characteristics.

3:40 PM

4.6 Statistical Investigation of the Impact of Program History and Oxide-metal Interface on OxRRAM Retention, *C.-Y. Chen, A. Fantini, R. Degraeve, A. Redolfi, G. Groeseneken, L. Goux and G. Kar, imec and also with ESAT-MICAS, KU Leuven*

Statistically investigation on weak retention bits in OxRRAM devices is performed. For a same cell, retention is affected by pulse duration, pre-Write pulse-pattern, and delay between pulses. Together with material engineering and programming

optimization, data stability improvement via tuning of oxygen chemical potential profile along the conductive filament is demonstrated.

4:05 PM

4.7 Fundamental Variability Limits of Filament-based RRAM, *A. Grossi, E. Nowak, C. Zambelli*, C. Pellissier, S. Bernasconi, G. Cibrario, K. El Hajjam, R. Crochemore, J.-F. Nodin, P. Olivo* and L. Perniola, CEA-LETI, *Università degli Studi di Ferrara*

While Resistive RAM (RRAM) are seen as an alternative to NAND Flash, their variability and cycling understanding remain a major roadblock. Extensive characterizations of multi-kbits RRAM arrays during Forming, Set, Reset and cycling operations are presented allowing the quantification of the intrinsic variability factors. As a result, the fundamental variability limits of filament-based RRAM in the full resistance range are identified.

4:30 PM

4.8 True Random Number Generator using Current Difference based on a Fractional Stochastic Model in 40-nm Embedded ReRAM, *Z. Wei, Y. Kato, S. Ogasahara, Y. Yoshimoto, K. Kawai, Y. Ikeda, K. Eriguchi*, K. Ohmori** and S. Yoneda, Panasonic Semiconductor Solutions Company Limited, *Kyoto University, **University of Tsukuba*

We show a robust 40-nm ReRAM true random number generator without extra chip area. True random is guaranteed by current difference in $1/f$ noise generated by Brownian motion, tested with fractional SDE model. Designed generator circuit passed all NIST SP800-22 tests, achieved 32 Mbps throughput with 0.04 nJ/bit power consumption.

Session 5: Nano Device Technology – 1D and 2D Devices

Monday, December 5, 1:30 p.m.

Continental Ballroom 5

Co-Chairs: Heike Riel, IBM Research

Deji Akinwande, University of Austin, Texas

1:35 PM

5.1 Carbon Nanotube Complementary Logic with Low-Temperature Processed End-Bonded Metal Contacts, *J. Tang, Q. Cao, D. Farmer, G. Tulevski and S.-J. Han, IBM T.J. Watson Research Center*

We demonstrate a new form of end-bonded contacts to CNTs by carbon dissolution into metal contacts with high carbon solubility (e.g., Ni, Co), requiring only low-temperature annealing. We further fabricate complementary logic using end-bonded Ni contacts, where stable NFETs are converted from PFETs using Al₂O₃ as n-type doping layer.

2:00 PM

5.2 First Demonstration of a Wrap-Gated CNT-FET with Vertically-Suspended Channels, *D. Lee, B.-H. Lee, J. Yoon*, B. Choi*, J.-Y. Park, D.-C. Ahn, C.-K. Kim, B.-W. Hwang, S.-B. Jeon, H. J. Ahn, M.-L. Seol**, M.-H. Kang***, B. J. Cho, S.-J. Choi,* and Y.-K. Choi, KAIST (Korea Advanced Institute of Science and Technology), *Kookmin University, **NASA Ames Research Center, ***National Nanofab Center*

Fully wrap-gated carbon nanotube transistors with vertically suspended semiconducting single-walled CNTs, purified up to 99.9%, are demonstrated for the first time. Without a sacrifice of scalability, remarkably enhanced gate controllability and charge transport capabilities were achieved due to the geometrical advantage of the gate-all-around structure with multiple channels. The VS channels were formed with the aid of a silicon-processed vertically integrated nanowire frame, offering high completeness and compatibility with silicon processes.

2:25 PM

5.3 Record Low Metal – (CVD) Graphene Contact Resistance Using Atomic Orbital Overlap Engineering, *A. Meersha, H. Variar, K. Bhardwaj, A. Mishra, S. Raghavan, N. Bhat and M. Shrivastava, Indian Institute of Science, Bangalore*

Different techniques to engineer atomic orbital overlap are proposed to improve metal – graphene contact. Fundamental insight into the orbital overlap engineering has resulted in record low contact resistance at room temperature. This has pushed graphene FET to its intrinsic limits with capability to scale, leading to record high transistor performance.

2:50 PM

5.4 First-principles Simulations of 2-D Semiconductor Devices: Mobility, I-V Characteristics, and Contact Resistance (Invited), *M. Luisier, A. Szabo, C. Stieger, C. Klinkert, S. Brück, A. Jain and L. Novotny, ETH Zurich*

We report in this paper ab-initio quantum transport simulations of different types of single-layer 2-D semiconductors: transition metal and group IV dichalcogenides in the 2H or 1T phase as well as black phosphorus. The electron and hole phonon-limited mobilities of eight selected 2-D crystals are first analyzed before using these materials as n- or p-type channels of ultra-scaled single-gate transistors, computing their I-V characteristics in the presence of electron-phonon scattering, and comparing them to each other. Finally, the properties of metal-MoS₂ contacts are investigated. It is revealed that the current tends to flow at the edge of the metal layer before entering the semiconductor, thus limiting the injection efficiency.

3:15 PM

5.5 Few-Layer Black Phosphorous PMOSFETs with BN/Al₂O₃ Bilayer Gate Dielectric: Achieving I_{on}=850μA/μm, g_m=340μS/μm, and R_c=0.58kΩ·μm, *L. Yang, G. Qiu, M. Si, A. Charnas, C. A. Milligan, D. Zemlyanov, H. Zhou, Y. Du, Y.-M. Lin*, W. Tsai*, Q. Paduano**, M. Snure** and P. Ye, Purdue University, *TSMC, **AFRL, Wright Patterson AFB*

In this paper, high-performance few-layer black phosphorus (BP) PMOSFETs have been demonstrated by using MOCVD BN and ALD Al₂O₃ as the top-gate dielectric as well as the passivation layer. Highest I_{on} of 850μA/μm (V_{ds} = -1.8V) and g_m of 340μS/μm (V_{ds} = -0.8V) have been achieved with the 200nm channel length (L_{ch}) devices. Record low contact resistance (R_c) of 0.58kΩμm has been obtained on BP transistors by contact engineering. The gate leakage of the BN/Al₂O₃ bilayer gate dielectric is less than 10-12A/μm² (V_g = -1V) with an EOT of 3nm. SS and hysteresis voltage as low as 70mV/dec and 0.1V have been achieved, indicating a high quality interface between BP and BN.

3:40 PM

5.6 Approaching Ballistic Transport in Monolayer MoS₂ Transistors with Self-Aligned 10 nm Top Gates, *C. English, K. Smithe, R. Xu and E. Pop, Stanford University*

We present 10 nm self-aligned top-gated transistors based on monolayer MoS₂. We achieve record saturation current (>400 uA/um), excellent sub-threshold slope and EOT. Combining modeling and measurements, we examine diffusive vs. ballistic transport and suggest a route to advance MoS₂ transistors closer to the ballistic limit.

4:05 PM

5.7 High-Yield Large Area MoS₂ Technology: Material, Device and Circuits Co-optimization, *L. Yu, D. El-Damak, U. Radhakrishna, A. Zubair, D. Piedra, X. Ling, Y. Lin, Y. Zhang, Y.-H. Lee*, D. Antoniadis, J. Kong, A. Chandrakasan, T. Palacios, Massachusetts Institute of Technology, *National Tsing-Hua University*

Two-dimensional electronics based on single-layer (SL) MoS₂ offers significant advantages for realizing large-scale flexible systems owing to the ultrathin nature, good transport properties and stable crystalline structure of MoS₂. However, the reported devices and circuits based on this material have low yield because of various variation sources inherent to the growth and fabrication technology. In this work, we develop a variation-aware design flow and yield model to evaluate the MoS₂ technology and provide a guideline for the co-optimization of the material, devices and circuits. Test chips with various inverters and basic logic gates (such as NAND and XOR) are fabricated as demonstration of the close- to-unit yield of the proposed technology platform.

4:30 PM

5.8 Quantitative Evaluation of Energy Distribution of Interface Trap Density at MoS₂ MOS Interfaces by the Terman Method, *M. Takenaka, Y. Ozawa, J. Han and S. Takagi, The University of Tokyo and CREST*

By using Terman method, we reveal MoS₂ MOS interfaces exhibit Dit peak of approximately 1E13 cm⁻²eV⁻¹ related to sulfur vacancies in MoS₂ with nearly constant Dit of 1E12 cm⁻²eV⁻¹. In conjunction with subthreshold swing analyses in MoS₂ MOSFETs, we successfully grasp energy distribution of Dit at native MoS₂ MOS interfaces.

Session 6: Sensors, MEMS, and BioMEMS - Focus Session: Wearables for the Internet-of-Things (IoT)

Monday, December 5, 1:30 p.m.

Continental Ballroom 6

Co-Chairs: Arokiya Nathan, Cambridge University

Montserrat Fernandez-Bolanos, EPFL

1:35 PM

6.1 High Performance, Flexible CMOS Circuits and Sensors Toward Wearable Healthcare Applications (Invited), *K. Takei, Osaka Prefecture University*

Macroscale, flexible, and/or stretchable electronics enable to collect a variety of information by attaching it on diverse objects including nonplanar surfaces such as human body. To realize the devices, there are several technical challenges such as (1) low-cost, macroscale sensor network formation, (2) low power and high performance flexible circuits, and (3) other flexible components including battery and wireless communications. In this study, we propose and develop a low power flexible circuit platform using inorganic material-based complementary metal-oxide-semiconductor (CMOS) on a flexible substrate and printed macro-scale, multi-functional sensor networks to address the challenges.

2:00 PM

6.2 Circuits and Systems for Energy Efficient Smart Wearables (Invited), *A. Sharma, T. Pande, P. Aroul, K. Soundarapandian and W. Lee, Texas Instruments Inc.*

Wearable devices and the associated push to smart health management have become an important facet of the Internet of Things. Wearable technology – with its diverse use cases, signal transduction mechanisms and unique software/ processing requirements – is an ideal lens through which to study the broader Internet of Things. This paper investigates the unique challenges in wearable technology by using optical heart rate monitoring as an example. Strategies encompassing process technology, devices, circuits, systems and algorithms are leveraged to achieve the trifecta of good performance, low power and small form factor.

2:25 PM

6.3 Flexible Metal-oxide Thin Film Transistor Circuits for RFID and Health Patches (Invited), *P. Heremans, N. Papadopoulos, A. de Jamblinne de Meux, M. Nag, S. Steudel, M. Rockele, G. Gelinck*, A. Tripathi**, J. Genoe and K. Myny, imec and University Leuven, *Holst Centre, **IIT Kanpur*

We discuss in this paper the present state and future perspectives of thin-film oxide transistors for flexible electronics. The application case that we focus on is a flexible health patch containing an analog sensor interface as well as digital electronics to transmit the acquired data wirelessly to a base station. We examine the electronic performance of amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) during mechanical bending. We discuss several ways to further boost the electronic transistor performance of n-type amorphous oxide semiconductors, by modifying the semiconductor or by improving the transistor architecture. We show analog and digital circuits constructed with several architectures, all based on n-type-only amorphous oxide technology. From circuit point of view, the discovery of a p-type amorphous semiconductor matching known n-type amorphous semiconductors would be of great importance. The present best-suited p-type is SnO, but it is poly-crystalline in nature and shows some ambipolarity due to the presence of n-type SnO₂. In search of a better p-type semiconductor, preferably amorphous, we present recent insights into the band structure of potential amorphous oxide p-type semiconductors.

2:50 PM

6.4 Challenges and Opportunities in Flexible Electronics (Invited), *R. Bringans and J. Veres, PARC, A Xerox Company*

Flexible electronics has an exciting potential for enabling roll-able, foldable displays, smart patches and smart packaging on paper and plastic substrates. Fabrication options and associated promise and challenges will be discussed, with an emphasis on printing technologies and the integration of large area, flexible electronics with chips.

3:15 PM

6.5 Advanced Integrated Sensor and Layer Transfer Technologies for Wearable Bioelectronics (Invited), *A. Alharbi, B. Nasri, T. Wu and D. Shahrjerdi, New York University*

We discuss two emerging technologies that are central for realizing an optically powered flexible bioelectronic platform. First, we discuss layer transfer through controlled spalling technology for producing high-performance flexible electronics. We present two examples: (1) advanced-node ultra-thin body silicon integrated circuits on plastic, and (2) flexible GaAs photovoltaic energy harvesters. Second, a 4-terminal biosensor is presented that is compatible with ultra-thin body silicon CMOS technology. Through in vitro glucose sensing, we demonstrate that the 4-terminal integrated biosensor enables the

amplification of biochemical signals at the device level. These advanced technologies can give rise to an unprecedented boost in the performance of wearable devices.

3:40 PM

6.6 Wearable Sweat Biosensors (Invited), *W. Gao, H. Nyein, Z. Shahpar, L.-C. Tai, E. Wu, M. Bariya, H. Ota, H. Fahad, K. Chen and A. Javey, University of California, Berkeley*

Wearable perspiration biosensors enable real-time analysis of the sweat composition and can provide insightful information about health conditions. In this review, we discuss the recent developments in wearable sweat sensing platforms and detection techniques. Specifically, on-body monitoring of a wide spectrum of sweat biomarkers are illustrated. Opportunities and challenges in the field are discussed. Although still in an early research stage, wearable sweat biosensors may enable a wide range of personalized diagnostic and physiological monitoring applications.

4:05 PM

6.7 Flexible Metamaterials, Comprising Multiferroic Films (Invited), *Y.P. Lee, Y. J. Woo, Y. J. Kim, H. M. Son and J. S. Hwang, Hanyang University*

The metamaterial (MM) devices on flexible substrates provide a new dimension in manipulating electromagnetic (EM) waves. This work reports MMs realized on flexible and elastomeric substrates, along with the relevant techniques and approaches. Future directions are mentioned with the promise to translate MMs into practical devices. We also present a multiferroic nano-composite film where BiFeO₃ (BFO) nanoparticles (NPs) were evenly dispersed into highly-insulating polyvinyl alcohol (PVA) polymer. The multiferroic (MF) properties of the film were revealed, such as the saturated ferroelectric curves due to the cut-off of current leakage. Moreover, the prepared films show high flexibility and their multiferroicities are preserved well even in a high curved condition, reflecting the possibility for fabricating wearable devices based on MF materials.

Session 7: Modeling and Simulation - Advanced Numerical and Compact Models

Monday, December 5, 1:30 p.m.

Continental Ballroom 7-9

Co-Chairs: Denis Rideau, STMicroelectronics

Xing Zhou, Nanyang Technological University

1:35 PM

7.1 A Novel Synthesis of Rent's Rule and Effective-Media Theory Predicts FEOL and BEOL Reliability of Self-Heated ICs, *W. Ahn, H. Jiang, S.H. Shin and M. Alam, Purdue University*

Precise specification of local temperature, $T(x,y,z)$, in ICs with self-heated surround-gate transistors (SG-FET) is essential to predict transistor and interconnect reliability, especially for Arrhenius-activated degradation modes, such as NBTI, HCI, electromigration, etc. One may calculate $T(x,y,z)$ by 3D Finite element modeling (FEM), but the complex back end of line (BEOL) structure, with 8~10 layers of multiple-connected percolating interconnects, makes this approach impractical for pre-Silicon design/optimization or fast turn-around reliability modeling. In this context, a physics-based, predictive effective media theory (EMT) for BEOL will transform the reliability modeling of self-heated SG-FET technologies. Therefore, in this paper, we (i) develop a physics based electro-thermal compact model for ICs (including the BEOL), based on an innovative synthesis of Rent's rule, EMT for ellipsoidal inclusion, and thermal image charge theory; (ii) validate the model by comparing against 3D FEM results and experimental data from the industry, and (iii) predict BEOL reliability (i.e., electromigration at the specific metal level) and front end of line (FEOL) reliability (i.e., NBTI, HCI) based on the temperature profile. Since the model anticipates changes in $T(x,y,z)$ with interconnect layout and geometry (e.g., wire length and number distribution, metal volumetric fraction, thermal resistance, etc.), our physics-based model suggests exciting opportunities for reliability-aware optimization of self-heated IC.

2:00 PM

7.2 New Approach for Understanding "Random Device Physics" from Channel Percolation Perspectives: Statistical Simulations, Key Factors and Experimental Results, *Z. Zhang, Z. Zhang, R. Wang, X. Jiang, S. Guo, Y. Wang, X. Wang*, B. Cheng*, A. Asenov* and R. Huang, Peking University, *Synopsis*

The concept of percolative channel is essential for understanding statistical variability and reliability in nanoscale transistors. In this paper, the quantitative factors of channel current percolation path (PP) are comprehensively studied in planar and FinFET devices for the first time, with statistical simulations and experimental characterizations. The properly-

defined PP parameters are well quantified by the proposed new approach, and extracted from 'atomistic' device simulation. The experimental data of random telegraph noise (RTN) is used via the atomic PP model to characterize the underlying channel local current fluctuations and thus to benchmark the PP in reality. Experimental results of extracted PP parameters are consistent with those predicted from simulations, confirming the effectiveness of the proposed approach. The 3D PP in FinFET has different features compared with 2D PP in planar devices, and exhibits additional distortion along Fin-width direction. This work provides a unique framework for deep understanding of "random device physics" and thus is helpful for future nano-device design.

2:25 PM

7.3 Oxide-Based Analog Synapse: Physical Modeling, Experimental Characterization, and Optimization, *B. Gao, H. Wu, J. Kang*, H. Yu** and H. Qian, Tsinghua University, *Peking University, **Southern University of Science and Technology*

Analog switching in oxide synaptic device has been recently proposed as an important technology for realizing hardware neural network with online training ability. This paper develops a new physical model to quantify the analog weight modulation behaviors in the oxide-based analog synapse. The analog SET, RESET, and retention loss processes are simulated and verified by the experimental data measured from the fabricated HfOx based synapse. Based on the simulation results, key material parameters are captured, and optimization guidelines are provided.

2:50 PM

7.4 Extending the Bounds of Performance in E-mode p-channel GaN MOSHFETs, *A. Kumar and M. M. De Souza, The University of Sheffield*

An investigation of the distribution of the electric field within a normally-off p-channel heterostructure field-effect transistor in GaN, explains why a high $|V_{th}|$ requires a reduction of the thickness of oxide and the GaN channel layer. The trade-off between on-current $|I_{ON}|$ and $|V_{th}|$, responsible for the poor $|I_{ON}|$ in E-mode devices is overcome with an additional cap AlGaIn layer that modulates the electric field in itself and the oxide. A record $|I_{ON}|$ of 50-60 mA/mm is achieved with a $|V_{th}|$ greater than $|-2|$ V in the designed E-mode p-channel MOSHFET, which is more than double that in a conventional device.

3:15 PM

7.5 NSP: Physical Compact Model for Stacked-planar and Vertical Gate-All-Around MOSFETs, *O. Rozeau, S. Martinie, T. Poiroux, F. Triozon, S. Barraud, J. Lacord, Y.-M. Niquet*, C. Tabone, R. Coquand, E. Augendre, M. Vinet, O. Faynot and J.-Ch. Barbé, CEA-Leti, *CEA-INAC*

In this work, a predictive and physical compact model for NanoWire/NanoSheet (NW/NS) Gate-All-Around (GAA) MOSFET is presented. Based on a novel methodology for the calculation of the surface potential including quantum confinement, this model is able to handle arbitrary NW/NS cross-section shape of stacked-planar and vertical GAA MOSFETs (circular, square, rectangular). This Nanowire Surface Potential (NSP) based model, validated both by numerical simulations and experimental data, is demonstrated to be very accurate in all operation regimes of GAA MOSFETs.

3:40 PM

7.6 A Physics-Based Compact Model for Material- and Operation-Oriented Switching Behaviors of CBRAM, *Y. Zhao, J. Hu, P. Huang, F. Yuan*, Y. Chai*, X. Liu and J. Kang, Peking University, *The Hong Kong Polytechnic University*

A physics-based compact model is developed to capture the essential resistive switching behaviors of CBRAM under DC and AC operations. Three types of evolution modes of conductive filament correlated with material properties and operation schemes are modeled based on the experimental observations. By modeling the temperature and electric-field effects as well as the electrical conduction, the model can well reproduce the DC and AC switching characteristics in different material stacks and operation modes.

4:05 PM

7.7 Multi-Domain Compact Modeling for GeSbTe-based Memory and Selector Devices and Simulation for Large-scale 3-D Cross-Point Memory Arrays, *N. Xu, J. Wang, Y. Deng, Y. Lu, B. Fu, W. Choi, U. Monga*, J. Jeon*, J. Kim*, K.-H. Lee* and E. S. Jung*, Samsung Semiconductor America, *Samsung Electronics*

A novel compact model is developed by coupling comprehensive physical equations from electrical, thermal and phase-transition domains in order to capture their correlations exist in GeSeTe (GST)-based device physics. Several non-ideal effects during GST memory cell operations have been studied with particular focus on cell Read/Write margins and reliability issues. Finally, large-scale 3-D cross-point memory array circuits have been simulated with developed physics-based models to further explore the design constraints.

Session 8: Optoelectronics, Displays, and Imagers - Imaging and Photon Counting Sensors

Monday, December 5, 1:30 p.m.

Imperial Ballroom B

Co-Chairs: Rihito Kuroda, Tohoku University

Assaf Lahav, TowerJazz Semiconductor

1:35 PM

8.1 Backside Illuminated SPAD Image Sensor with 7.83 μ m Pitch in 3D-Stacked CMOS Technology, *T. Al Abbas, N. Dutton*, O. Almer, S. Pellegrini*, Y. Henrion* and R. Henderson, The University of Edinburgh, *STMicroelectronics*

We present the first 3D-stacked backside illuminated (BSI) single photon avalanche diode (SPAD) image sensor capable of both intensity, and time-resolved imaging. The 128x120 prototype has a 7.83 μ m pixel pitch with 45% fill factor. A 40nm bottom tier hosts the processing electronics while a 65nm top tier hosts the photo-detectors.

2:00 PM

8.2 256 \times 256, 100kfps, 61% Fill-factor Time-resolved SPAD Image Sensor for Microscopy Applications, *I. Gyongy, N. Calder, A. Davies*, N. Dutton**, P. Dalgarno*, R. Duncan*, C. Rickman* and R. Henderson, University of Edinburgh, *Heriot-Watt University, **STMicroelectronics*

A 256 \times 256 Single Photon Avalanche Diode image sensor operating at 100kfps with 61% fill factor and 16 μ m pixel pitch is reported. Gating and cooling allow the suppression of dark noise, which, together with the high fill factor, enables competitive low-light performance with electron multiplying CCDs whilst offering time-resolved imaging.

2:25 PM

8.3 An APD-CMOS Image Sensor Toward High Sensitivity and Wide Dynamic Range (Invited), *M. Mori, Y. Sakata, M. Usuda, S. Kasuga, S. Yamahira, Y. Hirose, Y. Kato, A. Odagawa and T. Tanaka, Panasonic Corp.*

2:50 PM

8.4 Novel Stacked CMOS Image Sensor with Advanced Cu2Cu Hybrid Bonding, *Y. Kagawa, N. Fujii*, K. Aoyagi*, Y. Kobayashi, S. Nishi, N. Todaka, S. Takeshita, J. Taura, H. Takahashi*, Y. Nishimura*, K. Tatani*, M. Kawamura, H. Nakayama, T. Nagano*, K. Ohno*, H. Iwamoto*, S. Kadomura and T. Hirayama*, Sony Semiconductor Manufacturing, *Sony Semiconductor Solutions*

We have successfully mass-produced novel stacked back-illuminated CMOS image sensors. In the new CIS, we introduced advanced Cu2Cu hybrid bonding that we had developed. The electrical test results showed that our robust Cu2Cu hybrid bonding achieved remarkable connectivity and reliability. The performance of image sensor was also investigated.

3:15 PM

8.5 An Over 1Mfps Global Shutter CMOS Image Sensor with 480 Frame Storage Using Vertical Analog Memory Integration, *M. Suzuki*, M. Suzuki*, R. Kuroda*, Y. Kumagai, A. Chiba, N. Miura, N. Kuriyama and S. Sugawa*, LAPIS Semiconductor Miyagi Co., Ltd., *Tohoku University*

An over 1Mfps global shutter CMOS image sensor with 480 analog memories/pixel is presented using developed vertical analog memory integration technology. The fabricated prototype chip with 96H \times 128V pixels achieved ultra high speed video capturing at 1Mfps with 480 and 960 frames by full pixel and checkered-pattern half pixel modes, respectively.

3:40 PM

8.6 A 1.8e⁻ Temporal Noise Over 90dB Dynamic Range 4k2k Super 35mm Format Seamless Global Shutter CMOS Image Sensor with Multiple Accumulation Shutter Technology, *K. Kawabata, M. Kobayashi, Y. Onuki, H. Sekine, T. Tsuboi, Y. Matsuno, H. Takahashi, S. Inoue and T. Ichikawa, Canon Inc.*

A low noise and high dynamic range global shutter (GS) CMOS image sensor (CIS) with multiple accumulation shutter technology is described. The pixel having a 6.4 μm pitch, achieved 1.8e- temporal noise and full well capacity of 70,000e- with charge domain memory, corresponding to 92dB dynamic range in 30fps operation. In the signal readout procedure, light exposure and signal readout are executed simultaneously, hence the seamless signal accumulation can be carried out.

4:05 PM

8.7 Four-Directional Pixel-Wise Polarization CMOS Image Sensor Using Air-Gap Wire Grid on 2.5- μm Back-Illuminated Pixels, *T. Yamazaki, Y. Maruyama, Y. Uesaka, M. Nakamura, Y. Matoba, T. Terada*, K. Komori*, Y. Ohba*, S. Arakawa*, Y. Hirasawa**, Y. Kondo**, J. Murayama**, K. Akiyama, Y. Oike, S. Sato and T. Ezaki, Sony Semiconductor Solutions, *Sony Semiconductor Manufacturing, **Sony*

This paper presents a four-directional pixel-wise polarization CMOS image sensor using an air-gap wire grid on 2.5 μm back-illuminated pixels. The 150nm-pitch air-gap wire grid polarizer achieved the smallest polarization pixel with a transmittance of 63.3% and an extinction ratio of 85 at 550nm, realizing various mega-pixel fusion-imaging applications.

Session 9: Process and Manufacturing Technology - 3D Integration and BEOL

Tuesday, December 6, 9:00 a.m.

Grand Ballroom A

Co-Chairs: Lucille Arnaud, CEA Leti

Takahiro Kouno, Socionext

9:05 AM

9.1 Footprint-efficient and Power-saving Monolithic IoT 3D+ IC Constructed by BEOL-compatible sub-10nm High Aspect Ratio (AR>7) Single-grained Si FinFETs with Record High Ion of 0.38 mA/ μm and Steep-swing of 65 mV/dec. and Ion/Ioff Ratio of 8, *C.-C. Yang, J.-M. Shieh, T.-Y. Hsieh, W.-H. Huang, H.-H. Wang, C.-H. Shen, F.-K. Hsueh, P.-Y. Hsieh*, M.-C. Wu* and W.-K. Yeh, National Nano Device Laboratories, *National Tsing Hua University*

A footprint-efficient and power-saving BEOL compatible 3D+IC carrying monolithic 3D stackable FinFETs (3D+ FinFETs) and W interconnect were demonstrated by low thermal budget laser spike anneal technology ($T_{\text{sub}} < 400^\circ\text{C}$) and body-nano-planarizing processes. The narrow single-grained Si fin structure with ultra-low defect surface were fabricated by anisotropic ICP plasma etching and surface modification processes. The thus fabricated sub-10 nm and high aspect ratio ($H_{\text{Fin}}/W_{\text{Fin}} > 7$) 3D+ FinFETs exhibit steep subthreshold swing (S.S. $\sim 65\text{mV}/\text{dec.}$), record high driving current (Ion per W_{Eff} ($W_{\text{Eff}} = 2H_{\text{Fin}} + W_{\text{Fin}}$): 386 $\mu\text{A}/\mu\text{m}$ (n-type) and 352 $\mu\text{A}/\mu\text{m}$ (p-type)), and high Ion/Ioff (> 107), envisioning next generation low-cost heterogeneously integrated IoTs and wearable electronics.

9:30 AM

9.2 An Advanced 3D/2.5D Integration Packaging Approach Using Double-Self-Assembly Method with Complex Topography, and Micropin-Fin Heat Sink Interposer for Pressure Sensing System, *Y.-C. Hu, C.-P. Lin*, H.-C. Chang, Y.-T. Yang, C.-S. Chen* and K.-N. Chen, National Chiao Tung University, *National Applied Research Laboratories*

To cater complex topography sensors and circuit chips for smart lifestyle applications using IoT, we develop a novel efficient double-self-assembly packaging approach by 3D/2.5D heterogeneous integration. This technology is able to integrate various kinds of processed chips, especially with uneven surface and bottom topography. With liquid surface tension, complex topography chips can be handled and self-aligned on precise locations. Double-self-assembly approach demonstrates temporary bonding on carrier wafer and self-aligned permanent bonding in a pressure sensing system packaging. The optimized volume of liquid to use on various complex topography shapes and areas are investigated, while Cu/In low temperature metal bonding and self-assembly approach for high I/O density and low bonding resistance are demonstrated. Excellent electrical characteristics and mechanical strength of show the feasibility of the double-self-assembly approach on complex topography surface chips packaging applications.

9:55 AM

9.3 Interconnect Scaling: Challenges and Opportunities (Invited), *R. Brain, Intel Corp.*

Transistor and interconnect pitch scaling has been used successfully for greater than 40 years to drive significant density and performance benefits in integrated circuits. Transistor performance has continued to improve due to pitch scaling combined with other process enhancements. Interconnects represent a much larger portion of the overall delay and cost of

integrated circuits today than in the past. This paper reviews the relative comparison of interconnect and transistor scaling and key interconnect scaling challenges, and it highlights the transistor/interconnect co-optimization that is needed to create high performance and high yielding interconnects sufficient for today's ultra-large scale integration (ULSI) needs, and reviews future trends.

10:20 AM

9.4 CMOS Compatible MIM Decoupling Capacitor with Reliable Sub-nm EOT High-k Stacks for the 7 nm Node and Beyond, *T. Ando, E. Cartier, P. Jamison*, A. Pyzyna, S. Kim, J. Bruley, K. Chung*, H. Shobha*, I. Estrada-Raygoza*, H. Tang*, S. Kanakasabapathy*, T. Spooner*, L. Clevenger*, G. Bonilla*, H. Jagannathan*, V. Narayanan, IBM T. J. Watson Research Center, *IBM Research @ Albany Nanotech*

We demonstrate a record-low EOT of 0.8 nm for a BEOL MIM decoupling capacitor. We identify that electrical symmetry for opposite bias polarities is a key for multi-plate MIM capacitors. Our novel high-k stack with aggressively scaled EOT and ideal symmetry enables further capacitance enhancements for the 7 nm node and beyond.

10:45 AM

9.5 BEOL Compatible Graphene/Cu with Improved Electromigration Lifetime for Future Interconnects, *L. Li, Z. Zhu*, T. Wang, J. A. Currivan-Incorvia, A. Yoon* and H.-S. P. Wong, Stanford University, *Lam Research Corp.*

We demonstrate a method to grow graphene directly on patterned Cu wires below 400 °C, within the thermal budget of back-end-of line processes (BEOL). The process flow is compatible with direct etched Cu processes for advanced interconnects technology. The graphene/Cu composite exhibits 2× lower resistivity, 1.4× higher breakdown current density and 40× longer electromigration (EM) lifetime than as-deposited Cu. The electromigration performance of graphene/Cu is 10× better than 2 nm CoWP on Cu, and is comparable to the industry-standard 3 nm CoWP capping layer. DFT calculated reveal that the binding between the pristine in-situ grown graphene and Cu makes the Cu atom more resilient to external forces.

11:10 AM

9.6 Vertical Channel Devices Enabled by Through Silicon Vias (TSV) Technologies, *C. Kothandaraman, S. Rosenblatt, J. Safran*, P. Oldiges, P. Kulkarni-Kerber, J. Xumalo*, W. Landers, J. Liu*, J. Oakley*, S. Butt*, T. Graves-Abe*, N. Robson*, M. Farooq*, D. Berger* and S.S. Iyer**, IBM T.J. Watson Research Center, *Global Foundries, **UCLA*

Novel device structures with vertical channels gated by TSV's are demonstrated. The unique device structure is realized in a standard TSV process flow, without new material systems or processes. They can be used for both characterizing the TSV process as well as enable new functions

Session 10: Power Devices - Power Semiconductor Device Technologies

Tuesday, December 6, 9:00 a.m.

Continental Ballroom 1-3

Co-Chairs: Srabanti Chowdhury, University of California Davis

Sei-Hyung Ryu, Wolfspeed

9:05 AM

10.1 1.7 kV / 1.0 mΩcm² Normally-off Vertical GaN Transistor on GaN Substrate with Regrown p-GaN/AlGaIn/GaN Semipolar Gate Structure, *D. Shibata, R. Kajitani, M. Ogawa, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida and T. Ueda, Panasonic Corporation*

We present a normally-off vertical GaN-based transistor on GaN substrate with low specific on-state resistance of 1.0 mohmcm² and high breakdown voltage of 1.7 kV. The vertical GaN transistor with p-GaN/AlGaIn/GaN semipolar gate structure exhibits high threshold voltage of 2.5V and stable switching operation of 400V/15A.

9:30 AM

10.2 Novel GaN Trench MIS Barrier Schottky Rectifiers with Implanted Field Rings, *Y. Zhang, M. Sun, Z. Liu*, D. Piedra, M. Pan**, X. Gao**, Y. Lin, A. Zubair, L. Yu and T. Palacios, Massachusetts Institute of Technology, *Singapore-MIT Alliance for Research Technology, **IQE RF LLC*

We demonstrate a novel GaN vertical Schottky rectifier with trench MIS structures and field rings, for high-voltage and high-frequency applications. The new device greatly enhanced reverse characteristics (10^4 -fold lower leakage and 700 V breakdown voltage) while maintaining a good forward conduction, with high-temperature (250 C) operation and fast switching capability.

9:55 AM

10.3 High-Speed Switching and Current-Collapse-Free Operation by GaN Gate Injection Transistors with Thick GaN Buffer on Bulk GaN Substrates, *H. Handa, S. Ujita, D. Shibata, R. Kajitani, N. Shiozaki, M. Ogawa, H. Umeda, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida and T. Ueda, Panasonic Corporation*

We present a normally-off Gate Injection transistors (GITs) on GaN substrate. Increasing the thickness of GaN buffer layer greatly helps to reduce output charge enabling fast turn-off switching. The RonQoss as a figure-of-merit for high speed switching is reduced down to 940mohmC, which leads to high turn-off dV/dt of 285V/ns.

10:20 AM

10.4 Integration of LPCVD-SiN_x Gate Dielectric with Recessed-gate E-mode GaN MIS-FETs: Toward High Performance, High Stability and Long TDDDB Lifetime, *M. Hua, Z. Zhang, J. Wei, J. Lei, G. Tang, K. Fu*, Y. Cai*, B. Zhang* and K. J. Chen, The Hong Kong University of Science and Technology, *Chinese Academy of Sciences*

By employing an interface protection technique to prevent the etched GaN surface from degradation during high-temperature process, highly reliable LPCVD-SiN_x gate dielectric was successfully integrated with recessed-gate structure to achieve high-performance enhancement-mode GaN MIS-FETs with high V_{th} thermal stability, long time-dependent gate dielectric breakdown lifetime and low bias temperature instability.

10:45 AM

10.5 Superior Performance of SiC Power Devices and Its Limitation by Self-heating (Invited), *T. Terashima, Mitsubishi Electric Corporation*

Recently SiC power devices such as SiC-MOSFET have been improved drastically as a next generation power device because of its superior physical property. Although very high carrier density is essential reason for the superior characteristics of that, there is a fundamental problem to realize the predicted performances. One is limit of rating current density by self-heating. The other is destruction by transient self-heating at short circuit event. This paper evaluates performances of SiC-MOSFET compared to Silicon(Si) power devices under the those thermal limitations, and also clarify the substantial requirements to realize the predicted superior performances.

11:10 AM

10.6 Experimental Verification of a 3D Scaling Principle for Low V_{ce(sat)} IGBT, *K. Kakushima, T. Hoshii, K. Tsutsui, A. Nakajima*, S. Nishizawa*, H. Wakabayashi, I. Muneta, K. Sato**, T. Matsudai***, W. Saito***, T. Saraya^, K. Itou^, M. Fukui^, S. Suzuki^, M. Kobayashi^, T. Takakura^, T. Hiramoto^, A. Ogura^^, Y. Numasawa^^, I. Omura^^^, H. Ohashi and H. Iwai, Tokyo Institute of Technology, *Nat. Inst. Advanced Industrial Science and Technology, **Mitsubishi Electric Corp., ***Toshiba Corp., ^The University of Tokyo, ^^Meiji University, ^^Kyushu Institute of Technology*

Three dimensionally (3D) scaled IGBTs that have a scaling factor of 3 (k=3) with respect to current commercial products (k=1) were fabricated for the first time. The scaling was applied to the lateral and vertical dimensions as well as the gate voltage. A significant decrease in ON resistance, -- V_{ce(sat)} reduction from 1.70 to 1.26 V -- was experimentally confirmed for the 3D scaled IGBTs.

11:35 AM

10.7 Experimental Demonstration of -730V Vertical SiC p-MOSFET with High Short Circuit Withstand Capability for Complementary Inverter Applications, *J. An, M. Namai, M. Tanabe, D. Okamoto, H. Yano and N. Iwamuro, University of Tsukuba*

A new p-channel vertical 4H-SiC MOSFET has been successfully fabricated for the first time. Its breakdown voltage is over -730 V and the short circuit capability is 15% higher than that of 4H-SiC n-channel MOSFET. This could be a superior power device applicable for high frequency complementary inverter.

12:00 PM

10.8 On the Subthreshold Drain Current Sweep Hysteresis of 4H-SiC nMOSFETs, *G. Rescher, G. Pobegen, T. Aichinger* and T. Grasser***, *KAI GmbH, *Infineon AG, **Vienna University of Technology*

We study the subthreshold drain current hysteresis of 4H silicon carbide Si-face (0001) and a-face (1120) n-channel power MOSFETs between gate voltage sweeps from accumulation to inversion and vice versa. Depending on the direction of the gate voltage sweep, the MOSFETs show a different subthreshold drain current at the same gate voltage. The observed hysteresis between up-sweep and down-sweep can be expressed as a subthreshold voltage shift and may reach several volts. We show that the voltage shift is caused by hole capture in border traps during accumulation and is directly proportional to the charge pumping signal. The voltage shift is fully recoverable by applying a gate bias above the threshold voltage and does not impact device reliability.

Session 11: Memory Technology - Charge Based Memories and Scaling

Tuesday, December 6, 9:00 a.m.

Continental Ballroom 4

Co-Chairs: Han Zhao, Intel

Sungyong Chung, SK Hynix

9:05 AM

11.1 First Demonstration of FinFET Split-Gate MONOS for High-Speed and Highly-Reliable Embedded Flash in 16/14nm-node and Beyond, *S. Tsuda, Y. Kawasima, K. Sonoda, A. Yoshitomi, T. Mihara, S. Narumi, M. Inoue, S. Nuranaka, T. Maruyama, T. Yamashita, Y. Yamaguchi and D. Hisamoto**, *Renesas Electronics Corporation, *Hitachi, Ltd*

FinFET split-gate metal-oxide nitride oxide silicon (SG-MONOS) Flash memories have been fabricated and operated for the first time. Excellent subthreshold characteristics and small threshold-voltage variability owing to a Fin-structure are clarified. It is demonstrated that Fin top-corner effects are well suppressed by incremental step pulse programming for source side injection. Highly reliable data retention at 150 °C after 250K program/erase cycles is confirmed for the advanced automotive system applications.

9:30 AM

11.2 A New Ruler on the Storage Market : 3D-NAND Flash for High-density Memory and its Technology Evolutions and Challenges on the Future (Invited), *J. Lee, J. Jang, J. Lim, Y. G. Shin, K. Lee and E. Jung, Samsung Electronics*

Scaling limitations in planar-NAND cell are discussed, including the depletion of floating gate and anomalous programming behavior. It is inevitable to have a paradigm shift to 3D-NAND due to numerous scaling limitations of planar NAND. However, the process complexity also increases in 3D-NAND as the mold height goes up in an exponential trend. Thus, scaling down of mold pitch is required, which degrades the cell characteristics. COP (Cell over Peripheral) 3D- NAND architecture has been developed as an area- scaling technology. CSL (Common-Source Line) junction leakage and p+ junction leakage at peripheral transistors have been improved by increasing the grain size and the thickness of barrier metal, respectively.

9:55 AM

11.3 Polycrystalline-Silicon Channel Trap Induced Transient Read Instability in a 3D NAND Flash Cell String, *W.-J. Tsai, W. L. Lin, C. C. Cheng, S. H. Ku, Y. L. Chou*, L. Liu, S. W. Hwang, T. C. Lu, K. C. Chen, T. Wang* and C.-Y. Lu, Macronix International Company, LTD., *National Chiao-Tung University*

Vt instability caused by grain-boundary trap (GBT) in the poly-crystalline silicon (poly-Si) channel of a 3D NAND string are comprehensively studied. Experimental results reveal that trapping/detrapping of GBT would cause transient cell current with a time constant of 10us or longer, and this transient is strongly affected by the bias history. Sensing offset between program/erase verify (PV/EV) and read (RD) results in "pseudo" charge loss/gain that reduces the sensing margin. Modified EV, PV, or RD bias schemes are suggested to mitigate this effect.

10:20 AM

11.4 Automotive Requirements to Non-Volatile Memories – A Holistic Approach to Qualification (Invited), *V. Kottler, Robert Bosch GmbH, Automotive Electronics*

This work describes a holistic approach to the application of the Robustness Validation methodology to the qualification of non-volatile memories (NVM) for automotive applications, as well as the resulting requirements to the NVM supplier and to the NVM design and technology.

10:45 AM

11.5 A 28nm HKMG Super Low Power Embedded NVM Technology Based on Ferroelectric FETs, *M. Trentzsch, S. Flachowsky, R. Richter, J. Paul, B. Reimer, D. Utess, S. Jansen, H. Mulaosmanovic*, S. Müller*, S. Slesazek*, J. Ocker*, M. Noack*, J. Müller**, P. Polakowski**, J. Schreiter***, S. Beyer, T. Mikolajick* and B. Rice, GLOBALFOUNDRIES Fab1, *NaMLab gGmbH, **Fraunhofer IPMS, ***Racyics GmbH*

A ferroelectric field effect transistor (FeFET) based eNVM was successfully implemented into a 28nm HKMG 28SLP CMOS platform. The electrical baseline properties remain the same for the FeFET integration and the JTAG-controlled 64 kbit memory shows clearly separated states. High temperature retention is demonstrated and endurance up to 100.000 cycles was achieved.

11:10 AM

11.6 How to Make DRAM non-volatile? Anti-ferroelectrics: A New Paradigm for Universal Memories, *M. Pesic, S. Knebel, M. Hoffmann, C. Richter, T. Mikolajick and U. Schroeder, NaMLab gGmbH*

We propose a simple way how non-volatility can be achieved in state-of-the-art ZrO₂ based DRAM stacks. By employing electrodes with different workfunction values, a built-in bias is introduced within the dielectric stack to modify the anti-ferroelectric property of ZrO₂ from standard volatile to non-volatile behavior with high endurance strength.

11:35 AM

11.7 Fully BEOL Compatible TaO_x-based Selector with High Uniformity and Robust Performance, *Q. Luo, X. Xu, H. Lv, T. Gong, S. Long, Q. Liu, H. Sun, L. Li, N. Lu and M. Liu, Institute of Microelectronics, Chinese Academy of Sciences*

We report a novel TaO_x-based selector with trapezoidal band structure, formed by rapid thermal annealing in O₂ plasma. Salient features were successfully achieved, such as high current density (1MA/cm²), high selectivity (5×10⁴), low off-state current (~10 pA), robust endurance (>10¹⁰), self-compliance and excellent uniformity. The device is composed of fully CMOS-compatible materials and has no thermal budget compatibility concerns. Furthermore, the selector was fabricated in 1kb crossbar array and the integrated 1S1R device shows high nonlinearity in low resistance state (LRS), which is quite effective to solve the sneaking current issue. The demonstrated high performance selector device here shows high potential on manufacturing large scale crossbar array.

Session 12: Nano Device Technology - Negative Capacitance and New Material MOSFETs

Tuesday, December 6, 9:00 a.m.

Continental Ballroom 5

Co-Chairs: David Esseni, University of Udine

Takahiro Mori, National Institute of Advanced Industrial Science and Technology

9:05 AM

12.1 Physical Thickness 1.x nm Ferroelectric HfZrO_x Negative Capacitance FETs, *M.-H. Lee, S. T. Fan*, C.-H. Tang, P.-G. Chen, Y.-C. Chou, H.-H. Chen, J.-Y. Kuo, M.-J. Xie, S.-N. Liu, M.-H. Liao*, C.-A. Jong**, K.-S. Li**, M.-C. Chen**, C. W. Liu*, National Taiwan Normal University, *National Taiwan University, **National Nano Device Laboratories*

Ferroelectric HfZrO_x (FE-HZO) negative capacitance (NC) FETs is experimentally demonstrated with physical thickness 1.5 nm, SS = 52 mV/dec, hysteresis free (threshold voltage shift = 0.8 mV), and 0.65 nm CET (capacitance equivalent thickness). The NC-FinFET modeling is validated on standard 14nm FinFET. The transient behavior of gate and drain current response are exhibited with triangular gate voltage sweep. The dynamic NC model with compact equivalent circuit for ultra-thin FE-HZO is established with experimental data validation, and estimates the fast response. A feasible concept of coupling the ultra-thin FE-HZO (1.x nm) with NC as gate stack paves a promising solution for sub-10nm technology node.

9:30 AM

12.2 Ferroelectric HfZrO_x Ge and GeSn PMOSFETs with Sub-60 mV/decade Subthreshold Swing, Negligible Hysteresis, and Improved I_{DS}, *J. Zhou, G. Han, Q. Li, Y. Peng, X. Lu, C. Zhang, J. Zhang, Q.-Q. Sun*, D. W. Zhang* and Y. Hao, Xidian University, *Fudan University*

We report the first ferroelectric (FE) HfZrO_x (HZO) Ge and GeSn pMOSFETs with sub-60 mV/decade subthreshold swing (SS) (40~43 mV/decade), negligible hysteresis, and enhanced IDS. With a RTA at 450 oC, FE devices with reduced hysteresis of 40~60 mV demonstrate the significantly improved SS and IDS characteristics compared to control devices without FE, owing to the negative capacitance (NC) effect induced by HZO. FE Ge and GeSn pFETs achieve 22% and 20% IDS enhancement than control devices, respectively, at the drive voltage of 1.0 V. NC effect in FE devices is proved by the gate leakage and inversion capacitance characteristics.

9:55 AM

12.3 Experimental Study on Polarization-Limited Operation Speed of Negative Capacitance FET with Ferroelectric HfO₂, *M. Kobayashi, N. Ueyama, K. Jang and T. Hiramoto, The University of Tokyo*

We have experimentally investigated the polarization-limited operation speed of Negative Capacitance FET (NCFET) through direct measurement of negative capacitance in transient characteristics and physics-based modeling, for the first time. Systematic analysis enabled accurate parameter extraction. Our newly developed time-dependent NCFET model provided the evidence that NCFET can operate at >MHz.

10:20 AM

12.4 Fully Coupled 3-D Device Simulation of Negative Capacitance FinFETs for Sub 10 nm Integration, *H. Ota, T. Ikegami, J. Hattori, K. Fukuda, S. Migita and A. Toriumi*, National Institute of Advanced Industrial Science and Technology, *The University of Tokyo*

Performances of negative capacitance FinFETs (NC- FinFETs) at sub 10 nm gate length are analyzed with a newly developed technology computer-aided design (TCAD) simulation. This simulation fully couples the Landau-Khalatnikov (L-K) equation with the physical equations for FinFETs in 3-D. It reveals an excellent immunity against short-channel effects in NC-FinFETs owing to NC-enhancement by the gate- to-drain coupling, for the first time. NC-FinFETs with a gate length of 10 nm are projected to operate with more than 26 times energy-efficiency of conventional FinFETs.

10:45 AM

12.5 Impact of La₂O₃/InGaAs MOS Interface on InGaAs MOSFET Performance and its Application to InGaAs Negative Capacitance FET, *C.-Y. Chang, K. Endo, K. Kato, C. Yokoyama, M. Takenaka and S. Takagi, The University of Tokyo and JST-CREST*

The impact of La₂O₃/InGaAs MOS interfaces on the performance of InGaAs MOSFETs and the physical origins are systematically investigated. It is found that La₂O₃/InGaAs MOSFETs exhibit lower S. S. and lower carrier trapping properties, while have lower mobility than Al₂O₃/InGaAs MOSFETs because of higher fixed oxide charge density. Also, it is experimentally found for the first time that ALD La₂O₃ films with thermal budget lower than 300oC have ferroelectricity in W/La₂O₃/InGaAs MOS and W/La₂O₃/W MIM structures. The steep slope characteristics due to the negative capacitance effect have been demonstrated, for the first time, in W/La₂O₃(15nm)/InGaAs MOSFETs.

11:10 AM

12.6 Experimental Study on Hole and Electron Effective Masses in Inversion Layers of Ge (100), (110) and (111) p- and n-MOSFETs, *R. Zhang, J. Li, Z. Zheng, X. Yu, W. Dong and Y. Zhao, Zhejiang University*

The effective masses of hole and electron in the inversion layers have been quantitatively characterized for Ge p- and n-MOSFETs with Shubnikov–de Haas oscillation measurements. It was found that the effective mass clearly increased with a larger N_s for both hole and electron in (100)/(110)/(111) Ge p and n-MOSFETs.

Session 13: Optoelectronics, Displays, and Imagers - Focus Session: Quantum Computing

Tuesday, December 6, 9:00 a.m.

Continental Ballroom 6

Co-Chairs: Ryoichi Ishihara, QuTech, Delft University of Technology

Michael E. Flatte, University of Iowa

9:05 AM

13.1 Quantum Computing Within the Framework of Advanced Semiconductor Manufacturing (Invited), *J.S. Clarke, N. Thomas, J. Roberts, R. Pilliarisetty, Z. Yoscovits, R. Caudillo, H. George, K. J. Singh, D. Michalak, P. Amin, A. Mei, A. Bruno*, S. Poletto*, J. Boter*, G. Droulers*, N. Kalhor*, N. Samkharadze*, J.P. Dehollain*, L. Yeoh*, A. Sammak*, G. Scappucci*, M. Veldhorst*, L. DiCarlo and L. M. K. Vandersypen, Intel Corporation, *TU Delft*

Quantum computing holds the promise of exponential speedup compared to classical computing for select algorithms and applications. Relatively small numbers of logical quantum bits or qubits could outperform the largest of supercomputers. Quantum dots in Si-based heterostructures and superconducting Josephson junctions are just two of the many approaches to construct the qubit. These, in particular, bear similarities to the transistors and interconnects used in advanced semiconductor manufacturing. While initial results on few-qubit systems are promising, advanced process control is expected to improve the qubit uniformity, coherence time, and gate fidelity needed for larger systems. This can be realized through the systematic characterization of film growth, interface control, and patterning.

9:30 AM

13.2 Spin-based Quantum Computing in Silicon CMOS-compatible Platforms (Invited), *A.S. Dzurak, University of South Wales*

This paper reviews the current state of development of spin-based quantum bits (qubits) based on silicon metal-oxide-semiconductor (SiMOS) devices, including both single phosphorus donor qubits in silicon and gate-defined quantum dot qubits that are compatible with CMOS manufacturing.

9:55 AM

13.3 Coupled Quantum Dots on SOI as Highly Integrated Si Qubits (Invited), *S. Oda, G. Yamahata, K. Horibe and T. Koderu, Tokyo Institute of Technology*

Physically-defined coupled quantum dots (QDs) on silicon-on-insulator substrates represent potential multiple scaled qubits. This work demonstrated the fabrication of coupled QDs with control gates and charge sensor single-electron transistors, the observation of Pauli spin blockade and the control of a few electron regimes, as well as triple QDs and p-channel operation.

10:20 AM

13.4 SOI Technology for Quantum Information Processing (Invited), *S. De Franceschi, L. Hutin, R. Maurand, L. Bourdet, H. Bohuslavskiy, A. Corna, D. Kotekar-Patil, S. Barraud, X. Jehl, Y.-M. Niquet, M. Sanquer and M. Vinet, CEA, INAC and CEA, LETI and University of Grenoble Alpes*

We present recent progress towards the implementation of a scalable quantum processor based on fully-depleted silicon-on-insulator (FDSOI) technology. In particular, we discuss an approach where the elementary bits of quantum information – so-called qubits – are encoded in the spin degree of freedom of gate-confined holes in p-type devices. We show how a hole-spin can be efficiently manipulated by means of a microwave excitation applied to the corresponding confining gate. The hole spin state can be read out and reinitialized through a Pauli blockade mechanism. The studied devices are derived from silicon nanowire field-effect transistors. We discuss their prospects for scalability and, more broadly, the potential advantages of FDSOI technology.

10:45 AM

13.5 Cryo-CMOS for Quantum Computing (Invited), *E. Charbon, F. Sebastiano, A. Vladimirescu, H. Homulle, S. Visser, L. Song and R. Incandela, Delft University of Technology*

Cryogenic CMOS, or cryo-CMOS circuits and systems are emerging in VLSI design for many applications, in primis quantum computing. Fault-tolerant quantum bits (qubits) in surface code configurations, one of the most accepted implementations in quantum computing, operate in deep sub-Kelvin regime and require scalable classical circuits. In this paper we advocate the need of designing a new generation of deep-submicron cryo-CMOS circuits to achieve the performance required in a fault-tolerant qubit system. We outline the challenges and limitations of operating in near-Kelvin regimes, and we propose solutions. The paper concludes with several examples showing the suitability of the proposed approach.

11:10 AM

13.6 Diamond – A Quantum Engineer's Best Friend (Invited), *M. Loncar, Harvard University*

11:35 AM

13.7 Large-scale Quantum Technology Based on Luminescent Centers in Crystals (Invited), *M. Trupke, C. Salter, S. Reisenbauer, R. Vasconcelos, G. Wachter, K. Buczak, A. Angerer, J. Schmiedmayer, F. Aumayr, U. Schmid* P. Walther, W. Munro* and K. Nemoto***, *Technische Univ. Wien, *Nippon Telegraph and Telephone, **National Institute of Informatics*

Luminescent defects in crystals are prime candidates for the creation of a quantum technology, given their superlative spin coherence lifetimes. Here we describe the main features of a quantum technology based on crystalline defects which builds upon the impressive recent achievements in diamond research. The basic features of the architecture and the requirements for its implementation are outlined, together with experimental progress and practical considerations towards its realization.

Session 14: Modeling and Simulation - 2D Materials and Organic Electronics

Tuesday, December 6, 9:00 a.m.

Continental Ballroom 7-9

Co-Chairs: John Robertson, Cambridge University

Yang Liu, Zhejiang University

9:05 AM

14.1 Two-Dimensional Transistors Based on MoS₂ Lateral Heterostructures, *D. Marian, E. Dib, T. Cusati, A. Fortunelli*, G. Iannaccone and G. Fiori*, *University of Pisa, *CNR-ICCOM*

We propose two transistor architectures based on lateral heterostructures of metallic and semiconducting phases of monolayer MoS₂, whose patterning has been demonstrated via e-beam irradiation: i) lateral heterostructure FET and ii) "planar barristor", the 2D counterpart of the graphene barristor. We evaluate their performance with ab-initio simulations against the ITRS.

9:30 AM

14.2 Physics of Electronic Transport in Two-dimensional Materials for Future FETs (Invited), *M. Fischetti and W. Vandenberghe*, *The University of Texas at Dallas*

We discuss some basic physical properties of electron transport in two-dimensional materials. First, we discuss how the predicted thermodynamic instability of 2D crystals may influence charge transport via the coupling of electrons with acoustic flexural modes. We then review the properties of suspended and supported graphene and its ribbons and consider the problem of evaluating correctly the electron-phonon coupling in the case of phosphorene. Finally, we discuss the main features of 2D topological insulators and their possible use in transistors.

9:55 AM

14.3 A Numerical Study of Si-TMD Contact with n/p Type Operation and Interface Barrier Reduction for Sub-5nm Monolayer MoS₂ FET, *Y.-T. Tang, K.-S. Li, L.-J. Li*, M.-Y. Li*, C.-H. Lin, Y.-J. Chen, C.-C. Chen, C.-J. Su, B.-W. Wu, C.-S. Wu, M.-C. Chen, J.-M. Shieh, W.-K. Yeh, P.-C. Su**, T. Wang**, F.-L. Yang*** and C. Hu[^]*, *National Nano Device Laboratories, *King Abdullah University of Science and Technology, **National Chiao-Tung University, ***Academia Sinica, ^University of California, Berkeley*

An atomic-scale numerical study of Si contact with transition metal dichalcogenides (TMD) semiconductor materials is proposed by first-principles simulation for the first time. The monolayer MoS₂ channel can be operated as both of n- and p-type FET by properly doping Si S/D to adjust the TMD channel potential. The gradient MoS_x junction of dichalcogenide vacancies enables Si-MoS₂ contact resistance lower than 100Ω-μm for interface Schottky barrier height reduction. The compact Si-MoS₂ interface study can potentially provide monolayer TMD contact design guideline for the sub-5 nm TMD FET fabrication technology.

10:20 AM

14.4 A Modified Schottky Model for Graphene-semiconductor (3D/2D) Contact: A Combined Theoretical and Experimental Study, *S.-J. Liang, W. Hu*, A. Di Bartolomeo**, S. Adam*** and L. K. Ang*, *Singapore University of Technology and Design, *Lawrence Berkeley National Laboratory, **Universita degli Studi di Salerno, ***National University of Singapore and Yale-NUS College*

We present a theoretical and experimental study of graphene/semiconductor (3D/2D) contacts for different semiconductors and dimensionalities, and we propose a revised Schottky model for graphene/semiconductor contact, which is validated by

first-principle calculations and experiments. The proposed model offers new perspective on the nature of graphene/semiconductor contact.

10:45 AM

14.5 Performance Predictions of Single-layer In-V double-gate n- and p-type Feld-effect Transistors, *H. Carrillo-Nuñez, C. Stieger, M. Luisier and A. Schenk, ETH Zurich*

Through ab-initio quantum transport simulations the logic performance of single-layer InAs, InN, InP, and InSb III-V compounds is analyzed in this paper for n- and p-type applications. The key findings are that (i) the low electron effective masses of all these materials lead to very similar and attractive ON-currents in n-type transistors, but cause a rapid deterioration of their sub-threshold swing as the gate length shrinks to 10 nm and below, (ii) the p-type devices show much smaller and scattered current values that are too low to eventually challenge Si FinFETs, and (iii) the density-of-states bottleneck effect strongly influences the behavior of the n-type devices.

11:10 AM

14.6 Current Status and Challenges of the Modeling of Organic Photodiodes and Solar Cells (Invited), *R. R. Clerc, B. Bouthinon*, M. Mohankumar**, P. Rannou**, J. Vaillant***, T. Maindron***, B. Racine***, Y.-F. Chen^, L. Hirsch^, J.-M. Verilhac^, A. Pereira^ and A. Revaux^, University of Lyon, CNRS *ISORG, **CEA, Grenoble, ***CEA LETI, ^University of Bordeaux, ^CEA, LITEN*

Progress in the modeling of charge transport in solution processed solar cells and photodiodes is reviewed. Through several examples involving modeling and original experiments, the role of intentional doping, structural defects and oxygen contamination is discussed.

11:35 AM

14.7 Prospects of Ultra-thin Nanowire Gated 2D-FETs for Next-Generation CMOS Technology, *W. Cao, W. Liu and K. Banerjee, University of California, Santa Barbara*

A core/shell nanowire gated sub-20 nm 2D-FET, targeted at addressing the ultra-thin dielectric growth and channel formation challenges of nanoscale 2D-FETs is demonstrated. Rigorous quantum transport simulations are employed to uncover the full potential of this novel device, as well as to provide guidance to subsequent device design and optimization.

Session 15: Characterization, Reliability and Yield - FINFET and Nanowire Device Reliability

Tuesday, December 6, 9:00 a.m.

Imperial Ballroom A

Co-Chairs: Anthony Oates, TSMC

Cora Salm, University of Twente

9:05 AM

15.1 Reliability Characterization of 10nm FinFET Technology with multi- V_T Gate Stack for Low Power and High Performance, *M. J. Jin, C. Liu, J. Kim, J. Kim, H. Shim, K. Kim, G. Kim, S. Lee, T. Uemura, M. Chang#, T. An, J. Park and S. Pae, Samsung Electronics*

We report the reliability characterization of 10nm FinFET process technology. Unique reliability behavior by using multi- V_T 's through work function engineering is presented. Comparable intrinsic BTI, HCI and TDDB can be achievable vs. 14nm node, while transistors with different V_T -types exhibit no extrinsic issues, can support different V_{max} . Scaled taller and narrower fin shape increases the transistor self-heating which enhances PMOS HCI and on-state TDDB, yet can be mitigated in realistic circuit operations including AC mode which was further validated with modeling [1]. SRAM and product reliability results including SER also exceeds goal.

9:30 AM

15.2 Consideration of BTI Variability and Product Level Reliability to Expedite Advanced FinFET Process Development (Invited), *Y.-H. Lee, J.H. Lee, Y.F. Wang, R. Hsieh, Y.S. Tsai and K. Huang, TSMC*

In this study, the variability of conventional planar (20nm System-on Chip, 20SoC) and FinFET (16nm FinFET, 16FF) time-zero V_t and Bias-Temperature Instability (BTI) induced aging is investigated, as well as its impact on SRAM and Logic product reliability. For 16FF, the V_t after aging is dominated by initial V_t distribution rather than BTI induced V_t shift, and their V_t sigmas are also superior to planar 20SoC. NBTI (Negative Bias Temperature Instability) relaxation

between 20SoC and 16FF are comparable, while 16FF shows less PBTI (Positive Bias Temperature Instability) recovery due to the local high field on fin top. Correlation between SRAM static noise margin (SNM) and NBTI induced V_t shift concurs with the domination of initial V_t sigma for SNM drift. Chip and bit level High-Temperature Operating Life (HTOL) burn-in test with recovery phases demonstrates all the recovery occurs right after stress, so there is no V_t mismatch to make more V_{min} tailing. Bit level AC and DC HTOL V_{min} sigma concurs with the additional V_t mismatch by DC stress. Logic V_{min} recovery at higher temperature demonstrates the signature of BTI contribution in V_{min} . These results indicate that even some of the BTI features of 16FF are different from 20SoC, the adequate process optimization for initial V_t sigma tightening still dominates SRAM/Logic HTOL V_{min} shift rather than BTI aging.

9:55 AM

15.3 Statistical Model of the NBTI-induced Threshold Voltage, Subthreshold Swing, and Transconductance Degradations in Advanced p-FinFETs, *J. Franco, B. Kaczer, S. Mukhopadhyay*, P. Duhan*, P. Weckx, P. Roussel, T. Chiarella, L.-Å. Ragnarsson, L. Trojman**, N. Horiguchi, A. Spessot, D. Linten and A. Mocuta, imec, * IIT Bombay, **Universidad San Francisco de Quito*

We study the stochastic NBTI degradation of p- FinFETs, in terms of ΔV_{th} , ΔSS , and Δgm . We extend our Defect-Centric model to describe also the SS distribution in a population of devices of any area, at any stage of product aging. A large fraction of nanoscale devices is found to show a peak gm improvement after stress. We explain this effect in terms of the interaction of individual defects with the percolative channel conduction, and we propose a statistical description of gm aging. Our V_{th} , SS, and gm aging models are pluggable into reliability-enabled compact models to estimate design margins for a variety of circuits.

10:20 AM

15.4 Hot Carrier Effect in Ultra-Scaled Replacement Metal Gate Si_{1-x}Ge_x Channel p-FinFETs, *M. Wang, X. Miao, J. Stathis*, R. Southwick, B. Linder*, D. Liu, R. Bao and K. Watanabe, IBM @ Albany Nanotech, *IBM TJ Watson Research Center*

Hot carrier reliability is studied in replacement metal gate (RMG) Si_{1-x}Ge_x (x = 20%) channel p-FinFETs with high-k gate dielectrics. In this study, we show that: (1) interface state generation and hole-trapping contribute to the HC damage under high-V_g (~V_d) stress conditions; (2) hot electron injection is the dominant degradation mechanism for low- and mid-V_g biases, which are more representative stress conditions during typical CMOS logic circuit operation. We also found that excessive electron trapping in ultra-scaled SiGe pFinFETs can reduce the effective channel length and significantly increase the off-state leakage current (I_{off}).

10:45 AM

15.5 New Understanding of Dielectric Breakdown in Advanced FinFET Devices – Physical, Electrical, Statistical and Multiphysics Study, *S. Mei, N. Raghavan, M. Bosman*, D. Linten**, G. Groeseneken**, N. Horiguchi** and K. L. Pey, Singapore University of Technology and Design, *A*STAR, **IMEC KU Leuven*

A complete post-mortem study on FinFET dielectric breakdown has been presented combining electro-thermal simulations and reliability test data with in-depth physical analysis insights using TEM/EELS/EDX on multi-fin structures, providing a unified picture. The assumption that the kinetics of failure would remain the same for both planar and FinFET devices is proved to be untrue.

11:10 AM

15.6 Self-heating in FinFET and GAA-NW using Si, Ge and III/V Channels, *E. Bury, B. Kaczer, D. Linten, L. Witters, H. Mertens, N. Waldron, X. Zhou, N. Collaert, N. Horiguchi, A. Spessot and G. Groeseneken, IMEC*

The self-heating (SH) effect is studied experimentally and through simulations on an extensive set of industry relevant solutions for FF and GAA-NW Si and high- μ devices, with multiple processing options. Considerations for managing SH in future technologies are provided.

11:35 AM

15.7 Substrate and Layout Engineering to Suppress Self-heating in Floating Body Transistors, *S.H. Shin, S.H. Kim*, S. K. Kim*, H. Wu, P. D. Ye and M. Alam, Purdue University, *Korea Institute of Science and Technology (KIST)*

Self-heating (SH) has emerged as an important performance, variability, and reliability concern for floating body transistors (FB-FET), namely, extremely-thin-silicon-on-insulator (ETSOI), SOI- FinFET, gate-all-round NW-FET (GAA-FETs), etc.

The floating body topology offers electrostatic control, but restricts heat outflow: apparently an intrinsic trade-off. In this paper, we trace the trajectory of heat flow in a broad range of transistors to show that the trade-off is not fundamental, and self-heating can be suppressed by novel device designs that ease thermal bottlenecks. Towards this goal, we (i) characterize SH in various FB-FETs with different channel materials (Si, Ge, InGaAs) by submicron thermo-reflectance imaging; (ii) identify universal features and common thermal bottlenecks across various transistor technologies, (iii) offer novel, technology-aware device design to ease the bottlenecks and reduce self-heating, and (iv) experimentally demonstrate the effectiveness of these strategies in suppressing self-heating. We conclude that thermal aware transistor design can suppress self-heating without compromising performance and electrostatic control of the transistor.

12:00 PM

15.8 Local Thermometry of Self-heated Nanoscale Devices (Invited), *F. Menges, F. Motzfeld, H. Schmid, P. Mensch, M. Dittberner, S. Karg, H. Riel and B. Gotsmann, IBM Research - Zurich*

Hot spots with dimensions of only a few nanometers form in numerous nanoelectronic devices. Based on recent advances in spatial resolution, these hotspots can now be studied by means of Scanning Thermal Microscopy (SThM). Here, we discuss SThM for nanoscale thermometry in comparison with other established thermometry techniques. In situ measurements of semiconductor channels for logic, and phase change memory devices are used to demonstrate today's measurement capabilities. Temperature fields characterize not only energy dissipation in in-tact devices but can also serve to identify device failure and fabrication issues.

Session 16: Circuit and Device Interaction - Resistive Device Designs for von-Neumann Computing and Beyond

Tuesday, December 6, 9:00 a.m.

Imperial Ballroom B

Co-Chairs: Elisa Vianello, CEA-LETI

Meng-Fan Chang, National Tsing Hua University

9:05 AM

16.1 Hyperdimensional Computing with 3D VRRAM In-Memory Kernels: Device-Architecture Co-Design for Energy-Efficient, Error-Resilient Language Recognition, *H. Li, T. Wu, A. Rahimi*, K.-S. Li**, M. Rusch*, C.-H. Lin**, J.-L. Hsu**, M. Sabry, S. Burc Eryilmaz, J. Sohn, W.-C. Chiu**, M.-C. Chen**, T.-T. Wu**, J.-M. Shieh**, W.-K. Yeh**, J. Rabaey*, S. Mitra and H.-S. P. Wong, Stanford University, *University of California, Berkeley, **National Nano Device Laboratories*

The ability to learn from few examples, known as one-shot learning, is a hallmark of human cognition. Hyperdimensional (HD) computing is a brain-inspired computational framework capable of one-shot learning, using random binary vectors with high dimensionality. Device-architecture co-design of HD cognitive computing systems using 3D VRRAM/CMOS is presented for language recognition. Multiplication-addition-permutation (MAP), the central operations of HD computing, are experimentally demonstrated on 4-layer 3D VRRAM/FinFET as non-volatile in-memory MAP kernels. Extensive cycle-to-cycle (up to 1E12 cycles) and wafer-level device-to-device (256 RRAMs) experiments are performed to validate reproducibility and robustness. For 28-nm node, the 3D in-memory architecture reduces total energy consumption by 52.2% with 412 times less area compared with LP digital design (using registers as memory), owing to the energy-efficient VRRAM MAP kernels and dense connectivity. Meanwhile, the system trained with 21 samples texts achieves 90.4% accuracy recognizing 21 European languages on 21,000 test sentences. Hard-error analysis shows the HD architecture is amazingly resilient to RRAM endurance failures, making the use of various types of RRAMs/CBRAMs (1k ~ 10M endurance) feasible.

9:30 AM

16.2 Binary Neural Network with 16 Mb RRAM Macro Chip for Classification and Online Training, *S. Yu, Z. Li, P.-Y. Chen, H. Wu*, B. Gao*, D. Wang*, W. Wu* and H. Qian*, Arizona State University, *Tsinghua University*

On-chip implementation of large-scale neural networks with emerging synaptic devices is attractive but challenging, primarily due to the pre-mature analog properties of today's resistive memory technologies. This work aims to realize a large-scale neural network using today's available binary RRAM devices for image recognition. We propose a methodology to binarize the neural network parameters with a goal of reducing the precision of weights and neurons to 1-bit for classification and <8-bit for online training. We experimentally demonstrate the binary neural network (BNN) on Tsinghua's 16 Mb RRAM macro chip fabricated in 130 nm CMOS process. Even under finite bit yield and endurance cycles, the system performance on MNIST handwritten digit dataset achieves ~96.5% accuracy for both classification and online training,

close to ~97% accuracy by the ideal software implementation. This work reports the largest scale of the synaptic arrays and achieved the highest accuracy so far.

9:55 AM

16.3 A ReRAM-based Single-NVM Nonvolatile Flip-Flop with Reduced Stress-Time and Write-Power against Wide Distribution in Write-Time by Using Self-Write-Termination Scheme for Nonvolatile Processors in IoT Era, *C.-P. Lo, W.-H. Chen, Z. Wang***, *A. Lee**, *K.-H. Hsu, F. Su***, *Y.-C. King, C. J. Lin, Y. Liu***, *H. Yang***, *P. Khalili**, *K.-L. Wang** and *M.-F. Chang*, *National Tsing Hua University*, **University of California, Los Angeles*, ***Tsinghua University*

Recent nonvolatile flip-flops (nvFFs) enable the parallel movement of data locally between flip-flops (FFs) and nonvolatile memory (NVM) devices for faster system power off/on operations. The wide distribution and long period in NVM-write times of previous two-NVM-based nvFFs result in excessive store energy (ES) and over-write induced reliability degradation for NVM-write operations. This work proposes an nvFF using a single NVM (1R) with self-write-termination (SWT), capable of reducing ES by 27+x and avoid over-write operations. In fabricated 65nm ReRAM nvProcessor testchips, the proposed SWT1R nvFFs achieved off/on operations with a 99% reduction in ES and 2.7ns SWT latency (TSWT). For the first time, an nvFF with single NVM device is presented.

10:20 AM

16.4 50x20 Crossbar Switch Block (CSB) with Two-Varistors (a-Si/SiN/a-Si) Selected Complementary Atom Switch for a highly-dense Reconfigurable Logic, *N. Banno, M. Tada, K. Okamoto, N. Iguchi, T. Sakamoto, H. Hada, H. Ochi**, *H. Onodera***, *M. Hashimoto**** and *T. Sugibayashi*, *NEC Corp.*, **Ritsumeikan University*, ***Kyoto University*, ****Osaka University*

A 50x20 crossbar switch block (CSB) with two-varistors selected complementary atom switch (2V-1CAS) is newly developed for nonvolatile-FPGA. The 2V-1CAS can realize the multiple fan-outs without select transistors. The improved a-Si/SiN/a-Si varistor with a novel triple layered SiN shows superior nonlinearity of 1.1×10^5 with $J_{max} = 1.63 \text{ MA/cm}^2$. The developed CSB is also applicable for memory of LUTs.

10:45 AM

16.5 Zero Static-Power 4T SRAM with Self-Inhibit Resistive Switching Load by Pure CMOS Logic Process, *C. F. Liao, M.-Y. Hsu, Y.-D. Chih**, *J. Chang**, *Y. C. King* and *C. J. Lin*, *National Tsing Hua University*, **Taiwan Semiconductor Manufacturing Company*

A full logic compatible 4T2R nonvolatile Static Random Access Memory (nv-SRAM) is successfully demonstrated in pure 40nm CMOS logic process. This non-volatile SRAM consists of two STI RRAMs embedded inside the 4T SRAM with minimal area penalty and full logic compatibility. Data is accessed through SRAM cells, and stored by switching one of the loading RRAMs by a unique self-inhibit feature. With this embedded STI RRAM storage nodes, data can be held under power-off mode with zero static power.

11:10 AM

16.6 Experimental Demonstration of Short and Long Term Synaptic Plasticity Using OxRAM Multi k-bit Arrays for Reliable Detection in Highly Noisy Input Data, *T. Werner, E. Vianello, O. Bichler**, *A. Grossi, E. Nowak, J.-F. Nodin, B. Yvert***, *B. De Salvo, L. Perniola, CEA LETI*, **CEA LIST*, ***INSERM*

In this paper, we propose a new circuit architecture and a reading/programming strategy to emulate both Short and Long Term Plasticity (STP, LTP) rules using non-volatile OxRAM cells. For the first time, we show how the intrinsic OxRAM device switching probability at ultra-low power can be exploited to implement STP as well as LTP learning rules. Moreover, we demonstrate the computational power that STP can provide for reliable signal detection in highly noisy input data. A Fully Connected Neural Network incorporating STP and LTP learning rules is used to demonstrate two applications: (i) visual pattern extraction and (ii) decoding of neural signals. A high accuracy is obtained even in presence of significant background noise in the input data.

11:35 AM

16.7 Device Nonideality Effects on Image Reconstruction using Memristor Arrays, *W. Ma, F. Cai, C. Du, Y. Jeong, M. Zidan* and *W. Lu*, *University of Michigan*

We analyze the effects of device variability during experimental image reconstruction using memristor crossbar arrays. The effects of device variability during online and offline training were carefully studied, along with device failures including

SA0 and SA1. SA1 failure was found to significantly affect image reconstruction results, and a practical approach was developed to mitigate the effects of SA1 failure in memristor crossbars.

12:00 PM

16.8 Demonstration of Hybrid CMOS/RRAM Neural Networks with Spike time/rate-dependent Plasticity, *V. Milo, G. Pedretti, R. Carboni, A. Calderoni*, N. Ramaswamy*, S. Ambrogio and D. Ielmini, Politecnico di Milano and I.U.NET, *Micron Technology*

Neural networks with resistive-switching memory (RRAM) synapses can mimic learning and recognition in the human brain, thus overcoming the major limitations of von Neumann computing architectures. While most researchers aim at supervised learning of a pre-determined set of patterns, unsupervised learning of patterns might be attractive for brain-inspired robot/drone navigation. Here we demonstrate neural networks with CMOS/RRAM synapses capable of unsupervised learning by spike-time dependent plasticity (STDP) and spike-rate dependent plasticity (SRDP). First, STDP learning in a RRAM synaptic network is demonstrated. Then we present a 4-transistor/1-resistor synapse capable of SRDP, finally demonstrating SRDP learning, update, and recognition of patterns at the level of neural network.

Luncheon

Tuesday, December 6, 12:20 p.m.
Grand Ballroom B

Luncheon Presentation: Roberto Cingolani, Istituto di Tecnologia

“Translating Evolution Into Technology: From Biochemical Robots to Autonomous Anthropomorphic Machines”

Nature has developed a number of smart solutions to make very efficient living machines over billions of years: from antibodies, to plants to humans. Reproducing the characteristics of these systems in a machine is the way of choice to create robots which integrate perfectly inside our body and/or around ourselves, up to the ultimate challenge of reproducing the unique mind-body nexus of humans.

In this frame, the discussion will preliminary address a general comparison between living and artificial systems today. Artificial antibodies, plantoid robots, animaloids and humanoids will be presented, addressing the main technological topics, namely: New materials and biodegradability, Sensing, Power Sources, Manufacturing, Mind and Computation and Human-robot interaction.

Biography

Born on December 23, 1961 - Milano, Italy

IIT Scientific Director since December 8th, 2005

Scientific activity

- 1985 - Degree in Physics
- 1988 - PhD in Physics
- 1989 - Diploma di Perfezionamento in Physics, Scuola Normale Superiore di Pisa (Italy)
- 1989 - 1991 staff member at Max Planck Institut for Festkoerperforschung in Stuttgart (Germany)
- 1992 onwards - Professor of Experimental Physics, Lecce University (Italy)
- During 1997 Visiting Professor at the Institute of Industrial Sciences, Tokyo University, Tokyo (Japan)
- During 1998 Visiting Professor at Virginia Commonwealth University, Richmond, Virginia (USA)
- 2001 – 2005 Founder and Director of the National Nanotechnology Laboratory (NNL) of INFN, Lecce (Italy). Staff 200 people.
- Since December 2005 Scientific Director of Istituto Italiano di Tecnologia (IIT), Genova (Italy). Today IIT has a staff of 1500 people from 56 countries.

R. Cingolani is author or co-author of about 750 papers in international journals (H-index = 78, citations 25000 Source Google Scholar, October 2016), and he holds about 46 patent families in the fields of:

- Structural, optical and electronic properties of quantum nanostructures of semiconductors

- Optical spectroscopy of solids and modelling of the electronic states (1985-1995)
- Nanofabrication of quantum nanostructures by optical, X-ray and electron-beam lithography (1990-2000)
- Molecular nanotechnologies for plastic photonics, OLED e plastic electronic devices (since 2000).
- Bio-nanotechnologies, biomimetic systems, biological electronic devices (since 2003)
- Nanochemistry, study and interdisciplinary application of nanoparticles of controlled size, shape and composition for new fluorophores, intelligent drug delivery, nanocomposite materials
- Smart nanocomposite materials.
- Robotics, Bioinspired robotics

Awards and Honors

- 1978 National finalist of the X European Philips Contest for Young Researchers and Inventors
- 1980 and 1981 European finalist of the XII and XIII European Philips Contest for Young Researchers and Inventors (Amsterdam and Bruxelles, respectively)
- 1986 and 1990 Prize of the Italian Physical Society for young researchers
- 2000 Awarded the "ST-Microelectronics" award by the Italian Physical Society
- 2006 Awarded the title of "Commendatore della Repubblica" by the President of the Italian Republic
- 2006 Awarded the "Guido Dorso" prize by the Senate of the Italian Republic for his Research Activity
- 2010 Awarded the "Grande Ippocrate" prize by Novartis

Session 17: Process and Manufacturing Technology - Silicon Based Advanced CMOS

Tuesday, December 6, 2:15 p.m.

Grand Ballroom A

Co-Chairs: Pierre Morin, STMicroelectronics

Jong-Ho Lee, Seoul National University

2:20 PM

17.1 Air Spacer for 10nm FinFET CMOS and Beyond, *K. Cheng, C. Park*, C. W. Yeung, S. Nguyen, J. Zhang, X. Miao, M. Wang, S. Mehta, J. Li, C. Surisetty, R. Muthinti, Z. Liu, H. Tang, S. Tsai*, T. Yamashita, H. Bu and R. Divakaruni, IBM, *GLOBALFOUNDRIES*

For the first time, we report integration of air spacers with FinFET technology at 10nm node dimensions. The benefit of parasitic capacitance reduction by air spacers has been successfully demonstrated both at transistor level (15-25% reduction in overlap capacitance (Cov)) and at ring oscillator level (10-15% reduction in effective capacitance (Ceff)). Key process challenges and device implications of integrating air spacers in FinFET are identified. We propose a partial air spacer scheme, in which air spacers are formed only above fin top and sandwiched by two dielectric liners, as a viable option to adopt air spacers in FinFET technology with minimal risks to yield and reliability.

2:45 PM

17.2 FinFET Performance with Si:P and Ge:Group-III-Metal Metastable Contact Trench Alloys, *O. Gluschenkov, Z. Liu, H. Niimi*, S. Mochizuki, J. Fronheiser*, X. Miao, J. Li, J. Demarest, C. Zhang, C. Niu*, B. Liu*, A. Petrescu, P. Adusumilli, J. Yang, H. Jagannathan, H. Bu and T. Yamashita, IBM Research at Albany Nanotech, *GLOBALFOUNDRIES Inc.*

We achieved record n-type and p-type S/D contact resistivity of mid-10-10 Ohm-cm² and 1.9x10⁻⁹ Ohm-cm², respectively, by employing laser-induced liquid or solid phase epitaxy and forming semi-metallic, semiconductor-dopant metastable alloys within nano-scale contact trenches. Correspondingly, large Ron reduction and Id gain have been realized in scaled FinFETs.

3:10 PM

17.3 FOI FinFET with Ultra-low Parasitic Resistance Enabled by Fully Metallic Source and Drain Formation on Isolated Bulk-Fin, *Q. Zhang, H. Yin, J. Luo, H. Yang, L. Meng, Y. Li, Z. Wu, Y. Zhang, Y. Zhang, C. Qin, J. Li, J. Gao, G. Wang, W. Xiong, J. Xiang, Z. Zhou, S. Mao, G. Xu, J. Liu, Y. Qu, T. Yang, J. Li, Q. Xu, J. Yan, H. Zhu, C. Zhao and T. Ye, Institute of Microelectronics Chinese Academy of Sciences*

The large parasitic resistance has become a critical limiting factor to on current of FinFET and nanowire devices. Fully metallic source and drain (MSD) process is one of the most promising solutions but it often suffers from intolerant junction

leakage in bulk FETs. In this paper, fully MSD process on Fin- on-insulator (FOI) FinFET is investigated extensively for the first time. By forming fully Ni(Pt) silicide on FOI FinFET, about 90% reduction in contacted resistivities (Rcs) and 55% reduction in sheet resistances (Rss) are achieved without obvious junction leakage degradation. As a consequence, the on current (ION) of transistor, with gate length (Lg) of 20nm, is increased 30 times, up to 547 μ A/ μ m for NMOS and 324 μ A/ μ m for PMOS, respectively. Excellent controls of SCE and channel leakage with 47% DIBL, 32% SS and 2.5% device leakages reductions over the counterpart of conventional bulk FinFETs are also obtained. Meanwhile, the fully MSD process also induces clear tensile stress into narrow fin- channel, resulting in enhanced electron mobility in NMOS. A further improvement in PMOS drive ability (486 μ A/ μ m) by using Schottky barrier source and drain (SBSD) technology is also explored.

3:35 PM

17.4 Technology Viable DC Performance Elements for Si/SiGe channel CMOS FinFET, G. Tsutsui, R. Bao, K.-Y. Lim*, R. Robison, R. Vega, J. Yang, Z. Liu, M. Wang, O. Gluschenkov, C. W. Yeung, K. Watanabe, S. Bentley*, H. Niimi*, D. Liu, H. Zhou, S. Siddiqui*, H. Kim*, R. Galatage*, R. Venigalla, M. Raymond*, P. Adusumilli, S. Mochizuki, T. Devarajan, B. Miao, B. Liu*, A. Greene, J. Shearer, P. Montanini, J. Strane, C. Prindle*, E. Miller, J. Fronheiser*, C. Niu*, K. Chung, J. Kelly, H. Jagannathan, S. Kanakasabapathy, G. Karve, F. L. Lie, P. Oldiges, V. Narayanan, T. Hook, A. Knorr*, D. Gupta, D. Guo, R. Divakaruni, H. Bu and M. Khare, IBM Research, *GLOBALFOUNDRIES Inc.

Low Ge content SiGe-based CMOS FinFET is one of the promising technologies offering solutions for both high performance and low power applications. In this paper, we established a competitive SiGe-based CMOS FinFET baseline and examined various elements for high performance offering. The performance elements in gate stack, channel doping, contact resistance, and junction have been explored to provide a cumulative 20% / 25% (n/pFET) performance enhancement. These elements provide a viable path towards performance enhancement for future technology nodes.

4:00 PM

17.5 Improvement of the CMOS Characteristics of Bulk Si FinFETs by High Temperature Ion Implantation, Y. Kikuchi, T. Hopf, G. Mannaert, Z. Tao, A. Waite*, J. Cournoyer*, J. Borniquel*, R. Schreutelkamp*, R. Ritzenthaler, M.-S. Kim, S. Kubicek, S. A. Chew, K. Devriendt, T. Schram, S. Demuyne, N. Variam*, N. Horiguchi and D. Mocuta, imec, *Applied Materials

For the first time, we established a replacement metal gate CMOS process flow of bulk Si FinFETs for high temperature ion implantation process using dedicated patterning processes on 45-nm fin pitch. A detailed process flow is explained, and better electrical characteristics of MOSFETs and ring oscillators are obtained.

4:25 PM

17.6 Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain, S. Barraud, V. Lapras, M.-P. Samson*, L. Gaben, L. Grenouillet, V. Maffini-Alvaro, Y. Morand*, J. Daranlot, N. Rambal, B. Previtali, S. Reboh, C. Tabone, R. Coquand, E. Augendre, O. Rozeau, J.-M. Hartmann, C. Vizioz, C. Arvet*, P. Pimenta-Barros, N. Posseme, V. Loup, C. Comboutoure*, C. Euvrard, V. Balan, I. Tinti, G. Audoit, N. Bernier, D. Cooper, Z. Saghi, F. Allain, A. Toffoli, O. Faynot and M. Vinet, CEA, LETI, Minatec and University of Grenoble Alpes, *STMicroelectronics

We report on vertically stacked horizontal Si NanoWires (NW) p-MOSFETs fabricated with a replacement metal gate (RMG) process. For the first time, stacked-NWs transistors are integrated with inner spacers and SiGe source-drain (S/D) stressors. Recessed and epitaxially re-grown SiGe(B) S/D junctions are shown to be efficient to inject strain into Si p-channels. The Precession Electron Diffraction (PED) technique, with a nm- scale precision, is used to quantify the deformation and provide useful information about strain fields at different stages of the fabrication process. Finally, a significant compressive strain and excellent short-channel characteristics are demonstrated in stacked-NWs p- FETs

4:50 PM

17.7 A Novel Dual Isolation Scheme for Stress and Back bias Maximum Efficiency in FDSOI Technology, R. Berthelon, F. Andrieu, P. Perreau, D. Cooper, F. Roze, O. Gourhant*, P. Rivallin, N. Bernier, A. Cros*, C. Ndiaye*, E. Baylac*, E. Souchier*, D. Dutartre*, A. Claverie**, O. Weber, E. Josse*, M. Vinet and M. Haond*, CEA-Leti, *STMicroelectronics, **CEMES-CNRS

A novel dual isolation scheme with both Shallow Trench Isolation (STI) and local oxidation, so called Dual Isolation by Trenches and Oxidation (DITO), is presented to maximize the stress induced by SiGe channel and the back biasing

efficiency at the same time in FDSOI technology. DITO integration experimentally demonstrates +36% pMOSFET drive current at same leakage, which is translated into -23% ring-oscillator delay reduction at a supply voltage of $V_{DD}=0.8V$.

Session 18: Sensors, MEMS, and BioMEMS - Enhanced Sensing, Heterogeneous Integration and Wearables

Tuesday, December 6, 2:15 p.m.

Continental Ballroom 1-3

Co-Chairs: Debbie Senesky, Stanford University

Bernard Legrand, LAAS-CNRS

2:20 PM

18.1 Highly Improved Response and Recovery Characteristics of Si FET-type Gas Sensor Using Pre-bias, *J. Shin, Y. Hong, M. Wu, Y. Jang, J. S. Kim, B.-G. Park, C. S. Hwang and J.-H. Lee, Seoul National University*

By adopting a new pulse pre-bias (V_{pre}) scheme, the response and recovery characteristics is significantly improved in Si field-effect transistor (FET)-type gas sensor having ZnO film as a sensing layer. A target gas of NO₂, which is one of oxidizing gases, is detected by the FET-type sensor at various V_{pres} . It is demonstrated that a negative V_{pre} (-3 V) improves the response by ~2.5 times and a positive V_{pre} (4 V) reduces the recovery time by ~9 times in 0.5 ppm NO₂ ambience at 180 oC. The mechanism responsible for the pre-bias effect is explained using energy band diagram.

2:45 PM

18.2 Graphene-gate Transistors for Gas Sensing and Threshold Control, *N. Harada, K. Hayashi, M. Kataoka, J. Yamaguchi, M. Ohtomo, M. Ohfuchi, I. Soga, D. Kondo, T. Iwai and S. Sato, Fujitsu Laboratories Ltd.*

Graphene was employed as gate electrodes of silicon transistors. When gas molecules adsorb on an exposed graphene gate, its work function changes, shifting the transistor threshold. This graphene-gate sensor exhibited excellent sensitivities, detecting 7-ppb NO₂. Furthermore, the intentional doping of the graphene gate successfully shifted the threshold by 620 mV.

3:10 PM

18.3 Tunable and Wearable High Performance Strain Sensors Based on Laser Patterned Graphene Flakes, *L.-Q. Tao, D.-Y. Wang, H. Tian*, Z.-Y. Ju, Y. Liu, Y.-Q. Chen, Q.-Y. Xie, H.-M. Zhao, Y. Yang and T.-L. Ren, Tsinghua University, *University of Southern California*

Tunable and wearable strain sensors based on laser patterned graphene flakes (LPGF) are demonstrated in this paper. The performance can be adjusted by laser patterning, resulting in a preferable gauge factor (up to 457) or strain range (over 100%), both of which are significantly higher than most state-of-the-art graphene strain sensors. These tunable strain sensors will have great potentials in health care, voice recognition, gesture control and many other areas.

3:35 PM

18.4 Thinnest Transparent Epidermal Sensor System Based on Graphene, *S. K. Ameri, R. Ho, H. Jang, Y. Wang, D. Schnyer, D. Akinwande and N. Lu, University of Texas at Austin*

We report the fabrication of world's thinnest transparent graphene-based epidermal sensor system (GESS) with total thickness below 500 nm. It can fully conform to human skin without using any adhesives, which leads to low impedance interface for the measurement of electrophysiological signals (ECG, EEG, EMG), skin hydration, and skin temperature.

4:00 PM

18.5 Heterogeneously-Integrated Microdevices (Invited), *S. Tanaka, Tohoku University*

The integration of heterogeneous components or materials is a promising approach to create more functionalized, higher performance and smaller devices. However, there are technical problems in terms of process temperature limit, thermal expansion mismatch, process incompatibility, die size mismatch etc. To overcome such problems, significant efforts have been made in the world. This paper introduces two approaches, wafer bonding and film transfer, which have been developed in our group.

4:25 PM

18.6 A CMOS-compatible Large-Scale Monolithic Integration of Heterogeneous Multi-Sensors on Flexible Silicon for IoT Applications, *J. Nassar, G. Torres Sevilla, S. Velling**, *M. D. Cordero, M. Hussain, King Abdullah University of Science Technology (KAUST)*, **University of Waterloo*

We report CMOS technology enabled fabrication and system level integration of flexible bulk silicon (100) based multi-sensors platform which can simultaneously sense pressure, temperature, strain and humidity under various physical deformations. We also show an advanced wearable version for body vital monitoring which can enable advanced healthcare for IoT applications.

4:50 PM

18.7 Sensors and Haptics Technologies for User Interface Design in Wearables (Invited), *R. Baskaran and G.C. Dogiamis, Intel Corporation*

In this paper, a summary of various sensory technologies and interactions within them in wearable platforms is presented. In the first part of the paper, we discuss the way humans perceive various sensory inputs. Then, we review today's state of art sensor technologies for user interfaces, followed by discussions on opportunities uniquely enabled by the wearable form factor.

Session 19: Nano Device Technology - Tunnel and Nanowire FETs

Tuesday, December 6, 2:15 p.m.

Continental Ballroom 5

Co-Chairs: Rossella Ranica, STMicroelectronics

Andreas Schenk, ETH Zurich

2:20 PM

19.1 Vertical InAs/GaAsSb/GaSb Tunneling Field-Effect Transistor on Si with $S = 48$ mV/decade and $I_{on} = 10$ $\mu\text{A}/\mu\text{m}$ for $I_{off} = 1$ nA/ μm at $V_{DS} = 0.3$ V, *E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind and L.-E. Wernersson, Lund University*

A vertical nanowire InAs/GaAsSb/GaSb TFET, with a S_{min} of 48 mV/dec. for $V_{DS} = 0.1 - 0.5$ V and $I_{on} = 10.6$ $\mu\text{A}/\mu\text{m}$ for $I_{off} = 1$ nA/ μm at $V_{DS} = 0.3$ V is presented. The TFET demonstrates $S < 60$ mV/decade for $I_{DS} = 1$ nA/ μm up to a record high $I_{60} = 0.31$ $\mu\text{A}/\mu\text{m}$.

2:45 PM

19.2 Two-dimensional Heterojunction Interlayer Tunnel FET (Thin-TFET): From Theory to Applications (Invited), *M. Li, R. Yan, D. Jena, and H. Xing, Cornell University*

We review the conception and development of two-dimensional heterojunction interlayer field effect transistor (Thin-TFET), where a steep subthreshold swing (SS) and a high on-current are estimated theoretically. The Thin-TFET has been experimentally demonstrated using WSe₂/SnSe₂ stacked heterostructures, where the SS is mostly likely limited by the interfacial trap density of states and the parasitic MOSFET. Due to its vertical stacking structure, Thin-TFET intrinsically has a smaller gate-drain capacitance compared to the conventional lateral pin-TFET. In turn, this results in mitigated Miller Effect in Thin-TFET thus reducing dynamic energy dissipation in circuits.

3:10 PM

19.3 Hybrid Phase-Change – Tunnel FET (PC-TFET) Switch with Subthreshold Swing < 10 mV/decade and sub-0.1 body Factor: Digital and Analog Benchmarking, *E. Casu, W. Vitale, N. Oliva, T. Rosca, C. Alper, A. Biswas, A. Krammer, G. Luong*, Q. Zhao*, S. Mantl*, A. Schuler, A. Seabaugh** and A. Ionescu, EPFL*, **Peter Grünberg Institut, **University of Notre Dame*

In this paper we report the first hybrid Phase-Change – Tunnel FET (PC-TFET) device configurations for achieving a deep sub-thermionic steep subthreshold swing at room temperature and subthreshold power savings. The proposed hybrid device feedbacks the steep transition of Metal-Insulator transition in a VO₂ structure into Gate or Source configurations of strained silicon nanowire Tunnel FETs, to achieve a switching with I_{on}/I_{off} better than 5.5×10^6 and with a subthreshold swing of 4.0 mV/dec at 25 °C. We demonstrate that the principle of PC-TFET switching relates to an internal amplification resulting in a sub-unity body factor, m , which is reduced to values below 0.1 for a current range larger than 2-3 decades. We report a full experimental digital and analog benchmarking of the new device and compare it with Tunnel FETs and CMOS.

Remarkably, the PC-TFET can achieve analog figures of merit like gm/Id breaking the 40 V-1 limit of MOSFETs. We demonstrate and report the first buffered oscillator cell for neuromorphic computing exploiting the gate configuration of PC-TFET.

3:35 PM

19.4 Demonstrating Performance Improvement of Complementary TFET Circuits by I_{ON} Enhancement Based on Isoelectronic Trap Technology, *T. Mori, H. Asai, J. Hattori, K. Fukuda, S. Otsuka, Y. Morita, S. Ouchi, H. Fuketa, S. Migita, W. Mizubayashi, H. Ota and T. Matsukawa, National Institute of Advanced Industrial Science and Technology (AIST)*

IET technology, which enhances tunneling probability, successfully increased the ON current in Si-TFETs. The I_{ON} enhancement improved the inverter and ring oscillator (RO) circuit performance. The RO circuit operation with the complementary TFET inverters was demonstrated for the first time. IET technology may provide a breakthrough towards realizing TFET circuits.

4:00 PM

19.5 Tunneling MOSFET Technologies using III-V/Ge Materials (Invited), *S. Takagi, D. Ahn, M. Noguchi, T. Gotow, K. Nishi, M. Kim and M. Takenaka, The University of Tokyo*

The critical issues, technical challenges and viable technologies of tunneling MOSFETs (TFET) utilizing III-V/Ge materials are examined in this study. N-channel TFETs using InGaAs bulk and quantum well (QW) homo-junctions, GaAsSb/InGaAs and Ge/strained SOI type-II hetero-junction are fabricated with emphasis on the superior source p+/n junction formation and the electrical properties are experimentally evaluated.

4:25 PM

19.6 Performance Benchmarking of p-type In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6} and Ge/Ge_{0.93}Sn_{0.07} Hetero-junction Tunnel FETs, *R. Pandey, C. Schulte-Braucks***, R. N. Sajjad**, M. Barth, R.K. Ghosh*, B. Grisafe*, P. Sharma*, N. von den Driesch***, A. Vohra^, B. Rayner^^, R. Loo^, S. Mantl***, D. Buca***, C-C. Yeh^^, C-H. Wu^^, W. Tsai^^, D. Antoniadis** and S. Datta*, The Pennsylvania State University, *University of Notre Dame, **Massachusetts Institute of Technology, ***Peter Grünberg Institute (PGI-9) and JARA-FIT, Forschungszentrum Jülich GmbH, ^IMEC, ^^Kurt J. Lesker Company, ^^Taiwan Semiconductor Manufacturing Company*

Experimental demonstration of PTFETs at low |V_{DS}|=0.5V is presented using Group III-V (In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}) and Group IV (Ge/Ge_{0.93}Sn_{0.07}) semiconductor hetero-junctions exhibiting record minimum switching slope performance. This is enabled by engineering high quality gate stacks on GaAs_{0.4}Sb_{0.6} and Ge_{0.88}Sn_{0.12} substrates with thinnest demonstrated EOT of ~ 0.8 nm. Harnessing low direct band gap advantage in Ge_{1-X}Sn_X PTFETs, together with 10× lower Dit over competing Group III-V In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6} PTFETs, are excellent candidates for PTFETs with high I_{ON} and sub-kT/q SS.

4:50 PM

19.7 Vertically Stacked Gate-All-Around Si Nanowire CMOS Transistors with Dual Work Function Metal Gates, *H. Mertens, R. Ritzenthaler, A. Chasin, T. Schram, E. Kunnen, A. Hikavy, L.-Å. Ragnarsson, H. Dekkers, T. Hopf, K. Wostyn, K. Devriendt, S. A. Chew, M. S. Kim, Y. Kikuchi, E. Rosseel, G. Mannaert, S. Kubicek, S. Demuyne, A. Dangol, N. Bosman, J. Geypen, P. Carolan, H. Bender, K. Barla, N. Horiguchi and D. Mocuta, Imec*

We report on the CMOS integration of vertically stacked gate-all-around (GAA) silicon nanowire MOSFETs, with matched threshold voltages (V_{T,SAT} ~ 0.35V) for N- and P-type devices. The V_T setting is enabled by nanowire-compatible dual-work-function metal integration in a high-k last replacement metal gate process. Furthermore, we demonstrate that N- and P-type junction formation can influence nanowire release differently due to both implantation-induced SiGe/Si intermixing and doping effects. These findings underline that junction formation and nanowire release require co-optimization in GAA CMOS technologies.

Session 20: Power Devices – Focus Session: System-level Impact of Power Devices

Tuesday, December 6, 2:15 p.m.

Continental Ballroom 6

Co-Chairs: Clemens Ostermaier, Infineon Technologies

Jan Hoentschel, GLOBALFOUNDRIES

2:20 PM

20.1 Wide Bandgap (WBG) Power Devices and Their Impacts On Power Delivery Systems (Invited), *A. Huang, NC State University*

Wide bandgap (WBG) power semiconductor devices have the capability to reach higher voltage, higher frequency and higher temperature compared with silicon based power devices. These capabilities have the potentials to revolutionize the way we deliver and manage power in the future. This paper reviews the WBG progress and their potential transformative impacts on low voltage, medium voltage and high voltage power delivery systems.

2:45 PM

20.2 Si, SiC and GaN Power Devices: An Unbiased View on Key Performance Indicators (Invited), *G. Deboy, M. Treu, O. Haeberlen and D. Neumayr**, *Infineon Technologies Austria AG, *ETH Zurich*

This paper discusses key parameters such as capacitances & switching losses for silicon, SiC and GaN power devices with respect to applications in switch mode power supplies. Whereas wide bandgap devices deliver roughly one order of magnitude lower charges stored in the output capacitance, the energy equivalent is nearly on par with latest generation Superjunction devices. Silicon devices will hence prevail in classic hard switching applications at moderate switching frequencies whereas SiC and GaN based power devices will play to their full benefits in resonant topologies at moderate to high switching frequencies.

3:10 PM

20.3 System Level Impact of GaN Power Devices in Server Architectures (Invited), *A. Lidow, J. Glaser and D. Reusch*, *Efficient Power Conversion Corporation*

Gallium Nitride (GaN) integrated circuits and discrete transistors give the power system engineer a new set of tools for improving efficiency, cost, and power density in server and telecom systems. In this paper we examine the new benchmarks in performance as well as the various tradeoffs involved in designing power systems that take an input of 48 V and deliver it to the final destination – a 1 V digital load.

3:35 PM

20.4 GaN-based Semiconductor Devices for Future Power Switching Systems (Invited), *H. Ishida, R. Kajitani, Y. Kinoshita, H. Umeda, S. Ujita, M. Ogawa, K. Tanaka, T. Morita, S. Tamura, M. Ishida and T. Ueda*, *Panasonic Corporation*

Current status of GaN-based Gate Injection Transistors (GITs) with p-type gate on AlGaIn/GaN hetero structure and their application to power switching systems such as DC/DC converter ICs, together with methodologies for reducing on-resistance, increasing breakdown voltage, and suppressing current collapse are summarized.

4:00 PM

20.5 Application Reliability Validation of GaN Power Devices (Invited), *S. Bahl, J. Joh, L. Fu, A. Sasikumar, T. Chatterjee and S. Pendharkar*, *Texas Instruments*

Standard qualification methodology does not specify product-level testing. We show that it is not sufficient to assure good product-level operation. However, by adding hard-switching testing, we show that devices that pass "qual" but perform poorly in application can be detected. As a result, our devices pass qual and perform well in application.

4:25 PM

20.6 Horizon Beyond Ideal Power Devices (Invited), *H. Ohashi, NPERC-J*

Inconvenient truth is confronting us when we investigate possibility of the future power electronics and power devices. It is that efficiency of power convertor is approaching to full percentage. Change of target in power electronics progress is discussed from efficiency to prevalence of the efficient use of electrical energy. Standing on this viewpoint, new concept, nega-watt cost is proposed. In term of the nega-watt cost, role of advanced power devices are discussed looking at horizon beyond ideal power devices in efficiency.

Session 21: Characterization, Reliability and Yield - Reliability and Characterization of Memory Devices, Contacts and Interfaces

Tuesday, December 6, 2:15 p.m.

Imperial Ballroom A

Co-Chairs: Seokiu Lee, SK Hynix
Ehrenfried Zschech, Fraunhofer IKTS Dresden

2:20 PM

21.1 Reliability Study of a 128Mb Phase Change Memory Chip Implemented with Doped Ga-Sb-Ge with Extraordinary Thermal Stability, *W.-C. Chien, H.Y. Cheng, M. BrightSky*, A. Ray*, C.W. Yeh, W. Kim*, R. Bruce*, Y. Zhu*, H.Y. Ho, H.L. Lung and C. Lam*, Macronix International, *IBM T.J. Watson Research Center*

The comprehensive reliability study for the relationship between cycling endurance and thermal stability on a 128Mb PCM chip using modified doped Ga-Sb-Ge material is demonstrated. The chip exhibited excellent data retention for 10 years at 215C after 1K pre-cycles, 210C after 10K pre-cycles, and 205C after 100K pre-cycles.

2:45 PM

21.2 Impact of the Filament Morphology on the Retention Characteristics of Cu/Al₂O₃-based CBRAM Devices, *K. Ota, A. Belmonte*, Z. Chen*, A. Redolfi*, L. Goux* and G. S. Kar*, Toshiba Corp., *imec*

In this paper, we demonstrate that the morphology of the conductive filament is the key parameter to control the data retention characteristics of CBRAM devices. In particular, we prove that the evolution of the LRS and HRS distributions is qualitatively related to the filament shape, whereas it is influenced quantitatively by the materials constituting the CBRAM stack, and we propose the peculiar hourglass filament shape as a solution for enabling optimal retention performances. Further analysis of the effect of cycling on retention confirms the key role of the filament morphology in the CBRAM data retention trend.

3:10 PM

21.3 Microsecond Transient Thermal Behavior of HfOx-based Resistive Random Access Memory Using a Micro Thermal Stage (MTS), *Z. Jiang, Z. Wang, X. Zheng, S. Fong, S. Qin, H.-Y. Chen*, C. Ahn, J. Cao, Y. Nishi and H. -S. P. Wong, Stanford University, *GigaDevice Semiconductor, Inc.*

Microsecond transient thermal disturbance (TD) on the conduction and switching of HfOX-based resistive random access memory (RRAM) is investigated using a micro thermal stage (MTS). Temperature-dependent measurement (298 – 1134 K) induced from MTS is applied to the RRAM during forming, read, write, and reliability measurements for DC and AC conditions. In this work, the time scale of the temperature-dependent measurement is extended from DC down to ~ 10 μ s. Various mechanisms (drift, Soret and Fick diffusion) of the ion migration are analyzed using MTS-induced heating. A compact model is developed to capture drift and diffusion mechanisms. TD in the middle layer of 3D array (64 \times 64 \times 32) is estimated. More than 20 % devices can be programmed with a resistance shift at the next cycle caused by TD. 2.2 % devices may have a write failure.

3:35 PM

21.4 Identify the Critical Regions and Switching/failure Mechanisms in non-filamentary RRAM (a-VMCO) by RTN and CVS Techniques for Memory Window Improvement, *J. Ma, Z. Chai, W. Zhang, B. Govoreanu*, J. Zhang, Z. Ji, B. Benbakhti, G. Groeseneken* and M. Jurczak*, Liverpool John Moores Univeristy, *imec*

A novel method combining RTN, CVS and Weibull-plot has been developed for non-filamentary RRAM, which, for the first time, enables the identification of its switching and failure mechanisms at defect level, through directly observing the profile modulation of pre-existing defects and progressive formation of conductive percolation path by generated defects.

4:00 PM

21.5 Technology for Reliable Spin-Torque MRAM Products (Invited), *J.M. Slaughter, K. Nagel, R. Whig, S. Deshpande*, S. Aggarwal, M. DeHerrera, J. Janesky, M. Lin, H.-J. Chia, M. Hossain, S. Ikegawa, F.B. Mancoff, G. Shimon, J.J. Sun, M. Tran, T. Andre, S. M. Alam, F. Poh*, J.H. Lee*, Y.T. Chow*, Y. Jiang*, H.X. Liu*, C.C. Wang*, S.M. Noh*, T. Tahmasebi*, S.K. Ye* and D. Shum*, Everspin Technologies, Inc., *GLOBALFOUNDRIES Singapore PTE, Ltd.*

In this paper we present an overview of important features for reliable and manufacturable ST-MRAM as well as new results in two areas: pMTJ arrays with data retention sufficient for programming before 260°C wave solder, and performance of a 256Mb, DDR3 ST-MRAM product chip.

4:25 PM

21.6 Understanding Cycling Endurance in Perpendicular Spin-transfer Torque (p-STT) Magnetic Memory, *R. Carboni**, *S. Ambrogio**, *W. Chen*, *M. Siddik*, *J. Harms*, *A. Lyle*, *W. Kula*, *G. Sandhu* and *D. Ielmini**, *Micron Technology*, **Politecnico di Milano*

Perpendicular spin-transfer torque (p-STT) memory is attracting an increasing interest as storage class memory (SCM) or static/dynamic RAM replacement. In these applications, high speed and extended endurance are essential and sometimes conflicting requirements. This work addresses cycling endurance of p-STT devices by pulsed experiments and modeling of the dielectric breakdown. We present a new endurance model able to predict the STT endurance as a function of applied voltage, pulse width, pulse polarity and delay time. The trade-off between write time and endurance for RAM replacement is finally addressed.

4:50 PM

21.7 Graphenic Carbon-Silicon Contacts for Reliability Improvement of Metal-Silicon Junctions, *M. Stelzer* and *F. Kreupl*, *Technical University of Munich*

Graphenic carbon-silicon Schottky contacts are demonstrated that have a very low Schottky barrier height. In contrast to conventional metal-based contacts (like TiSi), they are over 100 million times more stable against high current pulses. The C-Si contact properties even show promise to establish an ultra-low, high temperature stable contact resistance.

Session 22: Optoelectronics, Displays, and Imagers - Optoelectronic Integration

Tuesday, December 6, 2:15 p.m.

Imperial Ballroom B

Co-Chairs: Zhiping (James) Zhou, Peking University

Boon S. Ooi, KAUST

2:20 PM

22.1 High-mobility TFT and Enhanced Luminescence Utilizing Nucleation-controlled GeSn Growth on Transparent substrate for Monolithic Optoelectronic Integration, *H. Oka*, *M. Koyama*, *T. Tomita*, *T. Amamoto*, *K. Tominaga*, *S. Tanaka*, *T. Hosoi*, *T. Shimura* and *H. Watanabe*, *Osaka University*

We proposed a novel GeSn growth technique on transparent substrate based on the liquid-phase crystallization and obtained high-quality tensile-strained GeSn alloy on quartz substrate. Significantly enhanced direct bandgap luminescence and high-performance GeSn p- and n-type TFTs were demonstrated for the first time.

2:45 PM

22.2 First Demonstration of a Back-Side Integrated Heterogeneous Hybrid III-V/Si DBR Lasers for Si-Photonics Applications, *J. Durel*, *B. B. Bakir**, *C. Jany**, *S. Cremer*, *B. Szelag**, *T. Bria**, *V. Larrey**, *L. Sanchez**, *P. Brianceau**, *J.-A. Dallery***, *R. Guiavarch**, *T. Card**, *R. Thibon**, *J.-E. Broquin**** and *F. Boeuf***, *STMicroelectronics*, **CEA-LETI*, ***Vistec Electron Beam GmbH*, ****University of Grenoble Alpes*

In this paper, we demonstrate for the first time the integration of a III-V/Si hybrid laser on the back-side of a SOI wafer. This integration allows preserving the compatibility with Si-waveguide integration and with CMOS front-side metal interconnects, while leveraging passive and active photonic device design.

3:10 PM

22.3 GeSn Lasers for CMOS Integration (Invited), *D. Buca*, *N. von den Driesch*, *D. Stange*, *S. Wirths*, *R. Geiger**, *C. Schulte Braucks*, *S. Mantl*, *J.M. Hartmann***, *Z. Ikonc****, *J. Witzens^*, *H. Sigg* and *D. Grützmacher*, *Forschungszentrum Jülich GmbH*, **LMN*, ***CEA*, *LETI*, *MINATEC*, ****University of Leeds*, *^RWTH Aachen*

3:35 PM

22.4 High Gain Semiconductor Optical Amplifier – Laser Diode at Visible Wavelength, *C. Shen*, *C. Lee**, *T. K. Ng*, *S. Nakamura**, *J. Speck**, *S. DenBaars**, *A. Alyamani***, *M. El-Desouki*** and *B. Ooi*, *King Abdullah University of Science and Technology*, **University of California, Santa Barbara*, ***King Abdulaziz City for Science and Technology*

We reported on the first experimental demonstration of a two-section semipolar InGaN-based laser diode with monolithically integrated semiconductor optical amplifier (SOA-LD). The onset of amplification effect was measured at 4V SOA bias (VSOA). The SOA-LD shows a large gain of 5.32dB at VSOA=6V.

4:00 PM

22.5 The Zener-Emitter: A Novel Superluminescent Ge Optical Waveguide-Amplifier with 4.7 dB Gain at 92 mA Based on Free-Carrier Modulation by Direct Zener Tunneling Monolithically Integrated on Si, *R. Koerner, D. Schwarz, I. Fischer, L. Augel, S. Bechler, L. Haenel, M. Kern, M. Oehme, E. Rolseth, B. Schwartz*, D. Weisshaupt, W. Zhang and J. Schulze, University of Stuttgart, *Brandenburg University of Technology Cottbus-Senftenberg*

Experimental demonstration of a Ge optical-amplifier and superluminescent light source on Si (100). Direct Zener tunnel injection with 38 mV/dec features optical-amplification up to 4.7 dB at 92 mA, gain-bandwidth of 98 nm (150 cm⁻¹) and pulsed lasing at 1667 nm (90 mA threshold) in a 1 mm waveguide.

4:25 PM

22.6 On-chip Optical Sense Strategy Illustrated in the Case of Flash Memory System, *J. Song, X. Luo, Y. Tang*, C. Li, L. Jia, X. Tu, Q. Fang, Y. Huang, H. Zhou, E.-J. Lim, T.-Y. Liow and G.-Q. Lo, A*STAR, *NXP Semiconductors*

Different from traditional electronically-sensing memory states scheme, we propose and demonstrate an optical-sensing strategy, which enables all memory states being sense simultaneously. We illustrate the concept through the monolithic on-chip integration of optical microring resonator and memory array. The results show 1200× sensing speed improvement and with large up-scale potential.

Session 23: Evening Panel

Tuesday, December 6, 8:00 p.m.

Continental Ballrooms 1-4

How Will Semiconductor Industry Change to Enable 30 Billion Connected Devices?

Moderator: *Aaron Thean, University of Singapore*

The deca-nanometer technology nodes from 28nm to the imminent 10nm supported the growth of smart phones, ultra books, and tablets, which drove the wireless and smart mobile devices market, over the last 10 years. As we enter the sub-deca-nanometer era of 7nm, 5nm, and beyond, we are transitioning into a new era in the application space. Not only will the demands for communication grow to the next order of magnitude (E.g. 5G), the diversity of application drivers may explode as well (E.g. Cloud servers, Field-Area Networks, Edge sensor nodes, etc.). We see technology advancing in terms of more energy-efficient microprocessors/microcontrollers/systems-on-chip targeting smart watches, sensors for smart homes, and ultra-portable electronics. This is accompanied by strong demands for more function integration, but also at much lower component costs and narrower profit margin? At the same time, we asks: How will new applications in autonomous vehicles, next-generation robotics/drones, and machine learning systems generate new waves of semiconductor electronic demands? Nonetheless, these drivers can lead to very fragmented needs in terms of semiconductor technologies from More-Moore to More-than-Moore. Hence, will business-as-usual continue to serve the market, or the Semiconductor industry should change to capture value? What does this mean for Semiconductor technology R&D and the technology roadmap(s)? How will that affect electron device researchers?

To get a pulse of what's happening, we have invited 5 distinguished technology experts from the Semiconductor Industry and Research Institutes to share their views. We hope to get a lively discussion and a sharing of minds between them and the IEDM community through this event.

Panelists:

Reza Arghavani, LAM Research
Ning Chen, Intel
Jean-Eric Michhallet, CEA LETI

Rajeev Rajan, GlobalFoundries
Jeff Xu, Qualcomm

Session 24: Evening Panel

Tuesday, December 6, 8:00 p.m.

Continental Ballrooms 6-9

Challenges and Opportunities for Neuromorphic and Machine Learning

Moderator: *Marc Duranton, CEA-LIST*

The panelists will discuss in this session the challenges and opportunities for neuromorphic systems and machine learning. After a first explosion in the 1990's, the interest for neuromorphic architectures is now again growing and applications based on Deep Learning are more and more hot topics. This is illustrated by the development of hardware and software solutions by Baidu, Facebook, Google, IBM, Qualcomm etc.

This panel will discuss whether neuromorphic architectures could be a good answer to the challenges of energy efficiency and of processing "natural" data. It will also have a focus on hardware accelerators, ranging from solutions using standard data encoding to solutions using "spike" based encoding.

Examples of questions to be answered could be:

- 1) What are Neuromorphic and deep learning systems, their relation(s) with machine learning and Artificial Intelligence? Why they are high in the hype curve?
- 2) Neuromorphic and Deep Learning, for which applications?
- 3) What are the current sweet spot(s) and limitation(s) of the Neuromorphic and machine learning?
 - For example, are neuromorphic architectures good answer to challenges of energy efficiency and of processing "natural" data such as images and voice?
- 4) What are the current approach(es) for neuromorphic computing and for deep learning? – Are we getting close or on the wrong track?
- 5) What is required in terms of hardware? And in term of software?
- 6) What will be the next step(s), what are the challenges to be solved for the various approaches?

Panelists:

Chung Lam, IBM TJ Watson Research Center
Karam Chatha, Qualcomm
Subhasish Mitra, Stanford (EE and CS)

Praveen Raghavan, IMEC
Carlo Reita, Director, CEA-Leti
Manan Suri, IIT Delhi

Session 25: Process and Manufacturing Technology - Beyond Conventional CMOS

Wednesday, December 7, 9:00 a.m.

Grand Ballroom A

Co-Chairs: John Dukovic, Applied Materials

Guilhem Larrieu, CNRS LAAS

9:05 AM

25.1 Heterostructure at CMOS Source/drain: Contributor or Alleviator to the High Access Resistance Problem?,

H. Yu, M. Schaekers, E. Rosseel, J. L. Everaert, P. Eyben, T. Chiarella, C. Merckling, T. Agarwal, G. Pourtois, A. Hikavy, S. Kubicek, L. Witters, A. Sibaja-Hernandez, J. Mitard, N. Waldron, S. Chew, S. Demuyne, N. Horiguchi, K. Barla, A. Thean, A. Mocuta, D. Mocuta, N. Collaert, and K. De Meyer, imec

This paper studies heterostructure interface resistivity with experiments and simulations. The paper elaborates on how to reduce resistances between p-SiGe/p-Si, and how to make use of favorable conduction band alignment property of n-Si/n-Ge to achieve ultralow contact resistivity on n-Ge. n-InAs/n-Si and n-InAs/n-Ge heterostructures are qualitatively discussed.

9:30 AM

25.2 General Relationship for Cation and Anion Doping Effects on Ferroelectric HfO₂ Formation,

L. Xu, S. Shibayama, K. Izukashi, T. Nishimura, T. Yajima, S. Migita and A. Toriumi, The University of Tokyo, *National Institute of Advanced Industrial Science and Technology*

This work discusses the general relationship for cation and anion doping effects on the HfO₂ para-/ferroelectric transition, which will provide us a helpful instruction for precise HfO₂ ferroelectricity design. In addition, ferroelectric N-doped HfO₂ has been demonstrated as a gate dielectric film on an oxide semiconductor for ferroelectric field-effect transistors (FeFETs).

9:55 AM

25.3 Monolithic Integration of AgTe/TiO₂ Based Threshold Switching Device with TiN Liner for Steep Slope Field-Effect Transistors, *J. Song, J. Park, K. Moon, J. Woo, S. Lim, J. Yoo, D. Lee and H. Hwang, Pohang University of Science and Technology (POSTECH)*

AgTe/TiN/TiO₂/TiN threshold switching (TS) device was monolithically integrated with silicon MOSFET to demonstrate steep subthreshold slope field-effect transistors. The TS device with AgTe top electrode showed the high on-current, since the Te allows an extraction of the Ag out of the filament. The TiN liner was also inserted at the AgTe/TiO₂ interface to prevent in-diffusion of Ag into the TiO₂ layer during back-end-of-line process. Finally, the transistor with TS device has a sub-5-mV/dec subthreshold slope (SS) and a high on/off current ratio (Ion/Ioff) of >10⁸ with a low drain voltage (0.5 V) even after the 400°C annealing process.

10:20 AM

25.4 Cost-effective Fabrication of In_{0.53}Ga_{0.47}As-on-Insulator on Si for Monolithic 3D via Novel Epitaxial Lift-Off (ELO) and Donor Wafer Re-use, *S. K. Kim, J. Shim, D.-M. Geum, C. Z. Kim**, H.-S. Kim, Y.-S. Kim, H.-K. Kang, J. D. Song, S.-J. Choi*, D. H. Kim*, W. J. Choi, H.-J. Kim, D. M. Kim*, S.H. Kim, Korea Institute of Science and Technology (KIST), *Kookmin University, **Korea Advanced Nanofab Center (KANC)*

Defect-less semiconductor-on-insulator (-OI) by a cost-effective and low temperature process is strongly needed for monolithic 3D (M3D) integration. Toward this, in this paper, we present a cost-effective fabrication of the InGaAs-OI structure featuring the direct wafer bonding (DWB) and the epitaxial lift-off (ELO) techniques as well as the re-use of the InP donor wafer. We systematically investigated the effects of the pre-patterning of the III-V layer before DWB, surface reforming (hydrophilic), and electro-chemical etching to speed up the ELO process for a fast and high-throughput process, which is essential for cost reduction. We also demonstrated the re-usability of the InP donor wafer. Finally, as a result of the high film quality of the InGaAs channel combined with DWB and ELO, fabricated InGaAs-OI MOSFETs show a record-high effective mobility of ~2800 cm²/Vs among surface channel In_{0.53}Ga_{0.47}As MOSFETs reported so far.

10:45 AM

25.5 Extremely High Modulation Efficiency III-V/Si hybrid MOS Optical Modulator Fabricated by Direct Wafer Bonding, *J. Han, M. Takenaka and S. Takagi, The University of Tokyo and CREST*

We have demonstrated an optical modulator with an InGaAsP/Si hybrid MOS-based phase shifter on Si photonics platform by using direct wafer bonding. Since the larger electron-induced refractive index change in InGaAsP than Si, a modulation efficiency $\sqrt{\pi}L$ of 0.047 Vcm, which is approximately 5 times larger than Si, is achieved.

11:10 AM

25.6 Additive Manufacturing for Electronics "Beyond Moore" (Invited), *J. Veres, R. Bringans, E. Chow, J.P. Lu, P. Mei, S. Ready, D. Schwartz and R. Street, PARC, a Xerox Company*

Additive manufacturing and 3D printing are poised to reshape entire manufacturing value chains. To be truly disruptive, additive manufacturing has to move beyond shapes and colors. Novel printing technologies are beginning to emerge that enable conformal electronics and even printing with inks containing microchips. This in turn also creates new openings for the progress of electronics itself. Over the last 50 years silicon microelectronics advanced through shrinking device dimensions and packing more and more functionality into tiny spaces. Printing technologies open up exciting new ways of scaling electronics "Beyond Moore", through the integration of micro and macro, creating new form factors, complex shapes, conformal devices and distributed systems. Printed, hybrid electronics systems will enable new classes of sensor systems, structural electronics and wearable devices, where the "system is the package"

Session 26: Sensors, MEMS, and BioMEMS - N/MEMS for Physical, Chemical, and Bio-sensing

Wednesday, December 7, 9:00 a.m.

Continental Ballroom 1-3

Co-Chairs: Maryam Ziaei, iSono Health

Marc Faucher, IEMN-CNRS

9:05 AM

26.1 Solid State pH and Chloride Sensor with Microfluidic Reference Electrode, *M. Zevenbergen, G. Altena, V. A. Dam, M. Goedbloed, P. Bemnowicz, P. McGuinness*, H. Berney*, A. Berduque*, T. O'Dwyer* and R. van Schaijk, Holst Centre/imec, *Analog Devices Inc.*

We present for the first time a miniaturized multi ion-selective sensor to simultaneously determine pH and chloride (Cl⁻) levels in fluid. The sensor combines solid state iridium oxide (IrOx) and silver chloride (AgCl) electrodes fabricated on a Si substrate with a microfluidic reference electrode (RE). The drift of the RE is similar to a standard RE while the internal reservoir is orders or magnitude smaller. The drift rate depends on the RE geometry as predicted by a model based on diffusion. The sensitivity, response time and accuracy were determined using solution with known composition, household solutions and samples of sweat and saliva. Overall performance is similar or even exceeds standard, relatively large and expensive ion-selective sensors.

9:30 AM

26.2 Fast Spintronic Thermal Sensor for IC Power Driver Cooling Down, *Y. Jiang, Y. Zhang, A. Klemm and J.-P. Wang, University of Minnesota*

A novel thermal sensor is designed and fabricated based on spin-transfer torque operated magnetic tunnel junction (STT-MTJ) device. It can fulfill thermal detection and overheat protection on integrated circuit. Moreover, it shows over 10 times faster thermal transit response speed than that of traditional CMOS thermal sensor. The unique property is really helpful for controlling integrated circuit's temperature due to heating by leakage current. A power driver at full loading situation is used to demonstrate this design. It shows that the sensor can be adopted as adaptive manner in a power source scaling strategy to cool down the IC in an effective way, showing a promising potential application not only as discrete sensor, but also as power solution for IC driver.

9:55 AM

26.3 Encapsulated Inertial Systems (Invited), *C.H. Ahn, D.L. Christensen, D.B. Heinz, V.A. Hong, E. J. Ng, J. Rodriguez, Y. Yang, G. O'Brien and T. Kenny, Stanford University*

There is significant interest in integration of multiple MEMS functionalities into a single compact device. Our group has developed a wafer-scale encapsulation process that provides an ultraclean, stable environment for operation of MEMS timing references, which has been commercialized by SiTime, Inc. In this paper, we discuss some of the issues associated with incorporation of inertial sensors into this encapsulation process, including design constraints, stiction, pressure, and other issues.

10:20 AM

26.4 Triboelectric Energy Harvester with an Ultra-Thin Tribo-Dielectric Layer by Initiated CVD and Investigation of Underlying Physics in the Triboelectricity, *D. Kim, W.-G. Kim, I. K. Jin, H. Park, M. J. Kwak, S. G. Im, and Y.-K. Choi, Korea Advanced Institute of Science and Technology (KAIST)*

A thickness effect of a tribo-dielectric layer (TDL) made of ultra-thin polymer in a triboelectric energy harvester (TEH) is experimentally and comprehensively studied. The TDL was deposited by the initiated chemical vapor deposition (i-CVD) method and its thickness was precisely controlled to analyze the thickness effect. The correlation between the thickness of the TDL and the output performance is experimentally determined and analytically understood with the aid of the dynamic contact-separation model. In contrast to the conventional static contact-separation model, in this case the output performance increases as the thickness of the TDL increases owing to the dynamic behavior of the electron, which includes drift and recombination phenomenon in the TDL.

10:45 AM

26.5 GaN-on-Si μ LED Optoelectrodes for High-spatiotemporal-accuracy Optogenetics in Freely Behaving Animals, *K. Kim, D. English*, S. McKenzie*, F. Wu, E. Stark*, J. Seymour, P.-C. Ku, K. Wise, G. Buzsaki* and E. Yoon, University of Michigan, *New York University*

We present the micromachined GaN-on-Si μ LED optoelectrodes with neuron-sized LEDs monolithically integrated on thin-and-narrow silicon shanks for optical stimulation and electrical recording in a behaving animal. In vivo validation of the fabricated optoelectrode confirmed the successful light-induced modulation of neuronal activities in hippocampus with 100- μ m long square optical pulses.

11:10 AM

26.6 Observation of Acoustoelectric Effect in Micromachined Lamb Wave Delay Lines with AlGaN/GaN Heterostructure, *H. Zhu, A. Ansari, W. Luo and M. Rais-Zadeh, University of Michigan*

We report on the first time observation of acoustoelectric (AE) effect from the interaction of acoustic Lamb waves and two-dimensional electron gas (2DEG) in an AlGaN/GaN heterostructure. Micro-fabricated Lamb wave delay lines are used to launch and guide travelling acoustic waves through the 2DEG region, resulting in a DC current flow between two ohmic contacts positioned on the delay line. The Lamb wave delay line shows much better acoustic transmission efficiency than the conventional surface acoustic wave (SAW) counterpart. The dependence of AE current on RF power and frequency is also verified.

11:35 AM

26.7 A 1 MHz 4 ppm CMOS-MEMS Oscillator with Built-In Self-Test and Sub-mW Ovenization Power, *C.-Y. Liu, M.-H. Li, R. Ganesh and S.-S. Li, National Tsing Hua University*

A 1 MHz 4 ppm temperature-stable micro-oven (uOven) controlled monolithic CMOS-MEMS oscillator has been demonstrated in this work, exhibiting heating power in sub-mW across the 100°C temperature span. The proposed novel isothermal uOven platform consists of dual heaters and a resistive temperature detector (RTD) for built-in self-test (BIST) and local resonator temperature monitoring.

12:00 PM

26.8 Sub-50 mV NEM Relay Operation Enabled by Self-Assembled Molecular Coating, *B. Osoba, B. Saha, J. Edgington, L. Dougherty, C. Qian, F. Niroui*, J. Lang*, V. Bulovic*, J. Wu and T.-J. King Liu, University of California, Berkeley, *Massachusetts Institute of Technology*

Sub-50 mV operation of nano-electro-mechanical relays is demonstrated for the first time, enabled by an anti-stiction molecular coating. Specifically, self-assembled perfluorodecyltriethoxysilane (PFDTES) is shown to be effective for reducing the switching hysteresis voltage of a relay, without dramatically increasing its ON-state resistance, enabling stable device operation at very low voltages.

Session 27: Memory Technology - MRAM

Wednesday, December 7, 9:00 a.m.

Continental Ballroom 4

Co-Chairs: Gwan-Hyeob Koh, Samsung

Hiroki Koike, Tohoku University

9:05 AM

27.1 4Gbit Density STT-MRAM using Perpendicular MTJ Realized with Compact Cell Structure, *S.-W. Chung, T. Kishi*, J.W. Park, M. Yoshikawa*, K. S. Park, T. Nagase*, K. Sunouchi*, H. Kanaya*, G.C. Kim, K. Noma*, M. S. Lee, A. Yamamoto*, K. M. Rho, K. Tsuchida*, S. J. Chung, J. Y. Yi*, H. S. Kim, Y.S. Chun, H. Oyamatsu* and S. J. Hong, SK Hynix Inc., *Toshiba Electronics Korea Corporation*

For the first time, 4Gbit density STT-MRAM using perpendicular MTJ in compact cell was successfully demonstrated. This paper includes the results regarding parasitic resistance control processes, MTJ process, and MTJ stack engineering. Both of successful 4Gb read and write operations were performed with high TMR, low I_c . This result will brighten the prospect of high-density STT-MRAM.

9:30 AM

27.2 Highly Functional and Reliable 8Mb STT-MRAM Embedded in 28nm Logic, *Y. J. Song, J. Lee, H.C. Shin, K. H. Lee, K. Suh, J. R. Kang, S. S. Pyo, H. T. Jung, S. H. Hwang, G. H. Koh, S. C. Oh, S. O. Park, J. K. Kim, J. C. Park, J. Kim, K. H. Hwang, G. T. Jeong, K. P. Lee and E. S. Jung, Samsung Electronics Corp.*

We fabricated 8Mb 1T-1MTJ STT-MRAM macro embedded in 28nm CMOS logic platform by developing novel integration/stack/patterning technologies. MTJ memory cell array was successfully embedded into Cu backend without open fail and severe degradation of magnetic property. Advanced perpendicular MTJ stack using MgO/CoFeB was developed to show high TMR value of 180% after full integration. In addition, ion beam etching (IBE) process was optimized with power, angle, and pressure to reduce a short fail below 1 ppm. Through these novel technologies, we

demonstrated highly functional and reliable 8Mb eMRAM macro having a wide sensing margin and strong retention property of 85 0C and 10yrs.

9:55 AM

27.3 Data Retention Extraction Methodology for Perpendicular STT-MRAM, *L. Tillie, E. Nowak, R. Sousa**, *M.-C. Cyrille, B. Delaet, T. Magis, A. Persico, J. Langer***, *B. Ocker***, *I.-L. Prejbeanu** and *L. Perniola, CEA-LETI, *SPINTEC, **Singulus Technologies AG*

While perpendicular STT-MRAM are seen as a promising next-generation memory, when scaling retention becomes critical and must be characterized precisely. Four extraction methods are compared taking special emphasize on accuracy and precision. They are then applied on single cell to kb-array, from 50 to 250 nm diameter cells and up to 235°C.

10:20 AM

27.4 Systematic Validation of 2x nm Diameter Perpendicular MTJ Arrays and MgO Barrier for Sub-10 nm Embedded STT-MRAM with Practically Unlimited Endurance, *J. Kan, C. Park, C. Ching**, *J. Ahn**, *L. Xue**, *R. Wang**, *A. Kontos**, *S. Liang**, *M. Bangar**, *H. Chen**, *S. Hassan**, *S. Kim, M. Pakala** and *S. Kang, Qualcomm Technologies, Inc., *Applied Materials, Inc.*

We present a comprehensive device and scalability validation of STT-MRAM for high performance applications in sub-10 nm CMOS by providing the first statistical account of barrier reliability in perpendicular magnetic tunnel junctions (pMTJs) from 70 to 25 nm diameter in 1 Gbit arrays. We have experimentally investigated the time- dependent dielectric breakdown (TDDDB) properties and the dependence of the pMTJ lifetime on voltage, polarity, duty-cycle, and temperature. A large write-to-breakdown voltage window of > 1 V ($> 20 \sigma_{avg}$) was measured and a long time-to- breakdown was projected ($> 10^{15}$ cycles) for 45 nm pMTJs, guaranteeing practically unlimited write cycles. We also reveal a dramatic enhancement of barrier reliability in conjunction with pMTJ size scaling down to 25 nm diameter, further widening the operating window at deeply scaled nodes.

10:45 AM

27.5 Novel Voltage Controlled MRAM (VCM) with Fast Read/Write Circuits for Ultra Large Last Level Cache, *H. Noguchi, K. Ikegami, K. Abe, S. Fujita, Y. Shiota**, *T. Nozaki**, *S. Yuasa** and *Y. Suzuki**, *Toshiba Corporation, *National Institute of Advanced Industrial Science and Technology*

This paper presents voltage-controlled MRAM (VCM) using fast read and write circuits for ultra-large last level cache. Our proposed circuit utilizes unipolar characteristics of voltage-torque MTJ and its voltage effects. The energy barrier is controlled by applying pulsed biases. The proposed VCM can operate even with 10%-sigma variability of fabrication.

11:10 AM

27.6 Voltage-Control Spintronics Memory (VoCSM) Having Potentials of Ultra-Low Energy-Consumption and High-Density, *H. Yoda, N. Shimomura, Y. Ohsawa, S. Shirotori, Y. Kato, T. Inokuchi, Y. Kamiguchi, B. Altansargai, Y. Saito, K. Koi, H. Sugiyama, S. Oikawa, M. Shimizu, M. Ishikawa, K. Ikegami and A. Kurobe, Toshiba Corporation*

We propose a new spintronics-based memory employing the voltage-control-magnetic-anisotropy effect as a bit selecting principle and the spin-orbit-torque effect as a writing principle. We have fabricated the prototype structure, and successfully demonstrated the writing scheme specific to this memory architecture.

Session 28: Circuit and Device Interaction - Technology Elements for 5nm Logic Platform and Advanced Automotive/IoT Applications

Wednesday, December 7, 9:00 a.m.

Continental Ballroom 5

Co-Chairs: Kang-ill Seo, Samsung Electronics

Koji Nii, Renesas Electronics

9:05 AM

28.1 A Novel Tensile Si (n) and Compressive SiGe (p) Dual-channel CMOS FinFET Co-integration Scheme for 5nm Logic Applications and Beyond, *D. Bae, G. Bae, K. Bhuwalka, S.-H. Lee, M.-G. Song, T.-S. Jeon, C. Kim, W. Kim, J. Park, S. Kim, U. Kwon, J. Jeon, K.-J. Nam, S. Lee, S. Lian, K. Seo, S.-G. Lee, J. H. Park, Y.-C. Heo, M. S. Rodder**, *J. A. Kittle**, *Y. Kim, K. Hwang, D.-W. Kim, M.-S. Liang and ES Jung, Samsung Electronics, *Advanced Logic Labs*

A novel tensile Si (tSi) and compressive SiGe (cSiGe) dual-channel FinFET CMOS co-integration scheme, aimed at logic applications for the 5nm technology node and beyond, is demonstrated for the first time, showing electrical performance benefits and excellent co-integration feasibility. A Strain-Relaxed SiGe Buffer (SRB) layer is introduced as buried stressor and successfully transfers up to ~1 GPa uniaxial tensile and compressive stress to the Si/SiGe n-/p-channels. As a result, both tSi and cSiGe devices show a 40% and 10% electron and hole mobility gain over unstrained Si, respectively. A common gate stack solution including a common interfacial layer (IL), HK, and metal gate for both n- and pFET is successfully developed. A gate stack process margin for the 5nm logic technology node is secured with low interface trap density (D_{it}) and threshold voltage (V_t) target for both the Si and SiGe devices, by skipping the dual Work Function Metal (WFM) processing and by simplifying the multi- V_{th} process module. Lastly, reliability investigation shows that tSi and cSiGe, employing the newly developed common gate stack scheme, possess superior reliability characteristics compared with those of equivalent Si devices.

9:30 AM

28.2 Extreme Scaling Enabled by 5 Tracks Cells: Holistic Design-device Co-optimization for FinFETs and Lateral Nanowires, *M. Garcia Bardon, Y. Sherazi, P. Schuddinck, D. Jang, D. Yakimets, P. Debacker, R. Baert, H. Mertens, M. Badaroglu*, A. Mocuta, N. Horiguchi, D. Mocuta, P. Raghavan, J. Ryckaert, A. Spessot, D. Verkest and A. Steegen, imec, *Qualcomm*

By optimizing design rules, layout, devices and parasitics, we show how 5 Tracks standard cells with one fin can be enabled. This reduces area by 16% without pitch scaling and provides 34% energy gain. The loss in speed of 15% can be recovered by different front-end solutions. Air gap spacers are the most efficient booster and provide an extra 16% gain in energy. Lateral Nanowires can compete in speed with FinFETs with an extra energy gain of 12% if tight vertical pitch of 10 nm between wires can be achieved.

9:55 AM

28.3 32-bit Processor Core at 5-nm Technology: Analysis of Transistor and Interconnect Impact on VLSI System Performance, *C.-S. Lee, B. Cline*, S. Sinha*, G. Yeric* and H.-S. P. Wong, Stanford University, *ARM Inc.*

32-bit processor core is implemented at 5-nm design rules to study transistor and interconnect technology and their impact on system performance. 2D-material-based FETs can theoretically achieve 2x better system performance compared to Si FinFET for the same contact resistivity; wire does not dominate at 5-nm node thanks to routing optimization.

10:20 AM

28.4 New Insights into the Near-Threshold Design in Nanoscale FinFET Technology for Sub-0.2V Applications, *X. Jiang, S. Guo, R. Wang, Y. Wang, X. Wang*, B. Cheng*, A. Asenov* and R. Huang, Peking University, *Synopsys*

Energy consumption has become the major concern of the IC industry. As a result, near-threshold-voltage (NTV) design has attracted a lot of attention for its superiority in energy efficiency. However, NTV design is faced with the key challenge—variability, especially for FinFET technology where device electrical FoMs are found to be strongly correlated. In this paper, new methodology of NTV design optimization for FinFET is proposed for the first time, and demonstrated based on silicon data. Significant improvements are achieved in the following three aspects: (1) Our newly proposed predictive compact variability models in all-region are accurately calibrated with experimental data, using a simple characterization method; (2) A new efficient approach for logic design space optimization is proposed based on a set of elaborately selected subthreshold FoMs, and the impacts of variation on energy efficiency, delay variation and failure probability are thoroughly investigated; (3) The conventional gate sizing method is also ameliorated specifically for FinFET NTV design. Based on silicon data, the proposed methodology is then demonstrated under $V_{dd}=199\text{mV}$ and $V_{dd}=145\text{mV}$, targeting energy-efficiency priority and V_{dd} priority scenarios, respectively. This work provides helpful guidelines for FinFET variation-aware near-threshold design.

10:45 AM

28.5 Novel MOS Varactor Device Optimization and Modeling for High-Speed Transceiver Design in FinFET Technology, *J. Jing, S. Wu, X. Wu, P. Upadhyaya and A. Bekele, Xilinx Inc.*

For the first time, an optimized MOS varactor design and a new physical based model for advanced FinFET process is presented for high speed analog circuit to achieve high tuning range and low jitter PLL design. The new varactor and model have been validated in 32.75 GB/s high speed transceiver design in 16nm FinFET technology.

11:10 AM

28.6 Embedded Flash Technology for Automotive Applications (Invited), *T. Yamauchi, Y. Yamaguchi, T. Kono and H. Hidaka, Renesas Electronics Corporation*

Future automotive applications such as advanced driver assistance require further progress of embedded Flash (eFlash) for automotive microcontroller units. Our split-gate MONOS eFlash has been successfully scaled down to 28nm process node, because of its excellent reliability and process scalability. Moreover our low-profile SG-MONOS structure enables to integrate with high-K metal gate CMOS for higher performance.

Session 29: Focus Session: Compound Semiconductor and High Speed Devices - Ultra-High Speed Electronics

Wednesday, December 7, 9:00 a.m.

Continental Ballroom 6

Co-Chairs: Mark Rodwell, University of California, Santa Barbara

Dae-Hyun Kim, Kyungpook National University

9:05 AM

29.1 InP HEMT Integrated Circuits Operating above 1,000 GHz (Invited), *W. Deal, K. Leong, W. Yoshida, A. Zamora and X.B. Mei, Northrop Grumman Corporation*

The last decade has seen tremendous increase in the operating frequency of transistor based in electronics. With InP HEMTs reaching 1.5 THz f_{MAX} and 610 GHz f_T , operating frequencies of integrated circuit amplifiers have seen corresponding increase to as high as 1 THz. This paper describes the transistor process, integrated circuit results at 1 THz, as well as background on packaging and measurements at this frequency.

9:30 AM

29.2 A 130 nm InP HBT Integrated Circuit Technology for THz Electronics (Invited), *M. Urteaga, J. Hacker, Z. Griffith, A. Young, R. Pierson, P. Rowell, M. Seo* and M. Rodwell, Teledyne Scientific Company, *SungKyunKwan University*

A 130 nm InP HBT IC technology has been developed capable of circuit demonstrations at > 600 GHz. Transistors demonstrate RF figures-of-merit $f_t > 500$ GHz and $f_{max} > 1$ THz. The HBTs support high current densities > 25 mA/ μm^2 with a common-emitter breakdown voltage $BV_{CEO} = 3.5$ V. The technology includes a multi-level thin-film wiring environment capable of low-loss THz signal routing and high integration density. A large-signal HBT model has been developed capable of accurately predicting circuit performance at THz frequencies. Circuit demonstrations include fundamental oscillators and amplifiers operating at > 600 GHz as well as integrated transmitter and receiver circuits.

9:55 AM

29.3 Resonant-Tunneling-Diode Terahertz Oscillators and Applications (Invited), *M. Asada and S.Suzuki, Tokyo Institute of Technology*

We report on our recent results of resonant tunneling diodes oscillating in the terahertz frequency range, including the structures for high frequency oscillation up to 1.92 THz at room temperature, high output power, high-speed direct modulation for wireless communication, and frequency tenability for spectroscopy.

10:20 AM

29.4 Physics of Ultrahigh Speed Electronic Devices (Invited), *M. Shur, Rensselaer Polytechnic Institute*

Feature sizes of advanced commercial electronic devices are now smaller than the mean free path of the electron collisions with impurities and lattice vibrations. This completely changes the physics of the electron transport. The effective field effect mobility becomes proportional to the device length because the electrons lose their drift momentum in the contacts. The high frequency impedance is strongly affected by the electron inertia and by the phase delays of the opposing electron fluxes in the device channel. The waves of the electron density (plasma waves) enable the device response well into the terahertz (THz) range of frequencies. At high excitation levels, these waves are transformed into the shock waves. The rectification and instabilities of the plasma waves enable a new generation of THz plasmonic devices. Ballistic and plasmonic effects in short channel FETs (such as commercial 10 nm Si CMOS) dramatically change the device physics. Exploring and using these effects should lead to the development of efficient and cost competitive THz electronics greatly expanding numerous applications of THz technology.

10:45 AM

29.5 InP/GaAsSb DHBTs for THz Applications and Improved Extraction of their Cutoff Frequencies (Invited), *C. Bolognesi, R. Flückiger, M. Alexandrova, W. Quan, R. Lövblom and O. Ostinelli, ETHZ*

InP/GaAsSb DHBT development is reviewed and contextualized with respect to other III-V high-speed technologies. Pertinent material properties and challenges in the proper assessment of f_{MAX} are discussed. An iterative de-embedding algorithm involving no additional test structures/measurements yields the correct f_{MAX} from unilateral gain data for both DHBTs and HEMTs.

11:10 AM

29.6 On-Chip Terahertz Electronics: From Device-Electromagnetic Integration to Energy-Efficient, Large-Scale Microsystems (Invited), *R. Han, J. Holloway, C. Jiang*, A. Mostajeran*, E. Afshari*, A. Cathelin***, Y. Zhang^, K. O^, L. Boglione^^, T. Hancock^^, C. Wang, Z. Hu and G. Zhang, Massachusetts Institute of Technology, *Cornell University, ***STMicroelectronics, ^University of Texas at Dallas, ^^Naval Research Laboratories, ^^MIT Lincoln Laboratories*

This paper summarizes our approaches which synthesize the optimum electromagnetic (EM)-wave environment around various silicon devices, in order to maximize the device efficiency with minimum passive loss and footprint. This has enabled multi-mW THz radiation in standard silicon processes. Various critical capabilities for future THz microsystems, including integrated phase locking, multi-pixel coherent imaging, and an ultra-broadband inter-chip waveguide link, are also demonstrated.

11:35 AM

29.7 Active Terahertz Metasurface Devices (Invited), *H.-T. Chen, Los Alamos National Laboratory*

Metamaterials and metasurfaces have demonstrated many unusual properties that are useful for creating high-performance terahertz devices and components. Integration of functional materials allows metasurfaces to expand their scope of applications. Here we show that hybrid metasurfaces can provide ultrafast modulation of terahertz waves that are critical for future applications in terahertz imaging and communications.

12:00 PM

29.8 Devices and Circuits in CMOS for THz Applications (Invited), *Z. Ahmad, W. Choi, N. Sharma, J. Zhang*, Q. Zhong, D.-Y. Kim, Z. Chen, Y. Zhang, R. Han+, D. Shim**, S. Sankaran***, E.Y. Seok***, C. Cao^, C. Mao^^, Shueler^^, I. Medvedev^^, D. Lary, H.-J. Nam, P. Raskin#, F. DeLucia###, J. P. McMillian###, C. F. Neese###, I. Kim####, I. Momson, P. Yelleswarapu, S. Dong, B.-K. Kim and K.K. O, University of Texas at Dallas, *NXP, **Seoul National University of Science & Technology, ***Texas Instruments Inc., ^MediaTek, ^^IDT, ^^Wright State University, #UTSouthwestern, ###Ohio State University, ####UConn Health, +MIT*

Recent advances of CMOS technology and circuits have made it an alternative for realizing capable and affordable THz systems. With process and circuit optimization, it should be possible to generate useful power and coherently detect signals at frequencies beyond 1THz, and incoherently detect signals at 40THz in CMOS.

Session 30: Modeling and Simulation - Steep Slope Devices and Nanowires

Wednesday, December 7, 9:00 a.m.

Continental Ballroom 7-9

Co-Chairs: Debdeep Jena, Cornell University

Geert Eneman, IMEC

9:05 AM

30.1 Scaling Perspective for III-V Broken Gap Nanowire TFETs: An Atomistic Study using a Fast Tight-binding Mode-space NEGF Model, *A. Afzalian, M. Passlack and Y.-C. Yeo, TSMC*

We report an in-depth atomistic study of the scaling potential of III-V GAA nanowire heterojunction TFET using an innovative tight-binding mode space technique with large speedup (up to 250×). n- and pTFET performance is best above 20 nm gate length and features a gain of 58× over a Si MOSFET.

9:30 AM

30.2 A Tunnel FET Design for High-Current, 120 mV Operation, *P. Long, J. Huang, M. Povolotskyi, D. Verreck, J. Charles, T. Kubis, G. Klimeck, B. Calhoun** and M. Rodwell***, Purdue University, **University of Virginia, ***University of California, Santa Barbara*

We report simulations of logic transistor operation at supply voltages VDD between 0.08- 0.18V. Tunnel FETs (TFETs) can operate at low voltage with low off-currents IOFF, but on-currents ION are greatly reduced by low tunneling probability. The minimum feasible VDD is constrained not only by the transistor subthreshold swing (SS) given a target ION/IOFF ratio, but also by the reduction of the drain current as the drain Fermi level approaches the channel conduction-band energy. This output conductance reduces the TFET voltage gain and impairs the logic gate noise margin; increasing the TFET threshold voltage Vth increases the noise margin while reducing both ION and IOFF. In ballistic simulations with 10-3A/m IOFF, triple- heterojunction tunnel FETs (3HJ-TFETs) show >50% tunneling probability and a high 265A/m ION at VDD=0.18V and 195A/m at VDD=0.12V. In simulations with an optical deformation constant (proportional to scattering strength) of 220meV/nm, consistent with $\alpha=1.1 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, reduces ION by 31% given fixed IOFF and VDD. In ballistic simulations, increasing Vth by 0.02V above that required for 10-3A/m IOFF, a noise margin of 24% of VDD is obtained at VDD=0.12V.

9:55 AM

30.3 Effect of Band-Tails on the Subthreshold Performance of 2D Tunnel-FETs, *H. Zhang, W. Cao, J. Kang and K. Banerjee, University of California, Santa Barbara*

Rigorous analysis of band-tails in 2D semiconductors is presented for the first time. Photoluminescence measurements, analytical modeling, and first-principle calculations, are employed to unveil the unique advantages of these materials, especially in 2D-2D lateral heterostructures, in terms of band-edge smearing and its fundamental role in determining the subthreshold performance of 2D tunnel-FETs.

10:20 AM

30.4 Multi-barrier Inter-layer Tunnel Field-Effect Transistor, *N. Prasad, X. Mou, L. Register and S. Banerjee, University of Texas at Austin*

Resonant tunneling characteristics of the inter-layer tunnel field-effect transistor (ITFET) can be made sharper by the use of multiple tunnel barrier layers within a "mITFET" variation. NEGF simulations are used to obtain the resonance characteristics. Circuit simulations illustrate how the sharper resonance can lead to lower operating voltages and power.

10:45 AM

30.5 Compact Models of Negative-Capacitance FinFETs: Lumped and Distributed Charge Models, *J. Duarte, S. Khandelwal, A. Khan, A. Sachid, Y.-K. Lin, H.-L. Chang, S. Salahuddin and C. Hu, University of California, Berkeley*

This work presents insights into the device physics and behaviors of ferroelectric based negative capacitance FinFETs (NC-FinFETs) by proposing lumped and distributed compact models for its simulation. NC-FinFET may have a floating metal between ferroelectric (FE) and the dielectric layers and the lumped charge model represents such a device. For a NC-FinFET without a floating metal, the distributed charge model should be used and at each point in the channel the ferroelectric layer will impact the local channel charge. This distributed effect has important implications on device characteristics as shown in this paper. The proposed compact models have been implemented in circuit simulators for exploring circuits based on NC-FinFET technology.

11:10 AM

30.6 Performance Projection of III-V Ultra-Thin-Body, FinFET, and Nanowire MOSFETs for two Next-Generation Technology Nodes, *M. Rau, E. Caruso*, D. Lizzit*, P. Palestri*, D. Esseni*, L. Selmi*, A. Schenk and M. Luisier, ETH Zürich, *DIEGM, Università degli studi di Udine*

The competitiveness of III-V compounds for next-generation high-performance logic switches at gate lengths 15 and 10.4 nm is confirmed using state-of-the art simulation tools. The gate-all-around nanowire architecture emerges as the only viable architecture worth scaling below 10.4 nm. III-V channels are found to significantly outperform their silicon counterparts at these nodes. The effects of series resistance combined with traps, surface roughness, alloy and electron-phonon scattering are found to deteriorate the ON-current by 50-60%.

11:35 AM

30.7 Vertically Stacked Nanowire MOSFETS for Sub-10 nm Nodes: Advanced Topography, Device, Variability, and Reliability Simulations, *M. Karner, O. Baumgartner, Z. Stanojević, F. Schanovsky, G. Strof, C. Kernstock, HW Karner, G. Rzepa* and T. Grasser**, Global TCAD Solutions GmbH, *TU Wien

Using our novel TCAD approach with advanced topology simulation, physical transport models for device performance, time-zero variability, and BTI device degradation modeling, we point out critical improvements required for the stacked NW-FET to surpass current FinFET technology for sub-10nm nodes.

Session 31: Characterization, Reliability and Yield - Reliability Modeling and Characterization of Dielectrics and Interfaces

Wednesday, December 7, 9:00 a.m.

Imperial Ballroom A

Co-Chairs: Chen Jiezhi, Shandong University

Chris H. Kim, University of Minnesota

9:05 AM

31.1 Engineering the Electronic Defect Bands at the Si_{1-x}Ge_x/IL Interface: Approaching the Intrinsic Carrier Transport in Compressively-Strained Si_{1-x}Ge_x pFETs, *C.H. Lee, R. Southwick and H. Jagannathan, IBM Research*

We identify the existence of electronic defect levels close to the Si_{1-x}Ge_x band edges associated with the Ge surface concentration at the Si_{1-x}Ge_x/IL interface ($0 < x < 0.5$). These electronic defects act as carrier scattering centers severely degrading the channel mobility and modulate the device threshold voltage. By successfully eliminating the electronic defect states at the Si_{1-x}Ge_x/IL interface, through control of the Ge surface concentration, high channel carrier mobility over wide charge densities in compressively-strained Si_{1-x}Ge_x channel pFETs is demonstrated. For the first time, the dominant scattering mechanisms for hole mobility in Si_{1-x}Ge_x channel pFETs are investigated to understand the carrier transport physics.

9:30 AM

31.2 Acceptor-like Trap Effect on Negative-Bias Temperature Instability (NBTI) of SiGe pMOSFETs on SRB, *G. Jiao, M. Toledano-Luque, K.-J. Nam, N. Toshiro, S.-H. Lee, J.-S. Kim, T. Kauerauf, E. Chung, D. Bae, G. Bae, D.-W. Kim and K. Hwang, Samsung Electronics*

In this work, the oxide electric field (E_{ox}) reduction caused by negatively charged traps is proposed to explain the robustness of SiGe pMOSFETs to negative gate bias temperature instability (NBTI) stress. The high density of negatively charged acceptor-like traps close to the SiGe valance band (E_v) lowers the E_{ox} and reduces the NBTI degradation at fixed overdrive. We demonstrate that trap engineering can be exploited to meet aggressive reliability requirements. Furthermore, it is predicted that there are no reliability issues in the SiGe pMOSFETs comparing with the Si counterparts.

9:55 AM

31.3 Fast-Trap Characterization in Ge CMOS Using Sub-1 ns Ultra-Fast Measurement System, *X. Yu, B. Chen, R. Cheng, Y. Qu, J. Han, R. Zhang and Y. Zhao, Zhejiang University*

Ge p- and n-MOSFETs with Al₂O₃/GeO_x/Ge gate stack were fabricated and characterized using a novel sub-1 ns ultra-fast measurement system. Devices operation under the conditions, that applying V_g with the ultra-fast rise edge down to less than 1 ns are confirmed. It is found that the current degradation within the first 10 ns is much more significant than that from 100 ns to longer time due to the fast trapping effect. In additions, the trap density distributions in Ge MOSFETs inside E_c and E_v are measured and calculated.

10:20 AM

31.4 Predictive As-grown-Generation (A-G) Model for BTI-induced Device/circuit Level Variations in Nanoscale Technology Nodes, *R. Gao, Z. Ji, S. Hatta, J. Zhang, J. Franco**, B. Kaczer**, W. Zhang, M. Duan, S. De Gendt**, D. Linten**, G. Groeseneken**, J. Bi*** and M. Liu***, Liverpool John Moores University, **imec, ***Institute of Microelectronics of the Chinese Academy of Sciences*

A new model for assessing NBTI and PBTI induced time-dependent variability under practical operation workloads is proposed. The model is based on a realistic understanding of different types of defects and has excellent predictive capability, as validated by comparison with experimental data. In addition, a new fast wafer-level test scheme for parameter extraction is developed, reducing test time to 1 hour/device and significantly improving the efficiency for variability tests

of nanoscale devices. The model is implemented into a commercial simulator and its applicability for circuit level simulation is demonstrated.

10:45 AM

31.5 Deep Insights into Dielectric Breakdown in Tunnel FETs with Awareness of Reliability and Performance Co-Optimization, *Q. Huang, R. Jia, J. Zhu, Z. Lv, J. Wang, C. Chen, Y. Zhao, R. Wang, W. Bu*, W. Wang*, J. Kang*, K. Hua*, H. Wu*, S. Yu*, Y. Wang and R. Huang, Peking University, *Semiconductor Manufacturing International Corporation*

The gate dielectrics reliability in Tunnel FETs (TFETs) has been thoroughly investigated for the first time, which is found to be the dominant device failure mechanism compared with bias temperature instability degradation, and is much worse than MOSFETs with the same gate stacks due to a new stronger localized dielectric field peak at gate/source overlap region. The non-uniform electric field of dielectric in TFET also leads to the different mechanisms between soft breakdown and hard breakdown failure. Moreover, dielectric-field-associated parameters are discussed in detail, showing an intrinsic trade-off between dielectrics reliability and device performance optimization caused by the positive correlation between dielectric field and source junction field. A new robust design consideration is further proposed for reliability and performance co-optimization, which is experimentally realized by a new TFET design with both dramatically improved performance and reliability, indicating its great potentials for ultralow-power applications.

11:10 AM

31.6 Comprehensive Model for Progressive Breakdown in nFETs and pFETs, *S. Lombardo, E. Wu* and J. Stathis*, CNR-IMM, IBM Research*

Through comparison with a large data set, we show that progressive breakdown (PBD) of gate oxides is described by a physical model coupling carrier energy dissipation to electromigration producing the PBD growth. Dependence on temperature, voltage, carrier type, oxide thickness, and the statistics are well described in a consistent framework.

11:35 AM

31.7 A Fundamental AC TDDDB Study of BEOL ELK in Advanced Technology, *M.N. Chang, Y.-H. Lee, S.Y. Lee and Y.S. Huang, TSMC*

In this study, we thoroughly investigated AC TDDDB in BEOL extreme low-k (ELK) dielectric in 10nm technology. We demonstrated that AC TDDDB of ELK dielectric has better median-time-to-failure (MTTF) and also much tighter Weibull distribution than constant voltage stress (DC TDDDB). In unipolar AC TDDDB stress, a very significant recovery process was observed. Through the capacitance recovery analysis, the capture and emission time constants for ELK were found to be $\sim 10^{-3}$ and $\sim 10^{-8}$ seconds respectively, which implies that there is low probability of charge trapping when the stress period is as fast as 10^{-3} seconds; meanwhile the charge detrapping happens continuously when the stress period is lower than 10^{-8} seconds. As a result, the unipolar AC TDDDB lifetime increased with increasing frequency. In addition, the unipolar AC TDDDB improvement shows a power law dependence on the duty ratio due to a very significant charge trap/detrapping effect. This is further validated through a physics-based simulation. On the other hand, bipolar AC stress caused the ion diffusion to be accompanied by the backflow Cu ion drift, thus extending the defect growth rate and improving the TDDDB performance. However, no significant frequency and duty ratio dependence on the bipolar AC to DC ratio was found because the critical Cu ion concentration was constrained by the ion diffusion mechanism. This study suggests that actual circuit operation in the AC condition should have a much longer back-end TDDDB lifetime than the projection by DC stress assessment for BEOL ELK dielectrics.

12:00 PM

31.8 Sustainable Electronics for Nano-Spacecraft in Deep Space Missions, *D.-I. Moon, J.-Y. Park*, J.-W. Han, G.-J. Jeon*, J.-Y. Kim*, J. Moon*, M.-L. Seol, C. K. Kim*, H. C. Lee*, M. Meyyappan and Y.-K. Choi*, NASA Ames Research Center, *KAIST*

On-the-fly self-healing devices are experimentally demonstrated for sustainable space electronics. High temperature generated by Joule heating in gate electrode provides on-chip annealing of ionizing radiation, hot carrier, and tunneling damages. With self-healing process, highly scaled SiNW GAA FETs show long-term reliability in Logic, floating body DRAM, and Flash memory. Thermally isolated gate structure is proposed to enhance self-healing effects.

Session 32: Optoelectronics, Displays, and Imagers - Thin Film Transistors for Imaging and Displays

Wednesday, December 7, 9:00 a.m.

Imperial Ballroom B
Co-Chairs: Soeren Steudel, IMEC
Ioannis (John) Kymissis, Columbia University

9:05 AM

32.1 An Active Artificial Iris Controlled by a 25- μ W Flexible Thin-Film Driver, *F. De Roose***, *S. Steudel*, *K. Myny*, *M. Willegems*, *S. Smout*, *M. Ameys*, *P. Malinowski*, *R. Gehlhaar*, *R. Poduval*, *X. Chen**, *J. De Smet**, *A. Vásquez Quintero*, *H. De Smet*, *W. Dehaene*** and *J. Genoe*, *imec*, **UGent*, ***KULeuven*

We show an active artificial iris with solely thin-film components, wherein several LCD elements are powered using thin-film photovoltaics (TFPV) and a-IGZO oxide TFT electronic power drive. Key aspects for the drive are size and low power consumption. We show power consumption down to 25 μ W for the full iris.

9:30 AM

32.2 High-Performance and Reliable Elevated-Metal Metal-Oxide Thin-Film Transistor for High-Resolution Displays, *L. Lu*, *J. Li*, *H. S. Kwok* and *M. Wong*, *the Hong Kong University of Science and Technology*

Incorporated with the annealing-induced source/drain (S/D), elevated-metal metal-oxide (EMMO) thin-film transistor (TFT) was proposed to provide an etch-stop (ES) layer while retain a small device size for high-resolution displays, which could not be combined in conventional TFT architectures. The "defect-populated" S/D and "defect-free" channel enabled the high performance metrics: a competitive field-effect mobility of ~ 14 cm²/Vs; an extremely low off-current of $\sim 10^{-18}$ A; an impressive on/off ratio of $\sim 10^{12}$; and the superior reliability against temperature, bias and current stresses.

9:55 AM

32.3 Polycrystalline Silicon TFTs on a Paper Substrate Using Solution-Processed Silicon, *M. Trifunovic*, *P. Sberna*, *T. Shimoda** and *R. Ishihara*, *Delft University of Technology*, **Japan Advanced Institute of Science Technology*

Polycrystalline silicon TFTs have been fabricated for the first time directly on a paper substrate using a liquid silicon solution. The fabrication temperature was limited to 100C. This work serves as a proof of concept, and opens the pathway toward low-cost, flexible electronics combined with the high performance of silicon.

10:20 AM

32.4 High-detectivity Printed Organic Photodiodes for Large Area Flexible Imagers (Invited), *A. Pierre* and *A. Arias*, *University of California, Berkeley*

10:45 AM

32.5 Dual-Gate Photosensitive FIN-TFT with High Photoconductive Gain and Near-UV to Near-IR Responsivity, *H. Ou*, *K. Wang*, *J. Chen*, *A. Nathan**, *S. Z. Deng* and *N. Xu*, *Sun Yat-sen Univeristy*, **University of Cambridge*

We report the first three-dimensional dual-gate photosensitive a-Si:H thin-film transistor operating in the sub-threshold regime for low-level light detection. The measured photoconductive gain is greater than 100 with photo-response ranging from near-ultraviolet to near-infrared wavelengths, making it a potential candidate as an image sensor for UV, visible, IR and X-rays.

11:10 AM

32.6 Extending the Functionality of FDSOI N- and P-FETs to Light Sensing, *L. Kadura*, *L. Grenouillet*, *T. Bedecarrats*, *O. Rozeau*, *N. Rambal*, *P. Scheiblin*, *C. Tabone*, *D. Blachier*, *O. Faynot*, *A. Chelnokov* and *M. Vinet*, *CEA LETI*

We demonstrate that FDSOI transistors co-integrated with a diode implemented below the buried oxide (BOX) become strongly sensitive to visible light. The carriers photogenerated in the diode create a Light-Induced VT Shift (LIVS) in both NFET & PFET transistors by means of capacitive coupling, without direct electrical connection between the photodiode and the sensing transistor. This optical back biasing effect is carefully examined as a function of both transistor and diode technological parameters. The experimental results are supported by TCAD simulations, suggesting that the proposed FDSOI/photodiode co-integration scheme can be used for efficient photodetectors. We also study the transient effects, and propose an efficient reset mechanism. Finally, we demonstrate for the first time that SRAM cells can be made controllable by light illumination.

Entrepreneurs Luncheon

Wednesday, December 7, 12:30 p.m.

Plaza A&B

Speaker: Vamsee Pamula, founder of Baebies, a newborn screening and pediatric testing company using digital microfluidics technology.

Jointly sponsored by IEDM and IEEE Women in Engineering, the Entrepreneurs Lunch will feature Vamsee Pamula, co-founder of Baebies, Inc. a company developing digital microfluidics technology for newborn screening and pediatric testing. Pamula co-founded Baebies in 2014, following the sale of a predecessor microfluidics company that he also co-founded – Advanced Liquid Logic – to Illumina, Inc.

Biography

Vamsee has years of experience with digital microfluidics. He has served as Principal Investigator on several National Institutes of Health-funded projects, and has led many talks and published more than 60 articles, five book chapters and a book on the topic. He has more than 200 issued and pending patents, a PhD in Electrical and Computer Engineering from Duke University, and also serves as Adjunct Professor there.

Session 33: Process and Manufacturing Technology - Ge Channel Devices

Wednesday, December 7, 1:30 p.m.

Continental Ballroom 4

Co-Chairs: Mitsuhiro Togo, GLOBALFOUNDRIES

Mariam Sadaka, SOITEC

1:35 PM

33.1 Record High Mobility ($428\text{cm}^2/\text{V}\cdot\text{s}$) of CVD-grown Ge/Strained $\text{Ge}_{0.91}\text{Sn}_{0.09}$ /Ge Quantum Well p-MOSFETs, *Y.-S. Huang, C.-H. Huang, F.-L. Lu, C.-Y. Lin, H.-Y. Ye, I.-H. Wong, S.-R. Jan, H.-S. Lan, C. W. Liu, Y.-C. Huang*, H. Chung*, C.-P. Chang*, S. Chu* and S. Kuppurao*, National Taiwan University, *Applied Materials Inc*

By optimizing the cap thickness, the record high mobility ($428\text{cm}^2/\text{V}\cdot\text{s}$) of the CVD grown-GeSn QW p-MOSFETs is achieved with low thermal budget of 400°C . The $\sim 7\%$ mobility enhancement on $\langle 110 \rangle$ channel direction is observed using external transverse uniaxial tensile strain of $\sim 0.11\%$ due to the reduction of effective mass. The mobility of GeSn QW p-MOSFETs increases with decreasing temperature at low N_{inv} , indicating that phonon scattering is dominated, different from bulk Ge p-MOSFETs. The normalized noise power density of GeSn p-MOSFETs decreases with increasing Ge cap thickness, reportedly for the first time, indicating that the carrier number fluctuation and correlated mobility fluctuation can be reduced when the carriers are away from interface.

2:00 PM

33.2 Processing and Characterization of Si/Ge Quantum Dots (Invited), *S. Miyazaki, K. Makihara, A. Ohta and M. Ikeda, Nagoya University*

We have demonstrated high density formation of Si quantum dots with Ge core on thermally-grown SiO_2 with control of highly-selective CVD. Through luminescence measurements, we have reported characteristic carrier confinement and recombination properties in the Ge core. Also, an impact of P delta-doping to the Ge core on the properties were shown.

2:25 PM

33.3 High Performance and Reliability Ge Channel CMOS with a MoS_2 Capping Layer, *J. Li, S. Xie, Z. Zheng, Y. Zhang, R. Zhang, M. Xu and Y. Zhao, Zhejiang University*

High performance Ge CMOS with quantum well- structured channels has been successfully realized using a single MoS_2 capping layer. Thanks to a large valence band offset (0.43 eV) and conduction band offset (0.5 eV) between the 2-layers-thick MoS_2 and the Ge substrate, both holes and electrons within the Ge p- and n-MOSFETs are confined into Ge channels and the scattering due to the traps in gate stack is suppressed effectively. As a result, the MoS_2/Ge p- and n- MOSFETs exhibit much improved hole and electron mobility, as well as the improved device reliability behaviors.

2:50 PM

33.4 Si-passivated Ge nMOS Gate Stack with Low D_{IT} and Dipole-induced Superior PBTI Reliability using 3D-compatible ALD Caps and High-pressure Anneal, *H. Arimura, D. Cott, R. Loo, W. Vanherle, Q. Xie*, F. Tang^, X. Jiang^, J. Franco, S. Sioncke, L.-Å Ragnarsson, E. Chiu**, X. Lu***, J. Geypen, H. Bender, J. Maes*, M. Givens, A. Sibaja-Hernandez, K. Wostyn, G. Boccardi, J. Mitard, N. Collaert and D. Mocuta, imec, *ASM Belgium, **Poongsan, ***Nanyang Technological University, ^ASM America*

We have demonstrated a 3D-compatible Si-passivated Ge nMOS gate stack solution with improved PBTI reliability and electron mobility. While ALD LaSiO insertion at HfO₂/SiO₂ interface improves PBTI reliability thanks to the dipole-induced band engineering, its combination with high-pressure anneal reduces D_{IT} to 5×10^{10} cm⁻²eV⁻¹ around midgap and improves mobility.

3:15 PM

33.5 High Performance Complementary Ge Peaking FinFETs by Room Temperature Neutral Beam Oxidation for Sub-7 nm Technology Node Applications, *Y.-J. Lee, T.-C. Hong*, F.-K. Hsueh, P.-J. Sung, C.-Y. Chen*, S.-S. Chuang*, T.-C. Cho*, S. Noda**, Y.-C. Tsou***, K.-H. Kao***, C.-T. Wu, T.-Y. Yu, Y.-L. Jian, C.-J. Su, Y.-M. Huang, W.-H. Huang, B.-Y. Chen, M.-C. Chen, K.-P. Huang^, J.-Y. Li^, M.-J. Chen^, Y. Li*, S. Samukawa**, W.-F. Wu, G.-W. Huang, J.-M. Shieh, T.-Y. Tseng*, T.-S. Chao*, Y.-H. Wang*** and W.-K. Yeh, National Nano Device Laboratories, *National Chiao Tung University, **Tohoku University, ***National Cheng Kung University, ^Industrial Technology Research Institute, ^National Taiwan University*

Ge peaking n- and p-FinFETs have been demonstrated by adopting neutral beam etching (NBE) and anisotropic neutral beam oxidation (NBO) processes. The irradiation-free NB processes not only suppress surface roughness but also guarantee low defect generation on the etched Ge surface. The fabricated Ge peaking FinFETs possess several unique features: (1) A peaking fin configuration with a 6-nm top-gate formed by an anisotropic NBO process at room temperature (RT). (2) Nearly defect-free three dimensional channel surfaces by NB processes. (3) ION and Gm improvement by NB processes as compared to that by conventional inductively coupled plasma (ICP) reactive ion etching. (4) Recorded high ION/IOFF ratio and low subthreshold swing (S.S. ~ 70 mV/dec) of Ge n- FinFETs. (5) Excellent immunity for short channel effect of Ge FinFETs.

3:40 PM

33.6 High Performance Ge Junctionless Gate-all-around NFETs with Simultaneous $I_{on} = 1235 \mu\text{A}/\mu\text{m}$ at $V_{OV} = V_{DS} = 1\text{V}$, $SS = 95 \text{ mV}/\text{dec}$, high $I_{on}/I_{off} = 2 \times 10^6$, and Reduced Noise Power Density using S/D Dopant Recovery by Selective Laser Annealing, *I.-H. Wong, F.-L. Lu, S.-H. Huang, H.-Y. Ye, C.-T. Lu*, J.-Y. Yan, Y.-C. Shen, Y.-J. Peng*, H.-S. Lan and C. W. Liu, National Taiwan University, *National Nan Device Laboratories*

The low channel doping concentrations of 1.2×10^{19} cm⁻³ to deplete the channel and the high S/D doping of 1.2×10^{20} cm⁻³ to reduce the S/D resistance are achieved simultaneously by selective laser annealing on epi-Ge on SOI. The device with W_{fin} down to 7 nm has $I_{on} = 1146$ mA/mm, $I_{on}/I_{off} = 2 \times 10^6$, and $SS = 95$ mV/dec. The I_{on} can be boost to 1235 mA/mm with tensile strain. The self-heating effect is responsible in part for high I_{on} , because the high device temperature can reduce the dominant impurity scattering. The lower low frequency noise is observed with junctionless gate-all-around FETs than planar inversion mode devices.

Session 34: Nano Device Technology - Devices Based on Quantum and Resistive Switching Phenomena

Wednesday, December 7, 1:30 p.m.

Continental Ballroom 5

Co-Chairs: Joachin Knoch, RWTH Aachen University

Wei Lu, University of Michigan

1:35 PM

34.1 Coupling MOS Quantum Dot and Phosphorous Donor Qubit Systems, *M. Rudolph, P. Harvey-Collard, R. Jock, T. Jacobson, J. Wendt, T. Pluym, J. Dominguez, G. Ten-Eyck, R. Manginell, M. Lilly and M. Carroll, Sandia National Labs*

Si-MOS based QD qubits are attractive due to their similarity to the current semiconductor industry. We introduce a highly tunable MOS foundry compatible qubit design that couples an electrostatic quantum dot (QD) with an implanted donor. We

show for the first time coherent two-axis control of a two-electron spin logical qubit that evolves under the QD-donor exchange interaction and the hyperfine interaction with the donor nucleus. The two interactions are tuned electrically with surface gate voltages to provide control of both qubit axes. Qubit decoherence is influenced by charge noise, which is of similar strength as epitaxial systems like GaAs and Si/SiGe.

2:00 PM

34.2 Quantum Information Processing in a Silicon-based System, *T.-Y. Yang, A. Andreev, Y. Yamaoka*, T. Ferrus, S. Oda*, T. Kadera*, D. Williams, Hitachi Europe Ltd., *Tokyo Institute of Technology*

For the first time, long coherence times up to tens of microseconds were observed in a silicon-based charge quantum bit (qubit) device at 4.2 K. The coherence times demonstrated in this paper are two orders of magnitude longer, and the operating temperature is two orders of magnitude higher than the reported semiconductor charge qubit systems. The first observation of the interaction between two sets of capacitively coupled charge movements was achieved by using our accurate charge detection technique.

2:25 PM

34.3 Experimental Demonstration of Nanomagnet Networks as Hardware for Ising Computing, *P. Debashis, R. Faria, K. Camsari, J. Appenzeller, S. Datta and Z. Chen, Purdue University*

This work explores nanomagnet networks as potential hardware for Ising computing, which is a field of much interest with applications in solving complex optimization problems, but lacks a natural hardware for implementation. We experimentally demonstrate that nanomagnets form natural stochastic elements, which when interconnected through configurable connections, mimic Ising networks.

2:50 PM

34.4 Functional Passive Material VO₂ for Analogue Signal Processing with High-Speed, Low Power, and Robust Performance, *T. Yajima, T. Nishimura and A. Toriumi, The University of Tokyo*

The voltage-induced metal-insulator transition in VO₂ was used for a two-terminal hysteretic voltage switch. The switch showed more than 10⁹ switching cycles and the arbitrary values of switching threshold and hysteresis. It enabled us to implement functionalities for analogue signal processing: (1) the noise canceling in analogue-digital conversion, (2) all-passive-element charge pumping, and (3) the two-terminal high-frequency limiter with excellent linearity.

3:15 PM

34.5 Low-Voltage Artificial Neuron using Feedback Engineered Insulator-to-Metal-Transition Devices, *J. Lin, A. Annadi, S. Sonde, C. Chen, L. Stan, K.V.L.V. Achari*, S. Ramanathan* and S. Guha, Argonne National Laboratory, *Purdue University*

We demonstrate a solid-state spiking artificial neuron based upon an insulator-to-metal (IMT) transition material element that operates at an unprecedented low voltage (0.8 V). We have developed a general coupled electrical-thermal device model for IMT based devices to accurately predict experimental outcomes. From the experiment and simulation, we show that voltage scalability to sub 0.3 V is possible by scaling of the IMT based neuron.

3:40 PM

34.6 Ag/HfO₂ based Threshold Switch with Extreme Non-Linearity for Unipolar Cross-Point Memory and Steep-slope Phase-FETs, *N. Shukla, B. Grisafe, R. K. Ghosh, N. Jao*, A. Aziz*, J. Frougier*, M. Jerry, S. Sonde**, S. Rouvimov, T. Orlova, S. K. Gupta*, S. Datta, University of Notre Dame, *The Pennsylvania State University, **University of Chicago*

In this work, we demonstrate (1) A novel Ag/HfO₂ based TS with ~10⁷ selectivity, I_{ON}=100μA, and I_{OFF}~10pA; (2) Feasibility of implementing the TS as a selector for PCM based cross-point memory; (3) A sub-kT/q (<3mV/dec over 5 orders of IDS) Phase-FET with >10x higher I_{ON}.

4:05 PM

34.7 Excellent Threshold Switching Device (I_{OFF} ~ 1 pA) with Atom-scale Metal Filament for Steep slope (< 5 mV/dec), Ultra Low Voltage (V_{DD} = 0.25 V) FET Applications, *S. Lim, J. Yoo, J. Song, J. Woo, J. Park and H. Hwang, Pohang University of Science and Technology (POSTECH)*

To realize a steep-slope-FET with low leakage current and low operating bias, we engineered two types of atom-switch devices and integrated them with a silicon MOSFET. The integrated atom-switch-FET exhibits extremely low leakage current (10^{-7} $\mu\text{A}/\mu\text{m}$), high ION/IOFF ratio ($> 10^7$), low operating bias (< 1 V) and sub-5 mV/dec subthreshold swing with abrupt transition range of 10^4 . Furthermore, through the comprehensive understanding on the steep-slope-transition phenomenon, control parameters of atom-switch devices such as ROFF and V_{th} , AS for optimal performances of atom-switch-FET were investigated at various operating bias conditions.

4:30 PM

34.8 2D h-BN Based RRAM Devices, *F. M. Puglisi, L. Larcher, C. Pan*, N. Xiao*, Y. Shi*, F. Hui*, M. Lanza*, Università di Modena e Reggio Emilia, *Soochow University*

This paper presents two dimensional (2D) RRAM devices exploiting multilayer hexagonal boron nitride (h-BN) as active switching layer. Different electrodes including Cu, Ni-doped Cu (CuNi) and graphene (G) are considered. The devices show low set/reset voltages, high on/off current ratio, good endurance and very low overall variability. Experimental results are interpreted using a novel simulation framework, which proves that the memory behavior is enabled by the manipulation of a boron (B)-deficient conductive filament (CF). The cyclical release and diffusion of B ions are the key physical mechanisms responsible for switching.

Session 35: Circuit Device Interaction - 3D Systems, Enabling Technologies and Characterizations

Wednesday, December 7, 1:30 p.m.

Continental Ballroom 6

Co-Chairs: Anne-Johan Annema, University of Twente

Susan Wu, Xilinx Inc.

1:35 PM

35.1 New Perspectives for Multicore Architectures using Advanced Technologies (Invited), *F. Clermidy, P. Vivet, D. Dutoit, Y. Thonnart, J.-L. Gonzales, J.-P. Noël, B. Giraud, A. Lévisse, O. Billoint and S. Thuriès, University Grenoble Alpes*

Impact of advanced technologies on the design and structure of multicore architectures is presented in this paper. More specifically, the power consumption and design complexity walls are examined leading to a "conquer-and-divide" strategy based on multicore partitioning and specialization. We then show how 3D stacking, Monolithic 3D integration and BEOL NVM can be associated to build new, simplified and power-efficient multicore.

2:00 PM

35.2 Ultra-Low-Resistance 3D InFO Inductors for Integrated Voltage Regulator Applications, *C.-L. Chen, Y.-C. Hsu, J.-S. Hsieh, C.-H. Tsai, V. Chang, A. Roth, E. Soenen, C.-T. Wang and D. Yu, Taiwan Semiconductor Manufacturing Company, Ltd.*

A novel 3D InFO inductor is developed to integrate with TSMC 16nm FinFET devices for high efficiency integrated voltage regulator. The InFO technology provides the ultra-low-resistance inductor (2.14 nH and 3.2 mOhm) and PDN (1.1 mOhm) concurrently for the IVR system design to achieve a peak power efficiency of 93%.

2:25 PM

35.3 High-Q Magnetic Inductors for High Efficiency On-Chip Power Conversion, *N. Wang, B. Doris, A. B. Shehata, E. O' Sullivan, S. Rosnagel, S. Brown, L. Gignac, J. Ott, M. Massouras, L. Romankiw and H. Deligianni, IBM T. J. Watson Research Center*

We experimentally demonstrate high performance magnetic inductors with Q as high as 17 in the frequency range of 50-250 MHz. These inductors meet target requirements for $>90\%$ efficient on-chip power converters. Physics-based models were used to understand magnetic losses, design novel magnetic stacks and innovative processes to achieve high Q.

2:50 PM

35.4 ESD Diodes in a Bulk Si Gate-All-Around Vertically Stacked Horizontal Nanowire Technology, *S.-H. Chen, G. Hellings, M. Scholz, D. Linten, H. Mertens, R. Ritzenthaler, R. Boschke*, G. Groeseneken* and N. Horiguchi, imec, *KU Leuven*

A Gate-All-Around (GAA) nanowire (NW) device is a candidate for sub-10nm bulk Si CMOS. The impact of the new architecture and its process options on intrinsic ESD performance needs to be studied. The measurement results and TCAD simulations prove that the ESD performance in bulk GAA NW based diodes is maintained in comparison to bulk FinFET diodes.

3:15 PM

35.5 Characterization of PVT Variation & Aging Induced Hold Time Margins of Flip-Flop Arrays at NTV in 22nm Tri-Gate CMOS, *C. Augustine, C. Tokunaga, A. Malavasi, A. Raychowdhury*, M. Khellah, J. Tschanz and V. De, Intel Corporation, *Georgia Institute of Technology*

With increasing process variation in scaled technology nodes, critical circuits are impacted which leads to performance loss/yield. We study min-delay in flip-flops in 22nm tri-gate CMOS and demonstrate through novel test-structures the impact of hold-time fluctuations across process/temperatures/voltage/aging conditions. This will guide design and process targets for min-delay failure mitigation.

3:40 PM

35.6 Thermal Resistance Modeling of Back-end Interconnect and Intrinsic FinFETs, and Transient Simulation of Inverters with Capacitive Loading Effects, *J.-Y. Yan, S.-R. Jan, Y.-J. Peng, H. H. Lin*, W. K. Wan*, Y.-H. Huang*, B. Hung*, K.-T. Chan*, M. Huang*, M.-T. Yang* and C. W. Liu, National Taiwan University, *MediaTek Inc.*

The intrinsic thermal resistances of 14nm FinFETs (Rth0, Device) are extracted with face-up and face-down configurations. Since the free convection of air has a large thermal resistance, the heat flow direction affects Rth0, Device. The volume of hot spot affects the cooling time. In an inverter, Tmax and the high temperature duration can be controlled by the current and output capacitive loading of the inverter. The residual temperature in the channel and the temperatures of M1 layer are found too low to reflect the real device temperature.

Session 36: Modeling and Simulation - Materials and Interfaces

Wednesday, December 7, 1:30 p.m.

Continental Ballroom 7-9

Co-Chairs: Chung-Cheng Wu, TSMC

Masumi Saitoh, Toshiba

1:35 PM

36.1 Surface Roughness Limited Mobility in multi-gate FETs with Arbitrary Cross-section, *O. Badami, D. Lizzit, R. Specogna and D. Esseni, University of Udine*

This paper presents the derivation, implementation and validation of a new model for Surface Roughness Scattering (SRS) in multi-gate FETs (MuGFETs) and gate-all-around nanowires (GAA-NW) FETs. The model employs a non linear relation between SRS matrix elements and interface fluctuations, that in planar MOSFETs allowed us to reconcile mobility simulations with experimental values for the r.m.s. interface roughness Δ_{rms} [Lizzit_JAP2014,Oves_TED2016]. The model is formulated for fairly arbitrary cross-sections and biasing conditions.

2:00 PM

36.2 Nitridation of GaN Surface for Power Device Application: A First-Principles Study, *Z. Zhang, B. Li, X. Tang, Q. Qian, M. Hua, B. Huang and K. J. Chen, The Hong Kong University of Science and Technology*

The effects of nitridation on GaN surface in the context of surface state distribution are investigated by first-principles calculation and XPS/UPS verification. The surface modification explains the significantly improved interface quality in GaN MIS-/MOS-structures featuring nitridation interfacial layer, and also provides evidence to support a physical model for the GaN band-edge emission in metal-AlGaIn/GaN Schottky heterojunction.

2:25 PM

36.3 Manipulating Spin Polarization and Carrier Mobility in Zigzag Graphene Ribbons using an Electric Field (Invited), *C. Delerue, J. Li* and Y.-M. Niquet*, IEMN-UMR CNRS, *Grenoble Alpes University*

We present atomistic calculations of the band structure and the phonon-limited carrier transport properties of zigzag graphene nanoribbons. We show that a lateral electric field can be used to tune the carrier mobility and mean free path over

orders of magnitude and to change the spin polarization of the current. These effects could be nicely exploited in electronic and spintronic devices.

2:50 PM

36.4 Density Functional Theory Simulations and Experimental Measurements of a-HfO₂/a-Si₃N₄/SiGe, a-HfO₂/SiO_{0.8}N_{0.8}/SiGe and a-HfO₂/a-SiO/SiGe Interfaces., *E. Chagarov, K. Sardashti, M. Edmonds, M. Clemons and A. Kummel, University of California, San Diego*

A comprehensive set of density functional theory (DFT) molecular dynamics (MD) simulations is presented for interfaces between a-HfO₂ high-K oxide and Si_{0.5}Ge_{0.5}(001) with several amorphous stoichiometric and sub-stoichiometric SiO_xN_y interlayers (a-SiO_{0.8}N_{0.8}, a-SiO_{0.4}N_{0.4}, a-Si₃N₂, a-Si₃N₄ and a-SiO) to determine their electrical passivation properties. In general the sub-stoichiometric interlayers had superior electrical properties because they minimized Ge-O and Ge-N bond formation and had low internal bond strain. The stack with oxygen deficient a-SiO interlayer demonstrated superior electric properties because it avoided all dangling bond formation. Experimental studies confirmed that a sub-stoichiometric SiON layer decreases the defects density of HfO₂(001)/Si_{0.5}Ge_{0.5}(001) MOCAPs.

3:15 PM

36.5 Insight into PBTI in InGaAs Nanowire FETs with Al₂O₃ and LaAlO₃ Gate Dielectrics, *Y. Li, S. Di, H. Jiang, P. Huang, Y. Wang, Z. Lun, L. Shen, L. Yin, X. Zhang, G. Du and X. Liu, Peking University*

The traps induced degradation of the Al₂O₃ and LaAlO₃ based InGaAs nanowire FETs are investigated by 3D KMC method considering trap coupling and trap generation. The measurement time constants of the defect in Al₂O₃ and PBTI can be well interpreted by consideration with metastable state. The power law of threshold shift can be greatly affected by the stress. Different from Al₂O₃ oxygen vacancies and interstitial Aluminum ions in LaAlO₃ have important roles in PBTI. Simulated results indicate that Al₂O₃ have better PBTI and recovery than that of LaAlO₃.

3:40 PM

36.6 Contact Resistivities in Gamma-valley Materials, *P. Solomon, IBM T.J Watson Research Center*

A model for contact resistivities of materials such as n-type III-V semiconductors with gamma-valley symmetry is developed which goes beyond current models in including non-parabolicity and screening effect of electrons on the Schottky barrier. These raise the contact resistivity, so that strategies involving negative barrier heights and interface velocity matching may be necessary to reach ITRS targets.

4:05 PM

36.7 TCAD-based Investigation on Transport Properties of Diamond-like Carbon Coatings for HV-ICs, *S. Reggiani, C. Giordano, A. Gnudi, E. Gnani, G. Bacarani, J. Dobrzynska*, J. Vobecky* and M. Bellini**, Università di Bologna, *ABB Semiconductors Ltd., **ABB Switzerland*

A TCAD-based approach is proposed to investigate the most relevant transport mechanisms of diamond-like carbon (DLC) films at different biases and ambient temperatures. Starting from the band structure and boundary conditions of a metal-insulator-metal (MIM) device, the most relevant trap levels have been determined against experiments along with the Poole-Frenkel conduction effect. The affinity of the DLC under study has been extracted from experiments on the corresponding metal-insulator-semiconductor (MIS) diode. A clear polarization effect has been found in the measured C-V curves at different frequencies. The latter has been modeled in the TCAD tool via the Debye equation leading to a nice agreement with experiments.



Seated from left to right: Martin Giles, Publicity Chair, Stefan De Gendt, Technical Program Chair, Patrick Fay, General Chair, Ken Rim, Technical Program Vice Chair, Mariko Takayanagi, Publications Chair

Second row standing from left to right: Dina Triyoso, Tutorial Chair, Suman Datta, Short Course Vice Chair, Tian-ling Ren, Asian Arrangements Chair, Jan Hoentschel, Circuit and Device Interaction Chair, Ryoichi Ishihara, Optoelectronics, Displays, and Imagers Chair, Shyh-Horng Yang, Focus Session Chair, Merlyne De Souza, European Arrangements Chair, Suman Banerjee, Modeling and Simulation Chair, Barbara De Salvo, Publicity Vice Chair, Debbie Senesky, Sensors, MEMS, and BioMEMS Chair

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