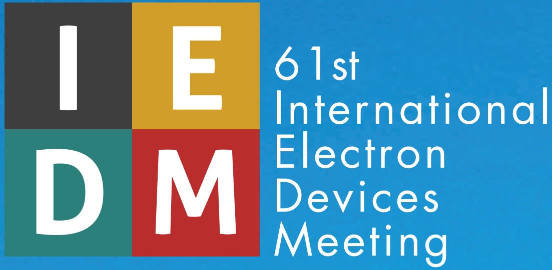

2015 IEDM Conference Proceedings

For More Information
IEDM Online: ieee-iedm.org

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Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

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Topics of Interest

CIRCUIT AND DEVICE INTERACTION (CDI)

Papers are solicited in the areas of CMOS platform technology and circuit-device interactions. Topics include digital, analog and RF technology, device and circuit scaling issues, technology-circuit co-optimization, power-performance-area analysis, impact of future device structures on circuit design, circuit and architecture implication of interconnects, and manufacturability issues such as DFM and process control. Submission of papers covering device and design interactions in memory, logic, analog, and mixed-signal circuit issues such as technology variability, power constraints, physical layout effects and design complexity in memory, logic, analog, and mixed-signal circuits is encouraged.

CHARACTERIZATION, RELIABILITY and YIELD (CRY)

Papers are solicited in all areas of characterization, yield and reliability, both front-end and back-end of the process. Topics include but are not limited to hot carriers, high-k and low-k dielectric wear-out and breakdown, process charging damage, latch-up, ESD, soft errors, noise and mismatch behavior, variability/reliability interaction and time-dependent variability, bias temperature instabilities, and thermal modeling at the device, circuit, and packaging level. Other topics include interconnect reliability, electromigration, the impact of back-end processing on devices, chip- package interaction, physics of failure analysis, as well as reliability issues for memory, logic, and 3D technologies and novel characterization techniques.

DISPLAY and IMAGING SYSTEMS (DIS)

Papers are solicited on devices, structures, and integration for displays, imaging systems, and detectors. A subset of key topics in the displays and imaging area includes CMOS imagers, high-speed imagers, optoelectronic devices, CCDs, TFTs, organic, amorphous, and polycrystalline devices, optoelectronic devices, as well as emissive and reflective displays. Submission of papers addressing fundamental performance differences between CMOS and CCD imagers, organic and inorganic displays, and covering new technology trends in imagers and displays are encouraged. Other relevant subjects include DIS design, fabrication, reliability, theory, and modeling.

MEMORY TECHNOLOGY (MT)

Papers are solicited covering all memory related technology topics, from novel memory cell concepts and integration schemes to fully integrated memories and manufacturing issues. Areas of interest include processes, reliability and modeling for volatile and nonvolatile memories, as well as novel memory cells including but not limited to ReRAM, STT-MRAM, PCRAM, cross-point, cross–point selectors, organic memory and NEMS-based devices. Other topics of interest are memory array optimization, 3D memory architectures, novel read/program/erase schemes, solid state drive (SSD) applications, and non-volatile memory enabled emerging logic applications.

MODELING and SIMULATION (MS)

Papers are solicited in the areas of analytical, numerical, and statistical approaches to modeling electronic, optical, and hybrid devices, and their isolation and interconnection. Topics include physical and compact models for devices and interconnects, modeling of fabrication processes and equipment, material modeling, process characterization, parameter extraction, early compact models for advanced technologies, performance evaluation, design for manufacturing, reliability, variability, and technology benchmarking methodologies. Other topics of interest include the modeling of interactions between process, device, and circuit technology. Submissions should advance the art of modeling and simulation or apply existing techniques to gain new insights into devices.

NANO DEVICE TECHNOLOGY (NDT)

Papers are solicited on novel solid state and nanoelectronic devices and concepts. This includes devices based on novel transport mechanisms such as tunnel FETs; molecular devices, and emerging concepts for devices based on topological insulators, phase transitions and non-von Neumann devices. Non-charge based logic, magnetic logic, spintronics, silicon photonics, plasmonics are also of interest. Furthermore, nanoelectronic devices based on low-dimensional systems are encouraged, including 2D materials, nanowires, nanotubes and quantum dots. Subsets of key topics include electron device physics, CMOS scaling issues, novel transistor structures, as well as devices with high-mobility channels such as strained silicon, germanium, SiGe, and GeSn.

POWER AND COMPOUND SEMICONDUCTOR DEVICES (PC)

Papers are solicited in the areas of compound semiconductors (GaAs, InP, GaN, SiC, Antimonides and their related alloys, etc.) for electronic and optoelectronic device applications. Papers are also solicited on discrete and integrated power devices and modules using Si, diamond, and compound semiconductors. Topics include III-V FETs, tunnel FETs, HBTs, superjunction devices, IGBTs, vacuum devices, LEDs, lasers, external modulators, RF, microwave and millimeter-wave devices, and SAW/

BAW devices. Also of interest are ballistic and quantum effect devices, optoelectronic integrated circuits, optical interconnects, photovoltaics, photonic bandgap structures and crystals, and active and passive electron devices for analog applications.

PROCESS and MANUFACTURING TECHNOLOGY (PMT)

Papers are requested on front-end, back-end, heterogeneous technology integration and packaging process modules for fabrication of logic, memory, and 3D integrated circuits on silicon and non-silicon technologies as well as advanced semiconductor manufacturing topics. Topics related to front-end processing include substrate technologies, new transistor materials and integration of alternative high mobility channel materials, lithography, etching, self-assembly techniques, isolation technologies, dielectric materials and metal electrodes for transistor gate stacks and MIM capacitors, shallow junctions, and silicides. Topics related to back-end processing include conductor systems, low dielectric constant materials, contact, via processes, barrier materials, planarization, integration considerations for multilevel interconnects, photonics-electronics integration on CMOS and advanced packaging. Advanced semiconductor manufacturing topics includes novel/emerging process technology, processes and tools designed to reduce variance, defect reduction in heterogeneous material systems, novel techniques around process understanding and stability as well as process control techniques for advanced CMOS, wide band-gap semiconductors and MEMS.

SENSORS, MEMS, and BioMEMS (SMB)

Papers are solicited in the area of sensors, sensor networks, micro electromechanical systems (MEMS), BioMEMS as well as NEMS-based logic devices. The sensors area includes, but is not limited to, ? TFT-based sensors, and sensors for chemical, molecular and biological detection including integrated biomedical sensing. Topics of interest in the MEMS and BioMEMS area include resonators and resonant sensors, RF MEMS, integrated inertial measurement units, integrated sensors and actuators, micro-optical devices, micro-fluidic, and bio-electronic devices inspired or enabled by biomimetic structures, micro power generators, energy harvesting devices and photovoltaics, optofluidic devices, and organic-inorganic hybrid-devices, with particular emphasis on new device concepts, integrated implementations and complete sensor systems and networks.

Program

See the Program Download for all abstracts and speaker bios.

Tutorials

The tutorials are in their fifth year and are 90 minute stand alone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields, and facilitate understanding of the technical sessions. In contrast, the traditional short courses are intensive full-day events focused on a single technical topic.

The tutorial sessions will take place on Saturday, December 5th. Three tutorials are given in parallel in two time slots, at 2:45 p.m.and 4:30 p.m. respectively.

Topics presented at 2:45 – 4:15 p.m.

1. Electronic Control Systems for Quantum Computation, David DiVincenzo, Aachen University
2. Advanced CMOS Device Physics for 7nm and Beyond, Scott Thompson, University of Florida
3. Thin Film Transistors for Displays and More, Tom Jackson, Penn State University

Topics presented at 4:30 p.m.-6:00 p.m.

1. Nanoscale III-V Compound Semiconductor MOSFETs for Logic, Luca Selmi, University of Udine
2. RF and Analog Device Technologies, Anthony Chou, GlobalFoundries
3. Implantable MEMS and Microsystems for Neural Interface, Eusik Yoon, University of Michigan

Short Courses

Below are the titles of the two IEDM Short Courses that will be held on December 6, 2015.

Emerging CMOS Technology at 5nm and Beyond

Course Organizer: Yuan Taur, University of California, San Diego

Memory Technologies for Future Systems

Course Organizer: Dick Wouters, RWTH Aachen University

Short Course 1 Emerging CMOS Technology at 5nm and Beyond

- 8:30 a.m. :: Introduction and Overview :: Yuan Taur, University of California, San Diego

- 8:45 a.m. :: Device Options and Tradeoffs :: Mark Lundstrom, Xingshu Sun, Purdue University, Dimitri Antoniadis, MIT, Shaloo Rakheja, New York University
- 10:15 a.m. :: Process Integration Challenges :: Bruce Doris, IBM Corporation
- 11:15 a.m. :: BEOL Process Challenges :: Takeshi Nogami, IBM Corporation
- 1:30 p.m. :: Emerging Interconnect Technologies :: Krishna Saraswat, Stanford University
- 2:30 p.m. :: Advanced Lithography :: Anthony Yen, TSMC
- 4:00 p.m. :: Variability and design for manufacturability :: Asen Asenov, Glasgow University, and Gold Standard Simulations Ltd.
- 5:15p.m. :: Conclusion

Short Course 2 Memory Technologies for Future Systems

- 9:15 a.m. :: Introduction and Overview :: Dirk Wouters, RWTH Aachen University
- 9:30 a.m. :: System Requirements for Memories :: Rob Aitken, ARM Research
- 11:00 a.m. :: Conventional Memory Technologies : DRAM :: Changyeol Lee, SK Hynix
- 1:30 p.m. :: Conventional Memory Technologies: Flash memory :: Youngwoo Park, Samsung Electronics
- 2:45 p.m. :: Emerging Memory Technologies : ReRAM and PCM :: Daniel Ielmini, Politecnico di Milano
- 4:15 p.m. :: Emerging Memory Technologies : STT-MRAM :: Thibaut Devolder, CNRS Research Associate, Univertsite Paris-Sud
- 5:30 p.m. :: Conclusion

Plenary Session

Welcome and Awards General Chair

John S. Suehle, NIST

Invited Papers

Technical Program Chair: Patrick Fay, University of Notre Dame

1.1 Moore's Law at 50: Are we planning For retirement?, Greg Yeric, ARM

1.2 Quantum Computing in Si, Michelle Simmons, University of New South Wales

1.3 Silicon for Prevention, Cure and Care: A Technology Toolbox of Wearables at the Dawn of a New Health System, Chris Van Hoof, Imec

Roger A. Haken Best Student Paper

The 2014 Roger A. Haken Best Student Paper Award will be presented on Monday, December 7, at the Plenary Session, to Jianqiang Lin of the Massachusetts Institute of Technology, for the paper entitled, "Novel Intrinsic and Extrinsic Engineering for High-Performance High-Density Self-Aligned InGaAs MOSFETs: Precise Channel Thickness Control and Sub-40-nm Metal Contacts".

One paper presented by a student at the 2015 IEDM will be selected for the 2015 Best Student Paper Award. To be eligible, the paper must be based on the student's own work and have been identified as a student paper at the time of submission. Presentation of the award will be made at the 2016 IEDM.

Focus Sessions

In 2015 there is an increased emphasis on neural-inspired architectures, 2D materials and applications, power devices and reliability, flexible electronics and applications, and silicon-based nano-devices for detection of biomolecules.

Special Focus Sessions:

- Beyond von Neumann Computing
- Layered 2D Materials and Devices: From Growth to Applications
- Advances in Wide Bandgap Power Devices
- Flexible hybrid electronics
- Silicon-based Nano-devices for Detection of Biomolecules and Cell Function

Technical Program

See the Program Download for all abstracts and speaker bios.

Monday — 9am - Noon

- Session 1 — Plenary Session

Monday - 1:30pm - 5:00pm

- Session 2: Nano Device Technology — Ge and Other Group IV Devices
- Session 3: Memory Technology — PCRAM and Flash
- Session 4: Circuit Device Interaction — Focus Session – Beyond von Neumann Computing
- Session 5: Modeling and Simulation — Physical Modeling for Advanced Devices, Power Devices, and Memories
- Session 6: Display and Imaging Systems — Integrated Thin Film Transistors
- Session 7: Characterization, Reliability and Yield — Reliability and Characterization of Resistive RAM and BEOL Processes
- Session 8: Process and Manufacturing Technology — 3D Integration and BEOL
- Session 9: Power and Compound Semiconductor Devices — Advanced Compound RF and Power Devices

Monday 6:30 pm – 8:00 pm

- International Ballroom Center — RECEPTION

Tuesday - 9:00 am - 12:00 pm

- Session 10: Memory Technology — RRAM
- Session 11: Circuit Device Interaction — CMOS Scaling and Circuit/Device Variability
- Session 12: Modeling and Simulation — Modeling of 2D and Organic Semiconductor Devices
- Session 13: Sensors, MEMS, and BioMEMS — Focus Session – Silicon-based Nano-devices for Detection of Biomolecules and Cell Function
- Session 14: Characterization, Reliability and Yield — Flash and Novel Device Characterization and Reliability
- Session 15: Process and Manufacturing Technology — Moore and More

Tuesday - 12:20 PM

- International Ballroom West — IEDM General Luncheon

Tuesday - 2:15 pm - 5:30 pm

- Session 16: Power and Compound Semiconductor Devices — Focus Session – Advances in Wide Bandgap Power Devices
- Session 17: Circuit Device Interaction — Neuromorphic Computing Techniques
- Session 18: Sensors, MEMS, nd BioMEMS — M/NEMS Resonators, Sensors and Actuators
- Session 19: Display and Imaging Systems — Focus Session – Flexible Hybrid Electronics
- Session 20: Characterization, Reliability and Yield — Transistors Ageing, Variability and the Impact on Circuit Design
- Session 21: Process and Manufacturing Technology — Advanced Modules and FinFET Devices
- Session 22: Nano Device Technology — Steep Slope Transistors

Tuesday - 8:00 pm - 10:00 pm

- Continental Ballroom 4-5-6 — 23 / 24 IEDM Evening Panel Session

Wednesday - 9:00 am - 12:00 pm

- Session 25: Circuit Device Interaction — More than Moore – Value Added Technologies
- Session 26: Memory Technology — MRAM, DRAM, and SRAM
- Session 27: Nano Device Technology — Focus Session – Layered 2D Materials and Devices: From Growth to Applications
- Session 28: Modeling and Simulation — Compact Modeling
- Session 29: Sensors, MEMS, and BioMEMS — Devices for In Vitro Bioanalytics and In Vivo Monitoring
- Session 30: Display and Imaging Systems — Advanced Imagers and Photodetectors

- Session 31: Power and Compound Semiconductor Devices — III-V: FETs, Photonics, Si Integration

Wednesday - 12:30 p.m.

- Jefferson Room — Entrepreneurs Lunch at IEDM

Wednesday - 1:30 pm - 5:30 pm

- Session 32: Nano Device Technology — Beyond CMOS Technologies
- Session 33: Sensors, MEMS, and BioMEMS — Emerging Nanodevices and Nanoarrays
- Session 34: Modeling and Simulation — Modeling of III-V and Ge Materials and Alternative CMOS Device Architecture
- Session 35: Power and Compound Semiconductor Devices — GaN Material and Device Interactions

IEDM Luncheon

Working backwards from the Customer to Physics of Failure in Consumer Electronics Reliability

Pat Tang, VP of Product Integrity, Amazon Lab126

Evening Panel Discussion

Evening Panel: Is there a potential for a revolution in on-chip interconnect?

Moderator: Paul Franzon, North Carolina State University

Candidates:

- The incumbent: Rod Augur, GlobalFoundries
- We can design around it: John Wilson, nVidia
- Nano/novel materials or devices to the rescue: Azad Naeemi, Georgia Tech
- Active Interconnect: Toshi Sakamoto, NEC
- Monotlithic 3D: Maude Vinot, CEA
- Multilithic 3D: Paul Enquist, Ziptronix

Evening Panel: Emerging Devices – Will they solve the bottlenecks of CMOS?

Moderator: Heike Riel, IBM Research

Panelists:

- Supriyo Bandyopadhya, Virginia Commonwealth University
- Wilfried Haensch, IBM Research
- Adrian Ionescu, EPFL
- Carlo Reita, CEA-LETI
- Sayeef Salahudin, UC Berkeley
- Frank Schwierz, Technical University of Illmenau

Entrepreneurs Luncheon

Abbie Gregg – President, Abbie Gregg, Inc. (AGI)

AGI was founded in 1985 and has extensive experience in nanotechnology, biotechnology, photovoltaic, wafer fab, assembly, multichip module, disc drive, flat panel display and flexible electronics start-up planning, process engineering and operations. AGI has gained global industry recognition for the depth of excellence our services provide. To date AGI has completed over 800 projects on 5 continents.

Appendix - Abstracts, Bios & Technical Program

WELCOME FROM THE GENERAL CHAIR

John Suehle
General Chair

On behalf of the IEDM Executive Committee, I would like to welcome you to the 2015 IEEE International Electron Devices Meeting to be held December 7-9, 2015 in Washington DC. On the 50th anniversary of Gordon Moore's publication of his renowned scaling law for microelectronics, the 61st annual IEDM continues to be the world's premier venue for presenting the latest breakthroughs in electron device technologies.

Patrick Fay
Technical
Program Chair

Stefan De Gendt
Technical Program
Vice Chair

The IEDM's outstanding technical sessions consisting both contributed and invited papers that will be presented by industrial, academic leaders and students from around the world. Short summaries of all the papers are available on the IEDM web site, which we encourage everyone to visit – http://www.ieee-iedm.org/. We will continue to distribute an abbreviated digest at the meeting, along with electronic versions of the complete abstracts. We are also providing an official IEDM smartphone and tablet application that supports iPhone, iPad and Android platforms to help our attendees navigate the conference. The full digest will be available on the IEEE Xplore website and the DVD package offered by the IEEE Electron Devices Society after the conference.

The meeting's technical activities begin on Saturday afternoon, December 5, when we will continue to offer our highly successful short tutorials that were introduced in 2011. These tutorials are directed to students, engineers, or anyone who wants a review of the basics of key electron device technologies. Three tracks run in parallel, for a total of six tutorial topics. On Sunday two comprehensive short courses will be offered: "Emerging CMOS Technology at 5nm and beyond", and "Memory Technologies for Future Systems". These courses are organized and presented by internationally recognized researchers active in their respective areas of technology. The topics and instructors have been carefully chosen to have broad appeal to IEDM participants, and will include material suitable for both newcomers as well as experts in the field.

The Plenary Session on Monday morning will feature three invited talks: Dr. Greg Yeric from ARM will give a thought-provoking talk titled "Moore's Law at 50: Are we planning for retirement?". followed by Prof. Michelle Simmons of the University of New South Wales, who will discuss a new type of computer that exploits the laws of physics at very small dimensions in her talk "Atomic-Scale Electronics for Quantum Computing". The final talk titled "Silicon for Prevention, Cure, and Care: A Technology Toolbox of Wearables at the Dawn of a New Health System" given by Dr. Christopher Van Hoof of IMEC will discuss how wearable electronic systems hold the grand promise of revolutionizing health care.

In addition to the excellent contributed paper sessions, five special "Focus Sessions" will once again feature talks from leading experts in exciting new areas. The topics of the invited sessions include neural inspired architectures, 2D layered materials and applications, power devices and their reliability on non-native substrates, flexible hybrid electronics, and silicon-based nano-devices for detection of biomolecules and cell functions.

On Tuesday night, we will feature two interactive panel sessions that promise to be intellectually stimulating and engaging. The first panel: "Is there a potential for a revolution in on-chip interconnect?" will be moderated by Paul Franzon of NCSU. Heike Riel of IBM will moderate the second panel: "Emerging Devices: Do they address the real issues?".

IEDM will feature two informative and entertaining luncheons on Tuesday and Wednesday. We are very fortunate to have Dr Patrick Tang, Vice President of Product Integrity at Amazon as our speaker for the Tuesday Luncheon. Dr. Tang is responsible for the architectural integrity and product reliability of Amazon's Kindle Fire tablets, e-readers, Fire TV and Fire Phone products. Our highly successful Entrepreneurs Lunch Series held on Wednesday will feature Abbie Gregg, President of AGI Inc. She will share her thoughts and experience in building and running a highly successful company that has gained global industry recognition and has completed over 800 projects on 5 continents.

I am also pleased to announce IEDM's first Special Issue published in the IEEE Transactions on Electron Devices. The Special Issue features 11 manuscript based on work presented at the 2014 IEDM held in San Francisco, CA. It is our hope that this Special Issue helps to pave a permanent pathway between the work featured at IEDM and EDS sponsored archival journals.

On behalf of Patrick Fay, Technical Program Chair, and Stefan DeGendt, Technical Program Vice-Chair, I want to express my sincere appreciation to all of the authors and speakers who contributed to the technical program and to each of the members of the IEDM Executive and technical Subcommittees whose dedication and tireless efforts were key in planning and organizing the 2015 conference.

The IEDM is sponsored by the IEEE Electron Devices Society. If you are not already an IEEE member, please consider joining this great institution which has played such an important role globally for over 120 years. More detailed information regarding the IEEE is available at the conference and on their website – http://www.ieee.org.

It is again my great honor and pleasure to extend a warm welcome to everyone attending the 2015 IEEE International Electron Devices Meeting, and helping to celebrate our 61st year.

John S. Suehle
General Chair

AWARD PRESENTATIONS

PLENARY SESSION

Monday, December 7

2014 Roger A. Haken Best Student Paper Award

To: Jianqiang Lin, Massachusetts Institute of Technology

For the paper entitled: "Novel Intrinsic and Extrinsic Engineering for High-Performance High-Density Self-Aligned InGaAs MOSFETs: Precise Channel Thickness Control and Sub-40-nm Metal Contacts"

EDS Paul Rappaport Award

To: Sylvain Barraud, Jean-Michael Hartmann, Virginie Maffini-Alvaro, Vincent Delaye, Lucie Tosti, Dominique Lafond
For the paper entitled: "Top-Down Fabrication of Epitaxial SiGe/Si Multi-(Core/Shell) p-FET Nanowire Transistors"

EDS George E. Smith Award

To: Winston Chern, Pouya Hashemi, James T. Teherani, Dimitri A. Antoniadis, Judy L. Hoyt

For the paper entitled: "Record Hole Mobility at High Vertical Fields in Planar Strained Germanium on Insulator with Asymmetric Strain"

2015 EDS Education Award

To: Roger T. Howe

"For contributions to mentoring and education in the fields of microelectromechanical systems and nanotechnology"

2015 EDS J.J. Ebers Award

To: Yuan-Chen Sun

"For sustained leadership and technical contributions to energy efficient foundry CMOS technologies"

EDS Celebrated Members Award

To: B. Jayant Baliga and Robert H. Dennard

"For fundamental contributions to the field of electron devices for the benefit of humanity"

2015 IEEE/EDS Fellows

**This is a complete listing of the 2015 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2015 IEDM.*

- David Abe, U.S. Naval Research Laboratory, Washington, DC, USA
- Christopher Auth, Intel Corporation, Hillsboro, OR, USA
- Victor Bright, University of Colorado, Boulder, CO, USA
- Martin Buehler, Decagon Devices, Pullman, WA, USA
- John Conley, Oregon State University, Corvallis, OR, USA
- John Dallesasse, University of Illinois at Urbana-Champaign, Urbana, IL, USA
- Weileun Fang, National Tsing Hua University, Hsinchu, Taiwan
- Lorenzo Faraone, University of Western Australia, Crawley, WA, Australia
- Reza Ghodssi, University of Maryland, College Park, College Park, MD, USA
- Deepnarayan Gupta, Hypres Inc., Elmsford, NY, USA
- Ray-Hua Horng, National Chung Hsing University, Taichung, Taiwan
- Giuseppe Iannaccone, University of Pisa, Italy, Pisa, Italy
- Meikei Ieong, TSMC Europe B.V., Amsterdam, Netherlands
- Safa Kasap, University of Saskatchewan, Saskatoon, SK, Canada
- Tsunenobu Kimoto, Kyoto University, Kyoto, Japan
- Hiroshi Kondoh, Centellax, Inc., Santa Rosa, CA, USA
- Paul Lee, Exelis Geospatial Systems, Amityville, NY, USA
- Yong Liu, Fairchild Semiconductor Corp., South Portland, ME, USA
- Susan Lord, University of San Diego, San Diego, CA, USA
- Roger Malik, First Solar, Santa Clara, CA, USA
- Wiltold (Witek) Maszara, Global Foundries, Santa Clara, CA, USA
- Sokrates Pantelides, Vanderbilt University, Nashville, TN, USA
- Luca Selmi, University of Udine, Udine, Italy
- Paul Tasker, Cardfiff University, UK, Cardiff, Wales, UK
- Jian-Ping Wang, University of Minnesota, Minneapolis, MN, USA
- Mark Weichold, Texas A&M University at Qatar, Doha, Qatar
- Chik Patrick Yue, Hong Kong University of Science & Tech., Clear Water Bay, Hong Kong
- Yong-Hang Zhang, Arizona State University, Tempe, AZ, USA

IEDM LUNCHEON

Tuesday, December 8

2015 IEEE Cledo Brunetti Award

To: Hiroshi Iwai

"For contributions to scaling of CMOS devices."

2015 IEEE Kiyo Tomiyasu

To: Vivek Subramanian and Kaustav Banerjee

"For contributions to nano-materials, devices, circuits and CAD, enabling low-power and low-cost electronics."

LUNCHEON PRESENTATION

"Working Backwards from the Customer to Physics of Failure in Consumer Electronics Reliability"

Pat Tang, VP of Product Integrity, Amazon Lab126

Every consumer electronics device we buy can be considered a bundle of competing failure mechanisms that have each taken years of research to properly risk assess. The reality in consumer electronics is that there are many more unknowns from complex system interactions and we are not afforded years of risk assessment in this highly competitive market. Product Development from concept to market in less than a year is becoming the norm. The appetite for increasing functionality in smaller and lighter devices is insatiable. We are now expecting access to cloud computing in the palm of our hands that can respond to your voice, touch gesture and your very location. What is the correct approach in ensuring reliability for a system that can fail with an unknown multitude of permutations but where engineering cost and schedule are finite?

This talk will examine a product integrity vision based on 3 technical strategies:

1. Working backwards from the customer to physics of failure
2. Design for reliability through simulation tools;
3. Development of customer-use centric standards using stress-strength analysis.

Reliability is rather opaque in the consumer electronics that we buy. This presentation aims to open the path towards a consumer electronics standard to offer integrity and transparency to the customer so that they know what they are getting.

Biography

Pat Tang joined Amazon in 2010 to lead Product Integrity and is responsible for the architectural integrity and product reliability of Amazon's Kindle Fire tablets, e-readers, Fire TV and Fire Phone products. He built teams of architectural simulation and materials testing, product reliability qualification and database field analysis for warranty cost. By using cloud-based simulation to aid design, thin, lightweight and reliable products like Kindle Fire HDX 8.9 and Kindle Paperwhite were realized.

Pat was previously at Apple where he was the reliability manager responsible for the qualification of Mac products: Macbook Pro, Macbook Air, iMac, MacPro, AppleTV and the first prototypes of iPad. Here he introduced large-scale reliability waterfalls to combine different stresses to replicate field use.

With interests in Physics and design Pat has also: designed the sensor pattern in Apple's Magic trackpad; designed and patented a semiconductor sensor for green house gases; designed power amplifier probes to perform RF measurements at wafer level; conducted theoretical and empirical research of semiconductor quantum wells for opto-electronics. Patrick holds a PhD degree in Physics from Imperial College UK and has over 30 publications.

Entrepreneurs Lunch at IEDM 2015!

Sponsored by IEDM and EDS Women in Engineering

Speaker: Abbie Gregg, Abbie Gregg, Inc. (AGI)

Wednesday, December 9
12:30 pm - 1:30 pm.

AGI was founded in 1985 and has extensive experience in nanotechnology, biotechnology, photovoltaic, wafer fab, assembly, multichip module, disc drive, flat panel display and flexible electronics start-up planning, process engineering and operations. AGI has gained global industry recognition for the depth of excellence our services provide. To date AGI has completed over 800 projects on 5 continents.

Bio: Abbie Gregg started Abbie Gregg, Inc. in September 1985 and just celebrated the company's 30th anniversary, a remarkable milestone in the company's history!

Abbie Gregg is an industry expert and cleanroom consultant with many years of experience in engineering consulting specializing in microelectronics process analysis and the design, startup and operations of clean laboratories and manufacturing facilities. Her interests and skills are comprised of process engineering and analysis, facility layout and design, site selection and strategic planning, yield enhancement, quality assurance, manufacturing operations management, equipment selection and qualification, factory/product cost modeling, and nanotechnology.

As President of AGI, she has completed over 826 projects worldwide, spanning five continents for industrial, government, and university clients. These projects have included Nanotechnology, Wafer Fab, MEMS, Flexible Electronics, Imaging, Photovoltaics, Disc Drive, Bio/Pharma, and FPD Projects.

Abbie has also developed a database and software system for computer aided layout, utility load analysis, and design of cleanrooms, advanced laboratories and characterization/imaging areas. She has done extensive turn-around consulting, assisting technical operations with project management, and implementing continuous improvement methods.

Abbie holds a Bachelor of Science in Metallurgy and Material Science and Engineering from Massachusetts Institute of Technology, and studied Electrical Engineering at the University of Maine.

TUTORIALS

Saturday, December 5, 2015
2:45 p.m. – 6:00 p.m.

Topics Presented at 2:45 – 4:15 p.m.
Lincoln West // Lincoln East // Monroe

Electronic Control Systems for Quantum Computation
David DiVincenzo
Aachen University

We have known for twenty years that quantum computers would have unique powers for solving certain classes of computational problems. Throughout these twenty years, workers have striven to identify a physical setting in which high-quality qubits can be created and employed in a quantum computing system. Very promising devices have been identified in several different areas of low-temperature electronics, namely in superconductor and in single-electron semiconductor structures (e.g., quantum dots). Rudimentary efforts at scale-up are presently reported; even for modules of 10 qubits, the complexity of the classical electronic control system becomes one of the main barriers to further progress.

The specifications of this control system are now well defined, and are daunting. It must deliver very low noise, precisely shaped pulses in the GHz band for qubit gate control; it must deliver interrogating microwave pulses that sense the qubit state, which must be amplified at the quantum-limited level and delivered quickly back to the control system; because of the nature of the fine-grained error correction needed for reliable quantum algorithm operation, subsequent control pulses must be determined by a rapid (classical) calculation performed using the measurement outcomes as inputs. All this must be done for a very large number of channels (about one per qubit) with rigorous control of timings and crosstalk.

This tutorial will discuss the current state of experiments, and explain the efforts underway to understand and achieve this control system.

Outline

- The nature of quantum algorithms
- What is a qubit
- Criteria for the physical implementation of a quantum computer
- Fault tolerance, and the noise threshold theorem
- Strategies for 2D layouts for qubits
- Measurement, Isolation, Amplification
- The full system view

Advanced CMOS Device Physics for 7nm and Beyond

Scott Thompson
University of Florida

The industry march along Moore's Law continues and new semiconductor nodes at 7 and beyond will certainly happen. However, many device, material, and economical challenges remain. This tutorial will target understanding key device concepts for 7nm node and beyond.

The tutorial will start with a brief review of state of the art for logic technologies followed by the likely metrics the industry will use to guide the 7nm and beyond device and material options. The next section of the talk will give a tutorial on many of the key device concepts that will shape the value proposition of 7nm and beyond.

Outline

1. Introduction to state-of-the- art for logic devices
2. Metrics for logic device going forward
3. Deeper look at some advanced device concepts
    - Transistor variation/ random doping effect
    - Strain Si, Ge and III-V channels
    - Quantum confinement
    - Drive Current and relation to mobility, velocity saturation, and density of states
    - External resistance
    - Sub fin doping and gate all around devices
4. Conclusion: How does the roadmap evolve?

Thin Film Transistors for Displays and More

Tom Jackson
Penn State University

Thin film transistors (TFTs) provide the electronic backplane for a ~$2 x 1011 active matrix display business and are poised for new applications in flexible electronics, health monitoring, sensor arrays, and more. Commercial applications are currently dominated by hydrogenated amorphous silicon (a-SiH) TFTs. Traps dominate transport in a-Si:H resulting in a field-effect ~1000 times lower than single crystal Si, but the ability to fabricate devices over large areas (~10 m2 or more) at low temperature and low cost is a critical advantage. Organic semiconductors may enable even lower cost manufacturing, but device performance, reproducibility, and stability are all major challenges. Oxide semiconductors have demonstrated improved performance and/or reduced temperature manufacturing. Oxide semiconductors are beginning to make inroads in active matrix display manufacturing and provide a path toward flexible electronics for more than just displays.

Outline

1. Introduction to thin film transistors (TFTs)
    - Similarities and differences compared to bulk silicon MOSFETs

2. Traps in thin film semiconductors
3. Amorphous silicon TFTs
4. Organic TFTs
5. Oxide TFTs
6. TFTs for flexible substrate electronics

Topics Presented at 4:30 – 6:00 p.m.

Lincoln West // Lincoln East // Monroe

Nanoscale III-V Compound Semiconductor MOSFETs for Logic

Luca Selmi
University of Udine

The replacement of silicon with alternative channel materials is only the last but perhaps the most challenging in the series of innovations introduced to sustain the progress of CMOS technology beyond the 65 nm node, and toward its ultimate limits. III-V compound semiconductors such as InxGa(1-x)As or GaSb entered this evolving scenario by offering higher mobility and injection velocity than strained Silicon, which makes them good candidates to achieve higher MOSFET on-current at given off-current. This is in turn an urging need to enable substantial power supply voltage scaling (well below the approximately 1V level maintained over the last generations) without compromising switching delay and area density; hence, ultimately, to have more efficient circuits and low power dissipation.

The development of III-V-based fully depleted SOI, FinFET or nanowire MOSFET technology for logic applications integrated onto Silicon wafers poses many challenges for material selection, device architecture design, fabrication, electrical characterization, modeling and simulation. If not properly understood, or duly controlled by optimized design, detrimental effects such as reduced density of states, interface traps and Fermi level pinning, enhanced leakage mechanisms, high series resistance (just to mention a few) may delay or prevent industry from achieving the benefits expected from III-V MOSFETs.

The tutorial will critically overview with a pedagogical approach the research in the field, and will benchmark some recent results with existing CMOS technology.

Outline

- Introduction to nanoscale MOSFETs and related technology boosters
- Device and digital circuit figures of merit
- Material properties of bulk and thin film III-V compound semiconductors
- Overview of state of the art III-V MOSFET architectures
- Characterization aspects for III-V MOSFET electrostatics and transport
- Advances in modeling and simulation of III-V MOSFETs
- III-V MOSFET performance and benchmarks

RF and Analog Device Technologies
Anthony Chou
Globalfoundries

RF wireless applications range widely from short range technologies such as Bluetooth, to longer distance communication like cellular transmission. The RF and analog device technologies that support this range of RF applications are similarly broad and varied, including RF-CMOS, RF-SOI, and SiGe BiCMOS.

Outline

- Key RF parametrics and characterization
- RF-CMOS / Analog System-on-Chip device technologies
  - RF FET characteristics
  - Capacitors
  - Inductors
  - Precision resistors
  - Diodes
- RF-SOI technologies
- SiGe BiCMOS technologies

Implantable MEMS and Microsystems for Neural Interface
Euisik Yoon
University of Michigan

Mapping brain activity has received growing interest as it may give a clue of what makes any one neuron fire, or not fire, and how they are connected to process information. This would eventually improve disease treatment and unlock biomimetic computational methods. MEMS and microsystems are expected to continue to offer new and exciting solutions to meet the need for high-density and high-fidelity neural interfaces.

The number of simultaneously recorded neurons has increased to ~1,000 over the past decades and will continue to increase beyond 10,000 or even more in the next five to ten years. Scaling silicon probe technologies using advanced photolithography with monolithic circuit integration can be an option to increase the density of recording channels, while hybrid MEMS/circuits integration is being pursued for versatile and adaptable use. Integrating LEDs or waveguides on the probe shank has been explored to add optical stimulation capability, which can provide selective stimulation for target neurons at a specific wavelength thanks to recent development of optogenetics. Flexible electrode arrays can provide conformal placement on cortex for ECoG or surface recording, and may reduce tissue reaction due to micromotions in the penetrating probes. Eventually, the neural interface module should resolve the tethering issue by wirelessly transmitting the recorded neural signals in a distributed system to cover the large area of the brain.

Outline

1. Brief history of neural interface
2. Modality of neural signals
3. Moore’s law in neural recording

4. Scaling silicon probe geometry
5. Flexible neural probes
6. Optoelectrodes: integrating optical devices on probes
7. ECoG and Neuro-Grid: surface recording
8. Distributed wireless neural interface
9. Brain mapping and high-density probes
10. Future Direction

SHORT COURSE

Emerging CMOS Technologies at 5nm and Beyond

Sunday, December 6, 2015
8:30 a.m. – 5:15 p.m.

In this short course, we invite world's leading experts to give us their vision on what's needed for future CMOS technology to scale to 5 nm and beyond. 5 nm is within a factor of ten of the atomic size, which demands a paradigm shift in many aspects of the technology: device type, process integration, interconnect, patterning, and manufacturability.

For device and material options, III-V MOSFETs, band-to-band tunnel FETs, nanowire FETs, and 2D semiconductors will be considered, among other options. Their merits and challenges, with reference to today's state-of-the-art 14 nm FinFETs, will be discussed. For process integration, the focus is on scaling of fully depleted devices, FinFETs, high-mobility channel material, and SRAM cell. Opportunities include horizontal and vertical nanowires with 3D integration. Interconnects will face power dissipation, insufficient bandwidth, and signal latency problems. The question is how far can we push Cu/low-k to its physical limitation? And will alternative schemes, like carbon nanotubes, optical interconnects, and 3D interconnects meet the challenge? Patterning at 5 nm and beyond will be extremely demanding, requiring a multiplex of resolution enhancing techniques and extreme ultra-violet lithography whose status will be reviewed. Challenges on the resist and mask will also have to be met. Variability is the maker or breaker of CMOS manufacturing at 5 nm. Various sources of local, global, and time dependent variability will be examined. Design-technology co-optimization (DTCO) will be discussed as one of the possible solutions. The short course will conclude with a few thoughts from the organizer on the historical perspective.

Device Options and Tradeoffs
Instructor: Mark Lundstrom and Xingshu Sun, Purdue University, Dimitri Antoniadis, MIT and Shaloo Rakheja, New York Univeristy

- IV Theory of Nanotransistors
- III-V MOSFETs
- Nanowire FETs
- Band-to-Band Tunnel FETs
- 2D channel Materials

Process Integration Challenges
Instructor: Bruce Doris, IBM Corporation

- Integration Challenges for 5nm Node FinFET
- SRAM area scaling
- Alternate Channel Materials
- Horizontal and Vertical Nanowires

BEOL Process Challenges
Instructor: Takeshi Nogami, IBM Corporation

- Extending the Cu/low-k integration
- Cu volume and grain size
- Physical limitation to RC performance
- Electromigration and TDDB reliability

Emerging Interconnect Technologies
Instructor: Krishna Saraswat, Stanford University

- Scaling limitation of Cu/low-k interconnects
- CNT and graphene
- Optical interconnects
- 3-D integration: bonding/TSV

Advanced Lithography
Instructor: Anthony Yen, TSMC

- Principles of projection imaging
- Resolution-enhancing techniques
- Scanner, mask, photoresist
- Extreme-ultraviolet lithography (EUVL)

Variability and design for manufacturability
Instructor: Asen Asenov, Glasgow University, and Gold Standard Simulations Ltd.

- Long range, short range and statistical variability
- Time dependent variability
- Variability aware compact model
- Design-Technology Co-Optimisation

SHORT COURSE

Memory Technologies for Future Systems

Sunday, December 6, 2014
9:15 a.m. – 5:30 p.m.

Course Organizer: Dirk Wouters, RWTH-Aachen University, Germany.

Memories form an increasingly important part of any electronic system, complying with the ever-growing demand for large size data handling and storage. In order to optimize both system performance and cost, a combination of three different memory types is conventionally used: SRAM for on-chip ultra-fast (cash) memory, DRAM for fast access working memory, and non-volatile Flash for (slow but) low cost storage memory. While SRAM is based on conventional CMOS technology, both DRAM and Flash have evolved to very specific technologies and are mainly implemented on separate chips.

Future system operation, however, may be in jeopardy as all these three conventional memories are facing important roadblocks towards further technology scaling. Solutions that are currently pursued surpass conventional scaling engineering and material improvements, and increasingly rely on new integration paradigms as 3D memory.

In parallel, new emerging memory concepts based on resistive switching (RRAM, PCM and STT-MRAM) are intensively investigated as possible replacing candidates. Particular of interest, however, seems their potential as a new class of memory, called storage class memory. Indeed, from a system perspective there is a huge gap in access time between DRAM and Flash, and system performance could be considerably improved by a so-called storage class memory technology that combines non-volatility with an intermediate speed.(and cost), like the recently announced 3D Xpoint™ memory.

This short course will discuss in detail the status and evolution of both DRAM and Flash memory technologies as well of the major emerging new memories (ReRAM, PCM and STT-MRAM). On the other hand, it will give a system-based view on the requirement for memories that drives their future technology roadmap as well as possible applications.

System Requirements for Memories

Instructor: Rob Aitken, ARM Fellow at ARM Research

- Limitations of current memory technologies for systems
- Including also discussion SRAM
- Storage Class Memories
- Requirements for future memories for system point of view

Conventional memory technologies : DRAM

Instructor: Changyeol Lee, research fellow, SK Hynix

- Current technology
- Further scaling roadmap
- Issues and potential roadblocks
- Including 3D stacked IC

Conventional memory technologies : Flash memory

Instructor: Youngwoo Park, Master in semiconductor R&D center at Samsung Electronics

- Current technology
- Scaling roadmap
- issues and potential roadblocks.
- Including 3D Flash

Emerging memory technologies : ReRAM and PCM

Instructor: Daniel Ielmini, Associate Professor at Politecnico di Milano

- Technology, scaling, operation potential and status
- Including discussion on potential applications (embedded – SCM –VRRAM)

Emerging memory technologies : STT-MRAM

Instructor: Thibaut Devolder, CNRS Research Associate, Univertsite Paris-Sud

- Technology, scaling and operation potential and status
- Including discussion on potential applications (SRAM – DRAM ?)

Plenary Session

Monday, December 7, 9:00 a.m.
International Ballroom Center

Welcome and Awards
General Chair: John Suehle, NIST

Invited Papers
Technical Program Chair: Patrick Fay,
University of Notre Dame

1.1 **Moore's Law at 50: Are We Planning for retirement?,** Greg Yeric, ARM Research

The Moore's Law era enjoyed a long run of lithographically-enabled pitch shrinking that directly reduced the cost per (von Neumann) function, as well as system power and performance improvements, via Dennard scaling. At the 50 year mark, the outlook for Moore's Law is muddier, as we encounter exponential complexity in MOS VLSI scaling and an increasing set of design limitations, including power limits, parasitics, variability, and of course cost. To continue to create compelling product scaling, we will increasingly require "all-of-the-above" advancements, more directly linking the MOS VLSI scaling to the circuits to the systems, in an era where future systems may be different than the computers we are familiar with.

1.2 **Quantum Computing in Silicon,** Michelle Simmons, University of New South Wales

Down-scaling has been the leading paradigm of the semiconductor industry since the invention of the first transistor in 1947. However miniaturization will soon reach the ultimate limit, set by the discreteness of matter, leading to intensified research in alternative approaches for creating logic devices. This talk will discuss the development of a radical new technology for creating atomic-scale devices which is opening a new frontier of research in electronics globally. We will introduce single atom transistors where we can measure both the charge and spin of individual dopants with unique capabilities in controlling the quantum world. To this end, we will discuss how we are now demonstrating atom by atom the best way to build a quantum computer – a new type of computer that exploits the laws of physics at very small dimensions in order to provide a predicted exponential speed up in computational processing power.

1.3 **Silicon for Prevention, Cure, and Care: A Technology Toolbox of Wearables at the Dawn of a New Health System,** Chris Van Hoof, IMEC

We are all enjoying an ever-increasing life expectancy but need to realize that the quality of our lives is at risk when we become more susceptible to chronic diseases. Today, this effectively and perversely

implies that we will be sick during a larger and increasing part of our lives. It is imperative that we focus on creating building stones that will contribute to a longer and healthier life span instead. Wearables have the grand promise and the largely untapped potential to become a cornerstone technology in the care and cure cycle as well as to enable true prevention. The different phases of one's life will require different technological tools. For chronic patients, tools are needed that improve the risk stratification, follow-up and management to monitor disease progression and prevent relapse. New technologies also have the potential to assist in curing diseases (e.g., Smart contact lenses for addressing presbyopia for everyone above the age of 45). For younger people, the tools and technologies that help us to adopt and maintain a healthy life style will come into play. A virtual coach has the potential to be your lifelong companion to a healthier life. Even earlier in life, wearable solutions used during pregnancy will give unprecedented insight in the health of the baby and the mother. Technology is not the solution but a new and highly powerful tool that can contribute to a healthier life. These efforts across the continuum of care will benefit the patient of today and may reduce the number of patients of tomorrow!

Session 2: Nano Device Technology – Ge and Other Group IV Devices
Monday, December 7, 1:30 p.m.
International Ballroom West
Co-Chairs: Wei Lu, University of Michigan
Junhee Lim, Samsung

1:35 p.m.
2.1 First Demonstration of Ge Nanowire CMOS Circuits: Lowest SS of 64 mV/dec, Highest g_{max} of 1057 µS/µm in Ge nFETs and Highest Maximum Voltage Gain of 54 V/V in Ge CMOS Inverters, H. Wu, W. Wu, M. Si, and P. Ye, Purdue University

Ge nanowire CMOS circuits are experimentally demonstrated on a Ge on insulator substrate for the first time. The nanowire CMOS devices have channel lengths from 100 to 40 nm, nanowire height of 10 nm and nanowire widths from 40 to 10 nm, and dielectric EOTs of 2 and 5 nm. Four types of Ge MOSFETs: accumulation mode and inversion mode nFETs and pFETs are studied in great details. Record low SS of 64 mV/dec and high maximum transconductance of 1057 uS/um are obtained on Ge nanowire nFETs. Furthermore, hybrid Ge nanowire CMOS with AM nFET and IM pFET is also first realized. The highest maximum voltage gain reaches 54 V/V.

2:00 p.m.
2.2 Experimental Study on Carrier Transport Properties in Extremely-Thin Body Ge-on-Insulator (GOI) p-MOSFETs with GOI Thickness Down to 2 nm, X. Yu, J. Kang, M. Takenaka, S. Takagi, The University of Tokyo

High quality ETB GOI pMOSFETs with thickness ranging from 25 nm to 2 nm have been successfully realized for the first time. The hole

mobility and the GOI thickness dependence over a wide range of GOI thickness down to 2 nm are analyzed from the viewpoint of the scattering mechanisms.

2:25 p.m.

2.3 First Monolithic Integration of Ge P-FETs and InAs N-FETs on Silicon Substrate: Sub-120 nm III-V Buffer, Sub-5 nm Ultra-thin Body, Common Raised S/D, and Gate Stack Modules, S. Yadav, K.-H. Tan*, Annie, K.H. Goh*, S. Subramanian, K. Lu Low, N. Chen, B. Jia*, S.-F. Yoon*, G. Liang, X. Gong, Y.-C. Yeo, National University of Singapore, *Nanyang Technological University

Monolithic integration of Ge p-FETs and InAs n-FETs on silicon substrate by employing a sub-120 nm III- V buffer technology is reported for the first time. Common process flow was developed to realize Ge p- FETs and InAs n-FETs with body thicknesses below 5 nm and channel lengths smaller than 200 nm, achieving record drive currents.

2:50 p.m.

2.4 Germanium-based Transistors for Future High Performance and Low Power Logic Applications (Invited), Y.-C. Yeo, X. Gong*, M. van Dal, G. Vellianitis, M. Passlack, Taiwan Semiconductor Manufacturing Company, *National University of Singapore

In this paper, we discuss recent research progress in advancing Ge-based transistor technologies. Integration of Ge on Si substrate to enable fabrication of high performance devices and formation of high-quality gate stack for Ge FETs (particularly for n-FETs) will be discussed. We also explore opportunities to boost the mobility of Ge, e.g. by incorporating Sn in Ge to form $Ge_{(1-x)}Sn_{(x)}$. Furthermore, by raising the Sn composition, the band gap of $Ge_{(1-x)}Sn_{(x)}$ becomes smaller and transits from indirect to direct, making $Ge_{(1-x)}Sn_{(x)}$ a promising material for tunneling transistors.

3:15 p.m.

2.5 A Novel Two-Varistors (a-Si/SiN/a-Si) Selected Complementary Atom Switch (2V-1CAS) for Nonvolatile Crossbar Switch with Multiple Fan-outs, N. Banno*+, M. Tada*+, K. Okamoto*, N. Iguchi*, T. Sakamoto*, M. Miyamura*+, Y. Tsuji*, H. Hada*+, H. Ochi**, H. Onodera***, M. Hashimoto****, and T. Sugibayashi*+, *NEC Corp., **Ritsumeikan Univ., ***Kyoto Univ., ****Osaka Univ., +JST-CREST

A nonvolatile and compact switch realizing multiple fan-outs of a crossbar has been newly developed by using two-varistors selected complementary atom switch (2V-1CAS). The two control lines connected to the varistors realize the accurate programming of each cross-point without select transistors. The novel nitrogen-modulated, TiN/a-Si/SiN/a-Si/TiN varistor shows superior nonlinear (NL) characteristic of $\sim 10^5$, which are successfully stacked on the top of CAS with dual-hard mask (DHM) process. The developed 2V-1CAS

($18F^2$) gives a promising switch block (SB) used for energy-efficient, nonvolatile programmable logic devices.

3:40 p.m.

2.6 Direct Bandgap GeSn Microdisk Lasers at 2.5 µm for Monolithic Integration on Si-Platform, S. Wirths, R. Geiger*^, C. Schulte-Braucks, N. von den Driesch, D. Stange, T. Zabel*, Z. Ikonic***, J.-M. Hartmann****, S. Mantl, H. Sigg*, D. Grützmacher, D. Buca, PG19 and JARA-FIT, *LMN, Paul Scherrer Institut, ^IQE, ETH, ***IMP, University of Leeds, ****Univ. Grenoble Alpes & CEA, LETI, MINATEC

We report the first experimental demonstration of direct bandgap group IV GeSn microdisk (MD) lasers grown directly on Si(001). The under-etched MDs exhibit energy offsets of E_L-E_G = 80 meV and lase at 2.5 µm. The lasing threshold and max. operation temperature amount to 220 kW/cm^2 and 135 K, respectively.

Session 3: Memory Technology – PCRAM and Flash

Monday, December 7, 1:30 p.m.

International Ballroom Center

Co-Chairs: Abu Sebastian, IBM-Zurich
Anquan Jiang, Fudan University

1:35 p.m.

3.1 MOVPE $In_{1-x}Ga_xAs$ High Mobility Channel for 3-D NAND Memory, E. Capogreco*, J.G. Lisoni, A. Arreghini, A. Subirats, B. Kunert, W. Guo, T. Maurice, C.-L. Tan, R. Degraeve, K. De Meyer, G. Van de bosch, J. Van Houdt, imec and *also with Ku Leuven

This paper presents, for the first time, feasibility of integration of $In_{1-x}Ga_xAs$ as replacement of poly-Si channel for vertical 3-D NAND memories with diameter down to 45 nm. Devices show much improved current conduction and good memory operations.

2:00 p.m.

3.2 A Novel Double-density, Single-Gate Vertical Channel (SGVC) 3D NAND Flash That Is Tolerant to Deep Vertical Etching CD Variation and Possesses Robust Read-disturb Immunity, H.-T. Lue, T.H. Hsu, C.J. Wu, W.C. Chen, T.H. Yeh, K.P. Chang, C.C. Hsieh, P.Y. Du, Y.H. Hsiao, Y.W. Jiang, G.R. Lee, R. Lo, Y.R. Su, C. Huang, S.C. Lai, L.Y. Liang, C.F. Chen, M.F. Hung, C.W. Hu, C.J. Chiu, and C.Y, Lu, Macronix International Co., Ltd

We demonstrate a novel vertical channel 3D NAND Flash architecture – SGVC. SGVC device is a single-gate, flat-channel TFT charge-trapping device with ultra-thin body. Our novel array decoding method enables a tight-pitch (25nm HP) metal BL design to fulfill the large page size (16KB) for high-performance NAND product. The SGVC flat cell possesses excellent P/E window of >8V, small X/Y/Z adjacent-cell interferences, good self-boosting inhibit, and >10K P/E cycling endurance. Due to the advantage of flat cell that is insensitive to

etching CD, SGVC device is tolerant to the non-ideal vertical etching and has shown excellent device uniformity from layer to layer. In sharp contrast to GAA VC, SGVC suffers no penalty from field-enhancement effect, thus has shown very robust read-disturb immunity against long-term gate stressing. Due to (1) two physical bits per X-Y cell footprint, and (2) efficient array design with minimal overhead, SGVC architecture has 2 to 4 times memory density than GAA VC 3D NAND at the same stacking layer number.

2:25 p.m.
3.3 A Floating Gate Based 3D NAND Technology with CMOS Under Array (Invited), K. Parat, C. Dennison*, Intel Corporation, and *Micron Technology

NAND Flash has followed Moore's law of scaling for several generations. With the minimum half-pitch going below 20 nm, transition to a 3D NAND cell is required to continue the scaling. This paper describes a floating gate based 3D NAND technology with superior cell characteristics relative to 2D NAND and CMOS under array for high Gb/mm^2 density.

2:50 p.m.
3.4 The Demonstration of Low-cost and Logic Process Fully-Compatible OTP Memory on Advanced HKMG CMOS with a Newly found Dielectric Fuse Breakdown, E.R. Hsieh, Z. H. Huang, S. Chung, J.C. Ke*, C.W. Yang*, C.T. Tsai*, and T.R. Yew*, National Chiao Tung University, *UMC

For the first time, the dielectric fuse breakdown has been observed in HKMG and poly-Si CMOS devices. It was found that, different from the conventional anti-fuse dielectric breakdown, such as the hard and soft breakdowns, this new fuse-breakdown behavior exhibits a typical property of an open gate and can be operated in much lower programming current($< 50\mu$A), fast speed($\sim 20\mu$sec), and excellent data retention, in comparison to the other fuse mechanisms. Based on this new mechanism, we have designed a smallest memory cell array which can be easily integrated into state-of-the-art advanced CMOS technology to realize highly reliable, secure, and dense OTP functionality with very low cost to meet the requirements of memory applications in the IoT era.

3:15 p.m.
3.5 Novel Fast-switching and High-data Retention Phase-change Memory Based on New Ga-Sb-Ge Material, H.-Y. Cheng, W.-C. Chien, M. BrightSky*, Y.-H. Ho, Y. Zhu*, A. Ray*, R. Bruce*, W. Kim*, C.-W. Yeh, H.-L. Lung, and C. Lam*, Macronix International Co., Ltd., *IBM T. J. Watson Research Center

Attempts to improve the retention so far must sacrifice switching speed. This work explores new phase change material based on pseudobinary GaSb-Ge system. The resulting new phase-change material has demonstrated fast switching speed of 80 ns, long endurance of 1G cycles and excellent data retention that survives 250 ^{o}C-300 hrs. The 10 years-220 ^{o}C data retention is the best ever reported. It is also the

fastest material that can pass the solder bonding criteria for embedded automotive applications.

3:40 p.m.

3.6 Crystalline-as-Deposited ALD Phase Change Material Confined PCM Cell for High Density Storage Class Memory, M. BrightSky, N. Sosa, T. Masuda*, W. Kim, S. Kim, A. Ray, R. Bruce, J. Gonsalves, Y. Zhu, K. Suu*, and C. Lam, IBM TJ Watson Research, *ULVAC

We show a robust 4:1 aspect ratio 33nm diameter confined PCM cell which utilizes an in-situ metal nitride liner plus nano-crystalline-as-deposited ALD Ge-Sb-Te phase change material. We report a programming endurance of beyond 1E10, 80ns 10x switching, and a path towards a high density PCM suitable for Storage Class Memory.

Session 4: Circuit Device Interaction – Focus Session – Beyond von Neumann Computing

Monday, December 7, 1:30 p.m.
International Ballroom East
Co-Chairs: Meng-Fan Chang, National Tsing Hua Univ.
Jan Hoentschel, GlobalFoundries

1:35 p.m.

4.1 Device and System Level Design Considerations for Analog-Non-Volatile-Memory Based Neuromorphic Architectures (Invited), S. Burc Eryilmaz, D. Kazum*, S. Yu**, H.S.P. Wong, Stanford University, *University of California, San Diego, **Arizona State University

This paper gives an overview of recent progress in the brain- inspired computing field with a focus on implementation using emerging memories as electronic synapses. Design considerations and challenges such as requirement on multilevel states, device variability, programming energy, array- level connectivity, fan-in/fan-out, wire energy and IR drop are presented. Directions for future research are discussed.

2:00 p.m.

4.2 Neuromorphic Architectures for Spiking Deep Neural Networks (Invited), G. Indiveri, F. Corradi, and N. Qiao, University of Zurich and ETH Zurich

Deep Neural Networks are massively parallel architectures that have recently shown state-of-art performance in multiple benchmarks tasks. We present neuromorphic circuits and systems for implementing such networks and demonstrate a constitutional network able to classify visual stimuli produced by a silicon retina in real-time.

2:25 p.m.

4.3 Development of a Neuromorphic Computing System (Invited), L. Shi, J. Pei, N. Deng, D. Wang, L. Deng, Y. Wang, Y. Zhang, F. Chen, M. Zhao, S. Song, F. Zeng, G. Li, H. Li, C. Ma, Tsinghua University

A new design rule of brain inspired computing system based on the current findings in brain science was proposed and the 'Tangji chip' was designed and fabricated based on it. The corresponding software and simulation platform were developed for further applications on the chip. Some applications were demonstrated.

2:50 p.m.
4.4 Large-Scale Neural Networks Implemented with Non-volatile Memory as The Synaptic Weight Element: Comparative Performance Analysis (Accuracy, Speed, and Power) (Invited), G.W. Burr, P. Narayanan, R.M. Shelby, S. Sidler, I. Boybat, C. di Nolfo, and Y. Leblebici*, IBM Research -- Almaden ,*EPFL

We review our work towards achieving competitive performance (classification accuracies) for on-chip machine learning (ML) of large-scale artificial neural networks (ANN) using Non-Volatile Memory (NVM)-based synapses, despite the inherent random and deterministic imperfections of such devices. We then show that such systems could potentially offer faster (up to 25x) and lower power (from 120–2850x) ML training than GPU–based hardware.

3:15 p.m.
4.5 Memristive Based Device Arrays Combined with Spike Based Coding Can Enable Efficient Implementations of Embedded Neuromorphic Circuits (Invited), C. Gamrat, O. Bichler, and D. Roclin, CEA, LIST

Since the rapid development of "potential" post-CMOS technologies in the last two decades, there has been a growing interest in utilizing them for implementing neuromorphic or brain-like computing architectures. We are focused on the implementation of such circuits in embedded applications with two majors concerns: integration and energy efficiency. This paper shed some lights on those developments based on results obtained in our group. The feasibility of large crossbars of synapse-like devices based on PCM or CBRAM has been studied and shows that there is still a long way ahead. Finally the introduction of spike based coding for deep neuromorphic architectures will be introduced and discussed.

3:40 p.m.
4.6 A Mixed-Signal Universal Neuromorphic Computing System (Invited), K. Meier, Ruprecht-Karls-Universität

The paper describes the design rationales, the implementation, the achievements and the future plans of the BrainScaleS neuromorphic computing system.

4:05 p.m.
4.7 Oxide Based Nanoscale Analog Synapse Device For Neural Signal Recognition System (Invited), D. Lee, J. Park, K. Moon, J. Jang, S. Park*, M. Chu**, J. Kim**, J. Noh**, M. Jeon**, B.H. Lee**, B. Lee**, B.-G. Lee** and H. Hwang, POSTECH, *SK-Hynix and **GIST

To implement an ultra-high density neuromorphic system, an ideal synapse device with various requirements (as shown in Table 1), such as >5-bit MLC characteristics, scalability down to 10nm, low power operation, endurance, data retention, and symmetric potentiation/depression characteristics is needed [1- 3]. Although various resistive switching devices were proposed for synapse application, so far, an ideal synpatic device which meets the requirements of a synapse device has not yet been reported. In this paper, we report the synapse characteristics of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) based analog resistive switching device and its application for a neural signal recognition system.

4:30 p.m.

4.8 What the Brain Tells Us about the Future of Silicon (Invited), J. Hawkins, Numenta Inc.

In this talk I will present recent progress in understanding how biological tissue in the neocortex works. These new insights suggest that many current assumptions about neuromorphic hardware will need to be modified if we want to build systems that work on the same principles as the brain.

4:55 p.m.

4.9 DARPA Neurcomputing (Invited), D. Hammerstrom, DARPA/MTO

New, neural-like, computer algorithms promise the possibility of learning on-line and in real time, to allow systems to evolve during operation. This talk will discuss DARPA's efforts in developing these algorithms, creating highly optimized hardware for them, and the resulting impact for a wide variety of DoD applications.

Session 5: Modeling and Simulation – Physical Modeling for Advanced Devices, Power Devices, and Memories

Monday, December 7, 1:30 p.m.
Georgetown Room
Co-Chairs: Susanna Reggiani, Bologna University
Haitao Liu, Micron

1:35 p.m.

5.1 Physical Modeling - a New Paradigm in Device Simulation, Z. Stanojević, O. Baumgartner, F. Mitterbauer, H. Demel, C. Kernstock, M. Karner, V. Eyert*, A. France-Lanord*, P. Saxe*, C. Freeman*, and E. Wimmer*, Global TCAD Solutions, *Materials Design s.a.r.l.

We go far beyond classical TCAD and create a simulation framework ready for contemporary and future devices. We extend drift-diffusion device simulation with additional tools: a subband structure tool, a Boltzmann transport solver, and a quantum transport solver, allowing to capture every important aspect of device operation at the nano-scale.

2:00 p.m.

5.2 ***Ab Initio*** **Study of Avalanche Breakdown in Diamond for Power Device Applications**, Y. Kamakura, T. Kotani*, K. Konaga, N. Minamitani, N. Mori, Osaka University, *Tottori University

We investigate the high-field carrier transport in diamond using a full band Monte Carlo method based on ab initio calculations. The calculated breakdown field and breakdown voltage show good agreement with experimental data of n+p- one-sided abrupt junctions with the acceptor density < 1e17 cm^{-3}. The evaluated power device figure-of-merit of diamond suggests its advantage for high temperature applications.

2:25 p.m.

5.3 Numerical Investigation of the Lateral and Vertical Leakage Currents and Breakdown Regimes in GaN-on-Silicon Vertical Structures., D. Cornigli, S. Reggiani, E. Gnani, A. Gnudi, G. Baccarani, P. Moens*, P. Vanmeerbeek*, A. Banerjee*, and G. Meneghesso**, University of Bologna, *ON Semiconductor, **University of Padova

A 2D TCAD approach is proposed to investigate breakdown of lateral and vertical GaN/AlGaN/Si structures at different temperatures. Defect-related conduction mechanisms are modeled showing, for the first time to our knowledge, that both impact ionization and Poole-Frenkel conduction must to be taken into account to correctly match the experimental data.

2:50 p.m.

5.4 Oxide-based RRAM: Requirements and Challenges of Modeling and Simulation (Invited), J. Kang, B. Gao, P. Huang, H. Li, Y. Zhao, Z. Chen, C. Liu, L. Liu, and X. Liu, Peking University

A new physical insight is presented to evaluate the RS behaviors of oxide-based RRAM. A platform including the simulators and compact models with various physical effects is developed for oxide-based RRAM. The physically based compact models including variation effect is developed for the implementation in RRAM arrays system design.

3:15 p.m.

5.5 Charge Storage Efficiency (CSE) Effect in Modeling the Incremental Step Pulse Programming (ISPP) in Charge-Trapping 3D NAND Flash Devices, W.-C. Chen, H.-T. Lue, Y.-H. Hsiao, T.-H. Hsu, X.-W. Lin*, and C.-Y. Lu, Macronix International Co., Ltd., *Synopsys Inc.

A CSE (charge storage efficiency) model is proposed to explain the origin of ISPP slope degradation for charge-trapping NAND Flash devices. It is clarified that the memory window is reduced with scaled dimension owing to the increased fringe field effect. A CSE value is defined to quantitatively account for such an effect. Our model suggests that the ISPP slope is equal to CSE.

3:40 p.m.

5.6 Statistical Poly-Si Grain Boundary Model with Discrete Charging Defects and its 2D and 3D Implementation for Vertical 3D NAND Channels, R. Degraeve, S. Clima, V. Putcha, B. Kaczer, P. Roussel, D. Linten, G. Groeseneken, A. Arreghini, M. Karner*, C. Kernstock*, Z. Stanojevic*, G. Van den bosch, J. Van Houdt, A. Furnemont, and A. Thean, imec, *Global TCAD Solutions

A new grain boundary model is proposed consisting of 1) a scattering part modeled by reduced mobility, independent of the microscopic details of the boundary, and 2) discrete randomly positioned charging defects. 2D and 3D model implementations are demonstrated, explaining several statistical properties in scaled poly-Si channel devices (particularly vertical NAND devices).

Session 6: Display and Imaging Systems – Integrated Thin Film Transistors

Monday, December 7, 1:30 p.m.
Jefferson Room
Co-Chairs: Soren Steudel, IMEC
Ryoichi Ishihara, Technical University Delft

1:35 p.m.

6.1 Carrier Transport Analysis of High-Performance Poly-Si Nanowire Transistor Fabricated by Advanced SPC with Record-High Electron Mobility, M. Oda, K. Sakuma, Y. Kamimuta, and M. Saitoh, Toshiba Corporation

This paper presents carrier transport analysis of high-mobility poly-Si nanowire transistors with advanced SPC. Record-high mobility (192cm^2/Vs) and higher electron/hole mobility than that of bulk Si at high N's are achieved, which results from not only decrease of grain boundaries but also reduction of defects inside grains and surface roughness.

2:00 p.m.

6.2 High Performance Poly Si Junctionless Transistors with Sub-5nm Conformally Doped Layers by Molecular Monolayer Doping and Microwave Incorporating CO_2 Laser Annealing for 3D Stacked ICs Applications, Y.-J. Lee, T.-C. Cho*, P.-J. Sung, K.-H. Kao**, F.-K. Hsueh, F.-G. Hou, H-C Chen, C.-T. Wu, S.-H. Hsu, Y.-J. Chen, Y.-M. Huang, Y.-F. Hou, W.-H. Huang, C.-C. Yang, B-Y Chen, K.-L. Lin, M.-C. Chen, C.-H. Shen, G-W Huang, K-P Huang^, M. Current^^, Y. Li*, S. Samukawa#, W.-F. Wu, J.-M. Shieh, T.-S. Chao*, and W. -K. Yeh, National Nano Device Laboratories, *National Chiao Tung University, **National Cheng Kung University, ***National Chung Hsing University, ^ITRI, ^^Current Scientific, #Tohoku University

A novel conformal shell doping profile (SDP) junctionless (JL) fin thin film transistor (FinTFT) formed by a damage-free molecular monolayer doping (MLD) method and a combination of microwave annealing (MWA) and CO_2 laser spike annealing (COLSA) is proposed and

studied. Thanks to the nonmelting COLSA avoiding fin deformation and dopant diffusion and resulting in an ultra- shallow (sub 5nm) and steep (< 0.8 nm/dec) doping profile with enhanced dopant activation and defect recovering. The JLFinTFT shows 163% enhancement on the Ion with superior gate control (I_{on}/I_{off} >10^7) for 3D stacked ICs applications.

2:25 p.m.

6.3 Implantation Free GAA Double Spacer Poly-Si Nanowires Channel Junctionless FETs with Sub-1V Gate Operation and Near Ideal Subthreshold Swing, P.-Y. Kuo, J.-Y. Lin, and T.-S. Chao, National Chiao Tung University

The implantation free gate-all-around (GAA) double spacer poly-Si nanowires (NWs) channel junctionless (JL) FETs (GAA DS-NW JL-FETs) have been successfully fabricated and demonstrated in the category of poly- Si NW FETs for the first time. We have scaled down the NW dimension (DNW) – length (LNW)×width (WNW)×thickness (TNW) – to 80nm×13nm×3nm by novel double spacer NW (DS-NW) processes without use of electron beam (e-beam) lithography tools. GAA DS-NW JL-FETs show good electrical characteristics: near ideal subthreshold swing (S.S.) ~ 61mV/dec., steep driving swing (D.S.) ~ 82mV/dec., and sub-1V gate operation without implantation processes for future three-dimensional integrated circuits (3-D ICs), system-on-panel (SOP) applications.

2:50 p.m.

6.4 TFT Backplane Technologies For Advanced Array Applications (Invited), R. Street, J.P. Lu, J. Bert, M. Strnad and L. Antonuk, Palo Alto Research Center

TFT backplanes are the key enabler of flat panel displays and digital x-ray imaging. As the technology continues to mature, new applications and improved performance require technology developments including flexible substrates, high performance pixel electronics and reduced manufacturing cost. The talk will describe recent progress in three alternative technologies to meet the new requirements.

3:15 p.m.

6.5 20-nm-node Trench-Gate-Self-Aligned Crystalline In-Ga-Zn-Oxide FET with High Frequency and Low Off-State Current, D. Matsubayashi, Y. Asami, Y. Okazaki, M. Kurata, S. Sasagawa, S. Okamoto, Y. Iikubo, T. Sato, Y. Yakubo, R. Honda, M. Tsubuku, M. Fujita, T. Takeuchi, Y. Yamamoto, and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd.

We proposed scalable trench-gate-self-aligned (TGSA) crystalline In-Ga-Zn-Oxide FETs formed by only 3 masks and demonstrated that the 20-nm-node FETs with 11-nm-EOT have good short-channel properties, high frequency and low off-state current. The TGSA FETs can be candidate for key devices to realize super low power LSI technology such as IoT.

3:40 p.m.
6.6 Extremely High Mobility Ultra-Thin Metal-Oxide with ns^2np^2 Configuration, C.W. Shih, A. Chin, and C.-F. Lu*, S.H. Yi*, National Chiao Tung University, *National Taiwan University

At an ultra-thin 4.5 nm thickness, high performance TFT is reached with 147 cm^2/Vs field-effect mobility, high I_{ON}/I_{OFF} of 2.3E7, small 110 mV/dec sub- threshold slope, and a low VD of 2.5 V for low power operation. From first principle quantum-mechanical calculation, the high mobility TFT is due to strongly overlapped orbitals even in ns^2np^2 configuration.

4:05 p.m.
6.7 Oxide Thin Film Transistor Technology: Capturing Device-Circuit Interactions (Invited), A. Nathan, S. Lee, S. Jeon**, and R. Chaji*, University of Cambridge, *IGNIS Innovation Inc. **Korea University
This paper presents the current status of oxide semiconductor technology for applications ranging from interactive displays to imaging systems with a strong focus on device-circuit interaction to compensate for material weaknesses and issues related to non-uniformity, instability, and persistent photoconductivity.

Session 7: Characterization, Reliability and Yield – Reliability and Characterization of Resistive RAM and BEOL Processes
Monday, December 7, 1:30 p.m.
Lincoln Room
Co-Chairs: Patrick Justison, GlobalFoundries
Tzu-Hsuan Hsu, Macronix

1:35 p.m.
7.1 Mapping of Wafer-Level Plasma Induced Charge Contour by Novel On-chip In-Situ Recorders in Advance FinFET Technologies, C.-H. Wu, Y.-P. Tsai, C-J Lin, Y and Y.-C. King, National Tsing Hua University

A novel approach of monitoring wafer-level plasma induced charging contours in FinFET process is proposed. On-chip charge collectors consist of antenna coupled floating gates have been demonstrated to record plasma charging levels during BEOL process. The data on these in-situ recorders reflect actual potential on transistor gates during plasma charging stress. Delivered wafer maps, containing positive and negative charging and antenna potential contours, provides a powerful tool for future FinFET process optimization and reliability evaluations.

2:00 p.m.
7.2 A Novel Method to Characterize the Effect from the Diffusion of Cu in Through Silicon Via (TSV), K.-D. Kim, K.-W. Kim*, M.-S. Yoo*, Y.-T. Kim*, S.-K. Park*, S.-J. Hong*, C.-H. Park**, B.-G. Park, J.-H. Lee, Seoul National University, *SK Hynix Inc., **Kwangwoon University

To characterize electrically the effect from the diffusion of Cu in TSV, a new test pattern is proposed and its effectiveness is verified experimentally. The test pattern has a shallow n+ region formed in an n- well region butted to the TSV dielectric surrounding the TSV. Through the n+/n well region, we can measure diode and gated diode currents, charge pumping current, and C-V to accurately analyze the effect. Our approach is verified to be very useful by investigating the Cu diffusion effect in the samples with two different barrier metal thicknesses.

2:25 p.m.
7.3 A Methodology to Predict The Impact Of Wafer Level Chip Scale Package Stress on High-Precision Circuits, R. van Dalen, H.P. Tuinhout, M. Stoutjesdijk, J. van Zwol, J.J.M. Zaal, J.H.J. Janssen, F.H.M. Swartjes, P.A.M. Bastiaansen, M.C. Lammers, L. Brusamarello, and M. Stekelenburg, NXP Semiconductors

A methodology is presented that allows quantitative prediction of the impact of WLCSP induced mechanical stress on high precision mixed-signal ICs. The simulation flow was tuned using high-resolution experimental variability data measured on dedicated test chips, and exemplified with an on-chip oscillator circuit suffering from WLCSP stress induced variability.

2:50 p.m.
7.4 A New Insight into BEOL TDDB Lifetime Model for Advanced Technology Scaling, M.N. Chang, Y. -H. Lee, S.Y. Lee, K. Joshi, and C.C. Ko, C.C. Chiu, K. Wu, TSMC

For the past several years, there have been debates that backend IMD-TDDB Sqrt(E) lifetime model is too conservative and becomes the constraint for BEOL technology scaling. In this study, it is demonstrated that low bias TDDB model could be varied from conservative E to aggressive Power-Law or 1/E model, depending on the materials characteristics of extreme low-k (ELK), etch stop layer (ESL), and the process conditions. Based on J-V, I-t and defect generation rate analysis, Sqrt(E) model is adequate for high-bias TDDB; however, hydrogen release, initiated by low-bias with extremely low current conduction for film with better process, explained the TDDB lifetime projection to a better fit such as the Power-Law lifetime model. The voltage acceleration factor from hydrogen release theory is quite consistent with that from TDDB data. Based on various clustering factors under wide range of TDDB stress voltages combined with the ELK chemical bonding analysis, we proposed that an inhomogeneous percolation model is an important factor in prolonging the TTF at medium or low bias and contributes to more aggressive Power-Law or 1/E lifetime models.

3:15 p.m.
7.5 Intrinsic Program Instability in HfO_2 RRAM and Consequences on Program Algorithms, A. Fantini, G. Gorine, R. Degraeve, L. Goux, C.Y. Chen**, A. Redolfi, S. Clima, A. Cabrini*, G. Torelli*, and M. Jurczak, imec, *University of Pavia, **KU Leuven

We statistically investigated resistance stability of HfO_2-based RRAM devices in the short (µs to s) time range after switching. We show for the first time that, the resistance value of both logic states is not stable after programming and subject to large discrete stochastic fluctuations. The frequency of fluctuation is found to be time-decaying thus making hard its detection in DC testing but effectively impairing write algorithms. We relate these fluctuations to spontaneous changes of filament geometry.

3:40 p.m.
7.6 Cycling-induced Degradation of Metal-oxide Resistive Switching Memory (RRAM), Z. Wang, S. Ambrogio, S. Balatti, S. Sills*, A. Calderoni*, N. Ramaswamy*, and D. Ielmini, Politecnico di Milano, *Micron Technology, Inc.

This work addresses cycling-induced degradation of HfOx RRAM. We evidence an increase of set/reset speed with cycling, which is attributed to defect generation causing enhanced ion mobility. The degradation kinetics is modelled by an Arrhenius-driven distributed-energy model. Our study allows to predict set/reset voltages at any cycle and cycling condition.

4:05 p.m.
7.7 Distribution Projecting the Reliability for 40 nm ReRAM and Beyond Based on Stochastic Differential Equation, Z. Wei, K. Eriguchi*, S. Muraoka, K. Katayama, R. Yasuhara, K. Kawai, Y. Ikeda, M. Yoshimura, Y. Hayakawa, K. Shimakawa, T. Mikawa, and S. Yoneda, Panasonic Semiconductor Solutions Co., Ltd., *Kyoto University

A physical analytic formula based on Stochastic Differential Equation was successfully developed to describe intrinsic ReRAM variation. The formula was proved useful for projecting scaled ReRAM memory window and resistance distribution after long-term retention, verified by testing 40 nm 2Mbits ReRAM. The formula also centered on practical and quantitative filament characterization.

Session 8: Process and Manufacturing Technology – 3D Integration and BEOL
Monday, December 7, 1:30 p.m.
Columbia Ballroom 1, 2, & 5
Co-Chairs: Takahiro Kouno, Socionext Inc.
Romy Liske, Fraunhofer Institute Photonic Microsystems IPMS

1:35 p.m.
8.1 Through-Cobalt Self Forming Barrier (tCoSFB) for Cu/ULK BEOL: A Novel Concept for Advanced Technology Nodes, T. Nogami, B. Briggs, S. Korkmaz, M. Chae*, C. Penny, J. Li, W. Wang, P. McLaughlin, T. Kane, C. Parks, A. Madan, S. Cohen, T. Shaw, D. Priyadarshini, H. Shobha, S. Nguyen, R. Patlolla, J. Kelly, X. Zhang*, T. Spooner, D. Canaperi, T. Standaert, E. Huang, V. Paruchuri, and D. Edelstein, IBM, * GlobalFoundries, Inc.

Through-Co self-forming-barrier (tCoSFB) metallization scheme is introduced, with Cu gap-fill capability down to 7 nm-node dimensions. Mn atoms from doped-seedlayer diffuse through CVD-Co wetting layer, to form $TaMn_xO_y$ barrier, with integrity proven by vertical-trench triangular-voltage-sweep and barrier-oxidation tests. tCoSFB scheme enables 32%/45% lower line/via resistance at 10 nm node, while achieving superior EM performance to TaN/Co, TaN/Ru.

2:00 p.m.
8.2 Novel Reconfigured Wafer-to-Wafer (W2W) Hybrid Bonding Technology Using Ultra-High Density Nano-Cu Filaments for Exascale 2.5D/3D Integration, K.-W. Lee, C. Nagai, J.-C. Bea, T. Fukushima, R. Suresh*, X. Wu*, T. Tanaka, and M. Koyanagi, Tohoku University, *Xilinx

A novel reconfigured wafer-to-wafer (W2W) hybrid bonding technology using tiny Cu electrode with 1µm size and unique anisotropic conductive film is proposed for exascale 2.5D/3D integration. To avoid the issues of current standard C2W/W2W hybrid bonding technologies, we developed three types of scaled electrodes using shallow-extrude Cu electrode, electro-less plated thin metal capping layers, thin glue adhesive layer below 1µm and anisotropic conductive film compose of ultra-high density nano-Cu filaments. Multi numbers of TEG dies with 7mm x 23mm size are simultaneously aligned with high accuracy of below 1µm and thermal-compression bonded in wafer-level. 136,800 Cu electrodes with tiny size of 3µm diameter are successfully intact bonded by new reconfigured W2W hybrid bonding technology.

2:25 p.m.
8.3 A Robust Wafer Thinning Down to 2.6- µm **for Bumpless Interconnects and DRAM WOW Applications**, Y. S. Kim, S. Kodama, Y. Mizushima, T. Nakamura, N. Maeda, K. Fujimoto, A. Kawai*, K. Arai*, and T. Ohba, Tokyo Institute of Technology, *DISCO Corporation.

An ultra-thinning down to 2.6- µm with and without Cu contamination at 10^{13} atoms/cm^2 using 300-mm wafer proven by 2Gb DRAM has been developed for the first time. The impact of Si thickness and Cu contamination at wafer backside for DRAM yield including retention characteristics is described. Thickness uniformity for all wafers after thinning was below 2- µm within 300-mm wafer. A degradation in terms of retention characteristics occurred after thinning down to 2.6- µm while no degradation after thinning down to 5.6- µm for both wafer and package level test were found.

2:50 p.m.
8.4 Advanced Device Performance Impact by Wafer Level 3D Stacked Architecture, J.C. Liu, K.C. Huang, Y.H. Chu, J.M. Hung, C.C. Change, Y.L. Wei, J.S. Lin, M.F. Kao, P.T. Chen, S.Y. Huang, H.C. Lin, W.D. Wang, P. Chou, C.F. Lu, Y.L. Tu, F.J. Shiu, C.F. Huang, C.H. Lin, T.H. Lu, and D.N. Yaung, Taiwan Semiconductor Manufacturing Company

A high density 50K~100K/mm^2 cross-tier connection featuring backside through-via (BTV) and wafer level 3D stacking technologies has been successfully demonstrated. Wafer stacking and thinning to < 1/250 Si thickness process showed little to no impact to advanced device performance. BTV induced stress effect was also studied; quite different behaviors between wafers with SiGe and without SiGe process were found. SiGe local strain will be diminished by BTV induced strain when BTV getting too close to channel, and hence lower hole mobility. This impact could be minimized by proper Keep-Out Zone (KOZ) design. Furthermore, 3D stacked architecture provides the opportunity to individually optimize process and design for each function block on separated wafers, thus improve chip performance and power consumption, and also benefit chip footprint.

3:15 p.m.
8.5 New Challenges and Opportunities for 3D Integrations (Invited), J. Michailos, P. Coudrain, A. Farcy, N. Hotellier, S. Cheramy*, S. Lhostis, E. Deloffre, Y. Sanchez, A. Jouve*, F. Guyader, E. Saugier, V. Fiori, P. Vivet*, M. Vinet*, C. Fenouillet-Beringer*, F. Casset*, P. Batude*, F. Boeuf, Y. Henrion, B. Vianne, L.-M. Collin, J.-P. Colonna*, L. Benaissa*, L. Brunet*, R. Prieto, R. Velard, and F. Ponthenier*, STMicroelectronics, *University of Grenoble Alpes

From low density 3D integrations embedding Via Last Through Silicon Vias (TSV) to high densities hybrid bonding or 3D VSLI CoolCube^{TM} solutions, a multitude of new product opportunities is now envisioned. An overview of existing emerging 3D integrations is provided covering Image sensors, Photonics, MEMS, Wide I/O memories and Silicon Interposers for advanced logics. Associated key challenges and developments are highlighted focusing on 3D platform performance assessment.

3:40 p.m.
8.6 Interest of SiCO Low k=4.5 Spacer Deposited at Low Temperature (400°C) in the Perspective of 3D VLSI Integration, D. Benoit, J. Mazurier*, B. Varadarajan**, S. Chhun, S. Lagrasta, C. Gaumer, D. Galpin, C. Fenouillet-Beranger*, D. Vo-Thanh, D. Barge, R. Duru, R. Beneyton, B. Gong**, N. Sun**, N. Chauvet**, P. Ruault**, D. Winandy**, B. van Schravendijk**, P. Meijer**, and O. Hinsinger, STMicroelectronics, *CEA-LETI MINATEC, ** Lam Research

A new SiCO spacer material deposited at 400°C is evaluated in 14FDSOI. The benefit of SiCO low-k value (4.5 vs 7 for SiN) translates into a 5% decrease for effective capacitance and delay of FO3 Ring Oscillators. Its low deposition temperature makes SiCO an attractive candidate for 3DVLSI CoolCube^{TM} integration.

4:05 p.m.
8.7 Enabling Low Power BEOL Compatible Monolithic 3D$^+$ Nanoelectronics for IoTs Using Local and Selective Far-Infrared Ray Laser Anneal Technology, C.-C. Yang, J.-M. Shieh, T.-Y. Hsieh, W.-H. Huang, H.-H. Wang, C.-H. Shen, T.-T. Wu, Y-F Hou, Y-J Chen*, Y-J Lee, M-C Chen, F-L Yang**, Y-H Chen, , M.-C. Wu*, and

W.-K. Yeh, National Nano Device Laboratories, *National Tsing Hua University, **Academia Sinica

Local and selective far-infrared ray laser annealing (FIR-LA) process with very short heating duration (<100us) and low substrate temperature (<400°C) enables sequentially stacked gate-first nanowire FETs (NWFETs), including $3D^+$ Si NWFET and poly-Ge junctionless (JL) NWFET, and BEOL compatible monolithic $3D^+$ nanoelectronics. The $3D^+$ Si NWFETs, demonstrated by green nano-second laser crystallization (GNS-LC) and FIR-LA processes exhibit steep subthreshold swing (<90mV/dec.) and high driving current (n-type: 310μA/μm and p-type: 220μA/μm). The 7nm poly-Ge JLNWFET shows high Ion/Ioff ratio ($>5\times10^4$) and small DIBL. The thus fabricated low driving voltage 6T SRAM shows a static noise margin (SNM) of 130 mV at V_d=0.4V enabling the low power and low cost $3D^+$IC for internet of things (IoTs).

4:30 p.m.

8.8 Advanced 3D Monolithic Hybrid CMOS with Sub-50 nm Gate Inverters Featuring Replacement Metal Gate (RMG)-InGaAs nFETs on SiGe-OI Fin pFETs, V. Deshpande, V. Djara, E. O'Connor, P. Hashemi*, K. Balakrishnan*, M. Sousa, D. Caimi, A. Olziersky, L. Czornomaz, and J. Fompeyrine, IBM Research GmbH, *IBM TJ Watson Research Center

We demonstrate, for the first time, scaled hybrid inverters built in a 3D Monolithic (3DM) CMOS process featuring short-channel replacement metal gate (RMG) InGaAs-OI wide-fin/planar nFET top layer and SiGe-OI fin pFET bottom layer. We achieve state-of-the-art device integration, using raised source drain (RSD) on both levels and silicide on bottom pFETs. Bottom SiGe-OI pFETs are scaled down to sub-20 nm gate length (L_g) using a gate first (GF) flow, and top InGaAs nFETs scaled down to sub-50 nm Lg are fabricated using a RMG process. With an optimized thermal budget for the top InGaAs nFETs, we show that the 3D integration scheme does not degrade the performance of the bottom SiGe-OI pFETs. Finally, we demonstrate well-behaved integrated inverters with sub-50 nm L_g down to V_{DD} = 0.25 V.

Session 9: Power and Compound Semiconductor Devices – Advanced Compound RF and Power Devices

Monday, December 7, 1:30 p.m.
Columbia Ballroom 3, 4, & 6
Co-Chairs: Marleen Van Hove, imec
Clemens Ostermaier, Infineon Technologies

1:35 p.m.

9.1 Collapse-Free High Power InAlGaN/GaN-HEMT with 3 W/mm at 96 GHz, K. Makiyama, S. Ozaki, T. Ohki, N. Okamoto, Y. Minoura*, Y. Niida, Y. Kamada*, K. Joshin, K. Watanabe, Y. Miyamoto*, Fujitsu Limited, *Tokyo Institute of Technology

We demonstrated excellent output power density of 3.0 W/mm at 96 GHz using novel current collapse free InAlGaN/GaN-HEMT with an

80-nm gate electrode. To eliminate the current collapse, unique double-layer silicon nitride (SiN) passivation film which has oxidation resistance was adopted.

2:00 p.m.
9.2 High Frequency High Breakdown Voltage GaN Transistors (Invited), F. Medjdoub, N. Herbecq, A. Linge, M. Zegaoui, IEMN-CNRS

In this paper, high performance ultrathin barrier GaN devices for high frequency applications are presented. In particular, key features to achieve significant breakdown voltages and high robustness while using sub-10 nm barrier thickness are discussed.

2:25 p.m.
9.3 26.5 Terahertz Electrically Triggered RF Switch on Epitaxial VO_2-on-Sapphire (VOS) Wafer, H. Madan, H.-T. Zhang, M. Jerry, D. Mukherjee, N. Alem, R. Engel-Herbert, and S. Datta, The Pennsylvania State University

An electrically triggered VO_2 RF switch with record switching cut-off frequency of 26.5THz was demonstrated. The switch exhibits an isolation >35dB and a low 0.5dB insertion loss, up-to 50GHz. The switch features a highly linear response with P1dB >12dBm and OIP_3 >44dBm. Additionally, the switch shows an electrical turn-on-delay of<25ns.

2:50 p.m.
9.4 Enhancement-mode GaN Double-Channel MOS-HEMT with Low On-resistance and Robust Gate Recess, J. Wei, S. Liu, B. Li, X. Tang, Y. Lu, C. Liu, M. Hua, Z. Zhang, G. Tang, and K.J. Chen, The Hong Kong University of Science and Technology

Enhancement-mode GaN double-channel MOS-HEMT was fabricated on an optimized heterostructure, featuring an upper MOS-channel with high quality interface and a lower heterojuntion channel with high electron mobility. The device delivers a small on-resistance, large current, high breakdown voltage, and sharp subthreshold slope. A larger tolerance in the gate recess depth is also obtained.

3:15 p.m.
9.5 A Next Generation CMOS-Compatible GaN-on-Si Transistors for High Efficiency Energy Systems, K.-Y. Wong, M.-H. Kwan, F.-W. Yao, M.-W. Tsai, Y.-S. Lin, Y.-C. Chang, P.-C. Chen, R.-Y. Su, J.-L. Yu, F.-J. Yang, G. P. Lansbergen, C.-W. Hsiung, Y.-A. Lai, K.-L. Chiu, C.F. Chen, M.-C. Lin, H.-Y. Wu, C.-H. Chiang, S.-D. Liu, H. -C. Chiu, P.-C. Liu, C.-M. Chen, C.-Y. Yu, C.-S. Tsai, C.-B. Wu, B. Lin, M.-H. Chang, J.-S. You, S.- P. Wang, L.-C. Chen, Y.-Y. Liao, L.Y. Tsai, T. Tsai, H.C. Tuan, and A. Kalnitsky, Taiwan Semiconductor Manufacturing Company, Ltd.

High switching performance of low cost CMOS-compatible GaN-on-Si 100/650V E-HEMTs and 650V D-MISFET are demonstrated. The mechanism of dynamic Ron is studied and a new methodology to

analyze the interface trap location is proposed. Furthermore, both 100V / 650V E-HEMT passed industrial reliability qualification (JEDEC) including 1000 hrs high temperature reverse bias (HTRB). Device performances are verified by energy system with strong robustness and are ready for manufacture.

3:40 p.m.
9.6 GaNFET Compact Model for Linking Device Physics, High Voltage Circuit Design and Technology Optimization, U. Radhakrishna, S. Lim, P. Choi, T. Palacios, and D.A Antoniadis, Massachusetts Institute of Technology

This work is the first demonstration of a physics- based GaN HEMT compact model that is calibrated and verified all the way from individual device- to a HV-buck converter circuit, along with an illustration of use in technology optimization. GaN HEMT based high voltage (HV) switching converters are gaining foothold in the medium voltage (<1000 V) power conversion applications. In order to design such high voltage GaN circuits, the device compact model must accurately describe static and dynamic switching behavior to enable designers to gain insight into the impact of the behavioral nuances of the GaN HEMTs on HV circuit performance, such as non-quasi-statics, which is not possible with the available models. The model is validated against DC-IV, -CV, and pulsed-IV measurements of fabricated devices and is then verified by comparing measured and simulated signals in a commercial buck converter. Furthermore we demonstrate that our physics-based model can be used as a device design and multi-dimensional optimization tool to estimate device parameters such as field plate (FP) lengths and FP dielectric thicknesses (t_d) to maximize the switching figure-of- merit (FoM), $BV^2/R_{on}Q_g$.

4:05 p.m.
9.7 GaN-on-GaN p-n Power Diodes with 3.48 kV and 0.95 mΩ·cm^2: A Record High Figure-of-Merit of 12.8 GW/cm^2, K. Nomoto, M. Zhu, B. Song, Z. Hu, M. Qi*, R. Yan, V. Protasenko, E. Imhoff**, J. Kuo***, N. Kaneda^, T. Mishima^^, T. Nakamura^^, D. Jena, H. Xing, Cornell University, *University of Notre Dame, **Naval Research Laboratory, ***Signatone Corporation, ^Quantum Spread, Ltd., ^^Hosei University

We report GaN p-n junction diodes on free-standing GaN substrates with record performance: a low specific on-resistance (Ron) of ~ 1 mΩ·cm^2 and high breakdown voltages (BV) ranging from 2.3 to 3.5 kV for drift layer thicknesses ranging from 20 to 32 μm.

Session 10: Memory Technology - RRAM
Tuesday, December 8, 9:00 a.m.
International Ballroom Center
Co-Chairs: Ludovic Goux, IMEC
Luca Perniola, CEA/LETI

9:05 a.m.
10.1 Non Volatile Memory Evolution and Revolution (Invited), P. Cappelletti, Micron Technology

The paper analyzes the present NVM scenario from an evolution strategy viewpoint, considering both technology features and application needs. It is shown how 3D NAND can and will continue the roadmap for lower-cost/higher-density NVMs. It is then discussed why emerging memories will hardly compete with 3D NAND in cost and density. The application range for emerging memories is finally mapped vs. required features, showing which EM technology looks most promising for each application.

9:30 a.m.
10.2 Demonstration of 3D Vertical RRAM with Ultra Low-leakage, High-selectivity and Self-compliance Memory Cells, Q. Luo, X. Xu, H. Liu, H. Lv, T. Gong, S. Long, Q. Liu, H. Sun, W. Banerjee, L. Li, J. Gao, N. Lu, S.S. Chung*, J. Li**, and M. Liu, Chinese Academy of Sciences, *National Chiao Tung University, **University of Wisconsin-Madison

In this work, a four-layer V-RRAM array, with high performance HfO_2/MIEC bilayer self-selective cell, was demonstrated for the first time. Several salient features were achieved, including ultra-low half-select leakage (<0.1 pA), very high nonlinearity (>10^3), low operation current (nA level), self-compliance, high endurance (>10^7), and robust read/write disturbance immunity.

9:55 a.m.
10.3 Improvement of Characteristics of NbO_2 Selector and Full Integration of $4F^2$ 2x-nm Tech 1S1R ReRAM, S.G. Kim, T.J. Ha, S. Kim, J.Y. Lee, K.W. Kim, J.H. Shin, Y.T. Park, S.P. Song, B.Y. Kim, W.G. Kim, J.C. Lee, H.S. Lee, J.H. Song, E.R. Hwang, S.H. Cho, J.C. Ku, J.I. Kim, K.S. Kim, J. H. Yoo, H.J. Kim, H.G. Jung, K.J. Lee, S.Chung, J.H. Kang, J.H. Lee, H. Kim, S.J. Hong, G. Gibson*, and Y. Jeon*, SK Hynix, *HP Laboratories

The authors report that 2x nm cross-point ReRAM with 1S1R structure has been successfully developed. Off- current at 1/2 V_{sw} of 1S1R is one of key factor for high-density ReRAM. NbO_2 was chosen as a selector material and off-current and forming characteristics were improved by using stack engineering of top and bottom barriers as well as spacer materials. Finally array operation was characterized with the integration of selector and resistor materials.

10:20 a.m.
10.4 Cu BEOL Compatible Selector with High Selectivity (>10^7), Extremely Low Off-current (~pA) and High Endurance

(>10^{10}), Q. Luo, X. Xu, H. Liu, H. Lv, T. Gong, S. Long, Q. Liu, H. Sun, W. Banerjee, L. Li, N. Lu, and M. Liu, Chinese Academy of Sciences

In this work, we present a high performance Cu BEOL compatible threshold switching (TS) selector with several outstanding features, such as high nonlinearity (~10^7), ultra-low off-state leakage current (~pA), robust endurance (>10^{10}), and sufficient on-state current density (~1 MA/cm^2).

10:45 a.m.
10.5 1Kbit FINFET Dielectric (FIND) RRAM in Pure 16nm FinFET CMOS Logic Process, H.-W. Pan, K.-P. Huang, S.-Y. Chen, P.-C. Peng, Z.-S. Yang, C.-H. Kuo*, Y.-D. Chih*, Y.-C. King, C.J. Lin, and National Tsing Hua University, *Taiwan Semiconductor Manufacturing Company

A fully CMOS process compatible FinFET Dielectric RRAM (FIND RRAM) is firstly proposed and demonstrated by 1kbit RRAM macro on 16nm standard FinFET CMOS logic platform. The new 16nm low voltage FIND RRAM consists of one FinFET transistor for select gate and an HfO2-based resistive film for a storage node of the cell. The FIND RRAM largely improves the set and reset characteristics by the locally enhanced field at fin corners and results in a low set voltage and reset current in array operation. Besides, by adopting the 16nm FinFET CMOS logic process, the FIND RRAM is shrink to an aggressive cell size of 0.07632μm^2 without additional mask or process step. The low voltage operation, excellent reliability, and very stable LRS/HRS window are all realized in the new fabricated 1kbit macro. They all support the new FIND RRAM technology is a promising embedded NVM in the coming FinFET era.

11:10 a.m.
10.6 Programming-Conditions Solutions Towards Suppression of Retention Tails of Scaled Oxide-Based RRAM, C.-Y. Chen*, A. Fantini, L. Goux, R. Degraeve, S. Clima, A. Redolfi, G. Groeseneken*, and M. Jurczak, imec, *also with KU Leuven

We evidence for the first time that LRS retention tails are not controlled by resistance levels but by low activation-energy diffusing species which are understood as metastable oxygen ions in the neighborhood of the conductive filament constriction. Effective programming pathways are demonstrated to minimize their impact.

11:35 a.m.
10.7 Comprehensive Assessment of RRAM-based PUF for Hardware Security Applications, A. Chen, GLOBALFOUNDRIES

The stochastic behavior and intrinsic variability of resistive random access memory (RRAM) can be utilized to implement physical unclonable function (PUF) for hardware security applications. Performance of RRAM PUF depends on RRAM device characteristics. Reliability of RRAM PUF may degrade with retention loss, read instability and thermal variation, while PUF uniqueness is maintained

as long as the randomness in RRAM resistance distribution is preserved. Based on key PUF metrics, this paper presents a systematic approach and a comprehensive evaluation for this novel application of RRAM.

Session 11: Circuit Device Interaction – CMOS Scaling and Circuit/Device Variability
Tuesday, December 8, 9:00 a.m.
International Ballroom East
Co-Chairs: Curtis Tsai, Intel
Susan Wu, Xilinx

9:05 a.m.
11.1 2RW Dual-port SRAM Design Challenges in Advanced Technology Nodes, K. Nii, M. Yabuuchi, Y. Yokoyama, Y. Ishii, T. Okagaki, M. Morimoto, Y. Tsukamoto, K. Tanaka, M. Tanaka, and S. Tanaka, Renesas Electronics Corporation

We discuss the candidates of 2 read/write (2RW) 8T dual-port (DP) SRAM bitcell layouts in advanced planar/FinFET technologies. 256-kbit 2RW DP SRAM macros with good symmetrical 8T DP bitcell were designed and fabricated using 16 nm FinFET technology. With introducing wordline over-driven read/write assist, V_{min} is improved by 120 mV and observed 0.5 V operations successfully.

9:30 a.m.
11.2 Design and Process Technology Co-Optimization with SADP BEOL in sub-10nm SRAM Bitcell, Y. Woo, M. Ichihashi, S. Parihar, L. Yuan, S. Banna, and J. Kye, GlobalFoundries

As the device scaling continues, multiple patterning technologies are implemented. The patterning technology and metal architecture should be co-optimized to improve electrical performance of circuitry. This paper demonstrates how such an optimization in a sub-10nm node technology can improve the electrical performance of SRAM bitcell.

9:55 a.m.
11.3 Experimental Study on BTI Variation Impacts in SRAM Based on High-k/Metal Gate FinFET: From Transistor Level Vth Mismatch, Cell Level SNM to Product Level Vmin, C. Liu, H. Nam, K. Kim, S. Choo, H. Kim, H. Kim, Y. Kim, S. Lee, S. Yoon, J. Kim, J. Kim, L. Hwang, S. Ha, M-J Jin, H.C. Sagong, J.-K. Park, S. Pae, and J. Park, Samsung Electronics Company Ltd.

Aging induced variability has been shaving away the design margins in advanced SRAM which may become more serious with highly scaled process node. This paper provides a systematical study of the BTI variation impacts in FinFET SRAM based on 14nm 128Mbit SRAM, including the characterization from transistor and cell level to product. The results indicate that besides the process optimization for BTI mean shifts, reliability aware circuit design is necessity to consider intrinsic BTI variation increase with transistor scaling down.

10:20 a.m.

11.4 Magnetic Thin-Film Inductors for Monolithic Integration with CMOS, N. Sturcken, R. Davies, H. Wu, M. Lekas, K. Shepard, K.W. Cheng*, C.C. Chen*, Y.S. Su*, C.Y. Tsai*, K.D. Wu*, J.Y. Wu*, Y.C. Wang*, K.C. Liu*, C.C. Hsu*, C.L. Chang*, W.C. Hua*, and A. Kalnitsky*, Ferric, Inc., Columbia University, *Taiwan Semiconductor Manufacturing Company

This paper presents magnetic thin-film inductors for monolithic integration with CMOS for DC-DC power conversion. Magnetic core inductors were fabricated using conventional CMOS processes to achieve peak inductance density of 290nH/mm^2, quality factor 15 at 150MHz, current density exceeding 11A/mm^2 and coupling coefficient of 0.89 for coupled inductors.

10:45 a.m.

11.5 Reliability Variability Simulation Methodology for IC Design: an EDA Perspective (Invited), A. Zhang, C. Huang, T. Guo, A. Chen, S. Guo*, R. Wang*, R. Huang*, J. Xie, Cadence Design Systems Inc., *Peking University

This paper presents reliability variability simulation with Monte Carlo method. Both process variation and aging variation, as well as their correlation, are considered. Two simulation flows are developed and used to study reliability variability. Simulation accuracy and performance are discussed. The flows are validated with ring oscillator and SRAM circuit.

11:10 a.m.

11.6 Self-heating on Bulk FinFET from 14nm Down to 7nm Node, D. Jang, E. Bury*, R. Ritzenthaler, M. Garcia Bardon, T. Chiarella, K. Miyaguchi, P. Raghavan, A. Mocuta, G. Groeseneken*, A. Mercha, D. Verkest, A. Thean, imec,*also with KU Leuven

Self-heating effects of scaled bulk FinFETs from 14nm to 7nm node are discussed, as well as ways to mitigate SHE at device level based on 3DFEM simulations and electrical measurements. Finally, the impact of SHE on circuit level performance is also studied for high performance and low power devices.

11:35 a.m.

11.7 Adding the Missing Time-Dependent Layout Dependency into Device-Circuit-Layout Co-Optimization--New Findings on the Layout Dependent Aging Effects, P. Ren, X. Xu*, P. Hao, J. Wang, R. Wang, M. Li, J. Wang**, W. Bu**, J. Wu**, W. Wong**, S. Yu**, H. Wu**, S.-W. Lee**, D.Z. Pan*, and R. Huang, Peking University, *The University of Texas at Austin, **Semiconductor Manufacturing International Corporation (SMIC)

In this paper, a new class of layout dependent effects (LDE)—the time-dependent layout dependency due to device aging, is reported for the first time. The BTI and HCI degradation in nanoscale HKMG devices are experimentally found to be sensitive to layout configurations, even biased at the same stress condition. This new effect of layout dependent

aging (LDA) can significantly mess the circuit design, which conventionally only includes the static LDE modeled for time-zero performance. Further studies at circuit level indicate that, for resilient device-circuit-layout co-design, especially to ensure enough design margin near the end of life, LDA cannot be neglected. The results are helpful to guide the cross-layer technology/design co- optimization.

Session 12: Modeling and Simulation – Modeling of 2D and Organic Semiconductor Devices
Tuesday, December 8, 9:00 a.m.
Georgetown Room
Co-Chairs: John Robertson, Cambridge University
Debdeep Jena, Cornell University

9:05 a.m.
12.1 Phonon-Limited Performance of Single-Layer, Single-Gate Black Phosphorus n- and p-type Field-Effect Transistors, A. Szabo, R. Rhyner, H. Carrillo-Nunez, and M. Luisier, ETH Zurich

An ab-initio quantum transport approach is used to calculate the electron and hole phonon-limited mobility of single-layer black phosphorus transistors and simulate their I-V characteristics. A strong anisotropy of the transport properties is observed with the armchair configuration delivering the highest mobility and drive currents.

9:30 a.m.
12.2 Effects of Interlayer Interaction in van der Waals Layered Black Phosphorus for Sub-10nm FET, K.T. Lam, S. Luo, B. Wang, C.-H. Hsu, A. Bansil*, H. Lin, and G. Liang, National University of Singapore, *Northeastern University

Current characteristics of few-layer BP FETs with 7-nm channel were calculated numerically using Wannier function Hamiltonians with accurate interlayer coupling terms. The potentials in each layer were different due to the weak van der Waals forces, necessitating a double-gated MOSFET for optimal performance. Elastic AP scattering reduced I_{ON} by 50%.

9:55 a.m.
12.3 Designing Band-to-Band Tunneling Field-Effect Transistors with 2D Semiconductors for Next-Generation Low-Power VLSI, W. Cao, J. Jiang, J. Kang, D. Sarkar, W. Liu, and K. Banerjee, University of California, Santa Barbara

Tunneling field-effect transistors (TFETs) are well known for their potential in low power electronics. The emerging two-dimensional (2D) semiconductors provide an excellent platform for constructing TFETs with desired properties. In this paper, by employing Non-Equilibrium Green's function (NEGF) based quantum transport simulations, 2D semiconductor based TFETs are innovatively designed and optimized, in terms of performance, energy efficiency, and scalability (up to 3 nm gate length) improvement w.r.t. ITRS requirements.

10:20 a.m.

12.4 How Good is Mono-Layer Transition-Metal Dichalcogenide Tunnel Field-Effect Transistors in sub-10 nm? --An *ab initio* Simulation Study, X.-W. Jiang, J.-W. Luo, S.-S. Li, and L.-W. Wang*, Chinese Academy of Sciences, *Lawrence Berkeley National Laboratory

Rigorous ab initio quantum transport simulations are presented to predict the performance at the scaling limit of the mono-layer transition-metal dichalcogenide tunnel field-effect transistors (TFETs). WTe_2-TFET appears as the most promising candidate for both high-performance and low-operating-power transistors satisfying the 2024 ITRS requirements for 7nm physical gate length scaling.

10:45 a.m.

12.5 A Computational Study of van der Waals Tunnel Transistors: Fundamental Aspects and Design Challenges, J. Cao, D. Logoteta, S. Özkaya*, B. Biel**, A. Cresti, M. Pala, and D. Esseni***, IMEP-LAHC, *Aksaray University, **University of Granada, ***DIEG-IUNET

We here propose a model Hamiltonian for vdW-TFETs relying on a few physical parameters that we calibrate against DFT band structure calculations. This approach allowed us to develop a fully three-dimensional (3-D), NEGF based simulator and to investigate fundamental and design aspects related to vdW-TFETs, such as: (a) area and edge tunneling components and IDS scaling with device area; (b) impact of top gate alignment and back-oxide thickness on the device performance; (c) influence of inelastic phonon scattering on device operation and SS value; (d) benchmarking of switching energy and delay.

11:10 a.m.

12.6 Charge Transport Modelling in Organic Semiconductors: From Diodes to Transistors, Memories and Energy Harvesters (Invited), A. Di Carlo, and F. Santoni, University of Rome "Tor Vergata"

Organic semiconductor are playing an increasingly important role for the fabrication of many electronic and optoelectronic devices. In this work we will present a consistent and transferable scheme for charge transport in organic semiconductors and applications of this model to the description of diodes, resistive memories, OTFTs and OPVs.

11:35 a.m.

12.7 Understanding the Nature of Metal-Graphene Contacts: A Theoretical and Experimental Study, T. Cusati, G. Fiori, A. Gahai**, V. Passi, A. Fortunelli*, M. Lemme**, and G. Iannaccone, University of Pisa, *CNR-ICCOM, **University of Siegen

We present a theoretical and experimental study of metal- graphene contacts for different metals, and we propose and validate a simple physical model on the basis of multi-scale simulations and experiments.

Our model also allows us to predict the minimum achievable contact resistance, which is well below 100 Ωxμm.

Session 13: Sensors, MEMS, and BioMEMS – Focus Session – Silicon-based Nano-devices for Detection of Biomolecules and Cell Function
Tuesday, December 8, 9:00 a.m.
Jefferson Room
Co-Chairs: Yuji Miyahara, Tokyo Medical and Dental Univ.
Severine LeGac, University of Twente

9:05 a.m.
13.1 Ultra-Low Power Sensing Platform for Personal Health and Personal Environmental Monitoring, (Invited), V. Misra, B. Lee, P. Manickam*, M. Lim, S. Pasha*, S. Mills, S. Bhansali*, North Carolina State University and *Florida International University

The vision of the NSF Center on Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST) is to develop nano-enabled technologies to achieve a paradigm shift towards long-term health and wellness management. To achieve this, the center is building self-powered, wearable and multimodal sensing systems for correlation of environmental exposures to physiological parameters. This paper presents the latest advances in environmental and personal health sensors that have ultra-low power consumption and are highly selective and sensitive to enable real time, continuous, and wearable platforms.

9:30 a.m.
13.2 Highly Integrated CMOS Microsystems to Interface with Neurons at Subcellular Resolution (Invited), A. Hierlemann, J. Muller, D. Bakkum, F. Franke, ETH Zurich

We demonstrate that CMOS high-density microtransducer arrays featuring several thousands of transducers (e.g., >3,000 electrodes per mm^2) can be used to record from or stimulate potentially any individual neuron or subcellular compartment on the CMOS chip. High- and subcellular-resolution recordings of individual neurons and networks are presented.

9:55 a.m.
13.3 High Throughput Cell Sorter Based on Lensfree Imaging of Cells (Invited), L. Lagae, D. Vercruysse, A. Dusa, C. Liu, K. de Wijs, R. Stahl, G. Vanmeerbeeck, B. Majeed, Y. Li, and P. Peumans, imec

A novel optofluidic device for high throughput cell sorting is demonstrated. The device combines CMOS based imaging of cells in fluidic channels with sorting based on thermal bubble generation through microheaters. The throughput is 1000 cells/s per channel with potential to sort millions of cells based on dense multichannel integration

10:20 a.m.

13.4 Lensfree Microscopy: A New Framework For the Imaging of Viruses, Bacteria, Cells and Tissue (Invited), C. Allier, S. Vinjimore Kesavan*, Y. Hennequin*, O. Cioni*, F. Momey*, T. Bordy, L. Hervé, J.-G. Coutard, S. Morel, A. Berdeu, F. Navarro, and J.-M. Dinten, CEA LETI, MINATEC

Lensfree imaging is an emerging microscopy technique based on in-line holography as invented by Gabor in 1948. Albeit the existence of the method since decades, the recent development of digital sensors, helped the realization of its full potential. Over the recent years, the performance have tremendously increased while keeping the design simple, robust, and at a reasonable low cost. The detection ability improved from 10 µm (cell) in 2009, to 1 µm (bacteria) in 2010 , down to 100 nm beads in 2012, paving the way to the detection of viruses in 2013.

10:45 a.m.

13.5 Precision Mass Measurements in Solution Reveal Properties of Single Cells and Bioparticles (Invited), S. Olcum, N. Cermak, and S. Manalis, Massachusetts Institute of Technology

Micro- and nanomechanical resonators enable mass measurements of single analytes with extraordinary precision. However the performance of these devices degrades when operated in solution due to viscous loss. The suspended microchannel resonators (SMR) were developed to overcome this limitation. The SMR is a mechanical resonator comprised of a microfluidic channel running through a cantilever oscillating at its resonant frequency. As particles flow through the integrated channel, the resonant frequency of the cantilever is transiently modulated by the particle's buoyant mass, enabling precise mass measurements in solution. Here, we will discuss the recent advancements of the SMR technology that enabled the quantification of single cell growth and density, and resolving nanoparticles down to 10 nm with single attogram precision. Finally, we will present a technology for simultaneously monitoring multiple resonances that enabled high throughput growth rate measurements. We will show how the same technology can potentially determine the shape of nanoparticles along with their masses.

11:10 a.m.

13.6 Fabrication and Analysis of SiN Nanopores for Direct DNA Sequencing (Invited), I. Yanagi, R. Akahori, T. Iwasaki, Y. Goto, K. Matsui, Y. Nara, N. Manri, M. Aoki, T. Yokoi, and K.-i. Takeda, Hitachi, Ltd

This paper summarizes the latest developments of solid-state nanopores in our laboratory. For the realization of direct DNA sequencing with solid-state nanopores, a simple method to precisely fabricate nanopores with diameters of 1 to 3 nm has been developed. From the measurements of translocation events of DNA through the fabricated nanopores, it was confirmed that single-stranded DNA (ssDNA) could pass through the nanopore even when the diameter of nanopore is down to 1.2 nm. In addition, it was discovered that the translocation speed of

single-stranded DNA is faster than that of double-stranded DNA (dsDNA) by two or three orders of magnitude.

Session 14: Characterization, Reliability and Yield – Flash and Novel Device Characterization and Reliability

Tuesday, December 8, 9:00 a.m.
Lincoln Room
Co-Chairs: James Stathis, IBM Research
Jungwoo Joh, Texas Instruments

9:05 a.m.
14.1 Scalpel Soft Retrace Scanning Spreading Resistance Microscopy for 3D-carrier Profiling in sub-10nm W_{FIN} FinFET, P. Eyben, T. Chiarella, S. Kubicek, H. Bender, O. Richard, J. Mitard, A. Mocuta, N. Horiguchi, and A.V.-Y. Thean, imec vzw

Site-specific real three-dimensional (3D) carrier profiling in sub-10nm W_{FIN} devices is demonstrated for the first time. Extension-gate overlap, active dopant concentration and distribution inside extensions and epi source/drain are observed with 1nm-spatial resolution along X,Y and Z. Using this new technique providing full 3D-carrier mapping we demonstrated improved sub-10nm fin width FinFET performance.

9:30 a.m.
14.2 Tunnel Junction Abruptness, Source Random Dopant Fluctuation and PBTI Induced Variability Analysis of $GaAs_{0.4}Sb_{0.6}/In_{0.65}$ $Ga_{0.35}As$ Heterojunction Tunnel FETs, R. Pandey, N. Agrawal, V. Chobpattana*, K. Henry**, M. Kuhn**, H. Liu, M. Labella, C. Eichfeld, K. Wang, J. Maier, S. Stemmer*, S. Mahapatra***, S. Datta, The Pennsylvania State University, *University of California, Santa Barbara, **Intel Corporation, ***IIT Bombay

III-V Heterojunction TFET (HTFET) tunnel interface is characterized at 3D atomic scale resolution. Impact of tunnel junction abruptness and source RDF is explored. HTFET PBTI is evaluated with High-K-dielectrics (sub-0.8 nm-EOT HfO_2, HfO_2- ZrO_2, ZrO_2)/ III-V interfaces. HfO_2 HTFET exhibits lower PBTI over ZrO_2 HTFET and lifetime improvement over III-V FinFET.

9:55 a.m.
14.3 Understanding of BTI for Tunnel FETs, W. Mizubayashi, T. Mori, K. Fukuda, Y. Ishikawa, Y. Morita, S. Migita, H. Ota, Y. Liu, S. O'uchi, J. Tsukada, H. Yamauchi, T. Matsukawa, M. Masahara, and K. Endo, AIST

We systematically investigated the NBTI degradation of Si-channel p-type tunnel FETs (pTFETs). The NBTI degradation mechanism of pTFETs is almost the same as that of pFETs. It was clarified that the NBTI degradation of pTFETs is only caused by the trap charge and the interface state degradation located in the tunneling region near the n+ source/gate edge. Furthermore, in terms of the BTI degradation of n- and p-types TFETs, although the injection source of carrier inducing

PBTI and NBTI is different, the applying drain bias corresponding to the operation conditions has an effect on the BTI lifetime improvement in both cases of n- and p-types TFETs.

10:20 a.m.
14.4 ESD Characterization of Gate-All-Around (GAA) Si Nanowire Devices, S.-H. Chen, D. Linten, G. Hellings, A. Veloso, M. Scholz, R. Boschke, G. Groeseneken, N. Collaert, and A. Thean, imec

Gate-all-around (GAA) nanowires (NW) are a promising candidate in sub-10nm CMOS nodes because of improved channel electrostatic control. ESD reliability is strongly impacted by various process options in CMOS scaling roadmap. In this work, ESD protection devices in GAA NW architecture are studied by TLP measurements and 3D TCAD simulations.

10:45 a.m.
14.5 On and off State Hot Carrier Reliability in Junctionless High-K MG Gate-All-Around Nanowires, M. Cho, G. Hellings, A. Veloso, E. Simoen, P. Roussel, B. Kaczer, H. Arimura, W. Fang, J. Franco, P. Matagne, N. Collaert, D. Linten, and A. Thean, imec

Improved HC reliability in junctionless (JL) HK/MG nanowire is demonstrated compared to the inversion-mode (IM) nanowire, at 'on' state stress. At 'off' state stress, HC degradation in JL nanowires at a high gate oxide field is discussed. The improved SS after stress in some JL devices will be also explained.

11:10 a.m.
14.6 Structural Coordination of Rigidity with Flexibility in Gate Dielectric Films for sub-nm EOT Ge Gate Stack Reliability, C. Lu and A. Toriumi, The University of Tokyo

This paper reports a gate dielectric film design for reliability-aware as well as scalability conscious gate stacks on Ge. Initially good characteristics of Ge gate stacks do not necessarily guarantee the long-term device reliability. To overcome this big hurdle, we propose a novel concept of the rigidity control in the dielectric films with continuous random network. Ge gate stacks with initially prominent passivation and long term reliability are demonstrated experimentally. This is a new view for achieving the built-in design of gate dielectric film with reliability as well as scalability.

11:35 a.m.
14.7 Time Dependent Threshold-Voltage Fluctuations in NAND Flash Memories: From Basic Physics to Impact on Array Operation (Invited), A. Goda, C. Miccoli, and C. Monzio Compagnoni*, Micron Technology Inc., *Politecnico di Milano

Random telegraph noise (RTN) during read and charge detrapping during data retention cause the time dependent threshold-voltage fluctuations in NAND flash memories. This paper reviews and discusses the physics of the time dependent V_T fluctuations and the impact on NAND operations and reliability.

12:00 p.m.
14.8 A Single-electron Analysis of NAND Flash Memory Programming, G. Nicosia, G.M. Paolucci*, C. Monzio Compagnoni, D. Resnati, C. Miccoli*, A.S. Spinelli, A.L. Lacaita, A. Visconti*, and A. Goda*, Politecnico di Milano, *Micron Technology Inc.

We present the first single-electron analysis of the program operation of NAND Flash arrays, allowing for the first time to directly extract the statistical spread of the control-gate to floating-gate cell capacitance and of the electron leakage through the inter-gate dielectric on fully processed samples under real operating conditions.

Session 15: Process and Manufacturing Technology – Moore and More
Tuesday, December 8, 9:00 a.m.
Columbia Ballrooms 1, 2, & 5
Co-Chairs: Seiji Samukawa, Tohoku University
Mariam Sadaka, SOITEC

9:05 a.m.
15.1 Diamond-shaped Ge and $Ge_{0.9}Si_{0.1}$ Gate-All-Around Nanowire FETs with Four {111} Facets by Dry Etch Technology, Y.-J. Lee, F.-J. Hou, S.-S. Chuang*, F.-K. Hsueh, K.-H. Kao**, P.-J. Sung, W.-Y. Yuan***, J.-Y. Yao, Y.-C. Lu*, K.-L. Lin, C.-T. Wu, H.-C. Chen, B-Y Chen, G-W Huang, H.J.-H. Chen***, J-Y Li^, Y. Li*, S. Samukawa^^, T.-S. Chao*, T.-Y. Tseng*, W.-F. Wu, T.-H. Hou*, and W.-K. Yeh, National Nano Device Laboratories, *National Chiao Tung University, **National Cheng Kung University, ***National Chi Nan University, ^National Taiwan University, ^^Tohoku University

We propose a feasible pathway to scale the Ge MOSFET technology by using a novel diamond-shaped Ge and $Ge_{0.9}Si_{0.1}$ gate-all-around (GAA) nanowire (NW) FETs with four {111} facets. The device fabrication requires only simple top-down dry etching and blanket Ge epitaxy techniques readily available in mass production. The proposed dry etching process involves three isotropic/anisotropic etching steps with different Cl_2/HBr ratios for forming the suspended diamond-shaped channel. Taking advantages of the GAA configuration, favorable carrier mobility of the {111} surface, nearly defect-free suspended channel, and improved dopant activation by incorporating Si, nFET and pFET with excellent performance have been demonstrated, including an Ion/Ioff ratio exceeding 1e8, the highest ever reported for Ge- based pFETs.

9:30 a.m.
15.2 InGaAs 3D MOSFETs with Drastically Different Shapes Formed by Anisotropic Wet Etching, J. Zhang, M. Si, X.B. Lou*, W. Wu, R.G. Gordon*, and P.D. Ye, Purdue University, *Harvard University

We report a novel anisotropic wet etching based process technology for 3D InGaAs MOSFETs by simply aligning the structures along different crystal orientations to realize drastically different 3D devices including

FinFETs with nearly vertical sidewalls with record I_{ON}/I_{OFF} over 10^8 and minimum I_{OFF}~3pA/μm through barrier engineering on off-state leakage path.

9:55 a.m.
15.3 Novel Wafer-Scale Uniform Layer-by-Layer Etching Technology for Line-Edge-Roughness Reduction and Surface-Flattening of 3-D Ge Channels, Y. Morita, T. Maeda, H. Ota, W. Mizubayashi, S.-i. O'uchi, M. Masahara, T. Matsukawa, and K. Endo, AIST

We have proposed novel oxygen etching technology for Ge. Advantages of the technology are listed as follows; (a) Layer-by- layer etching realizing atomically-flat step-terrace surface. (b) Free from etch-rate variation by temperature inhomogeneity over large wafer due to very small activation energy of the etching reaction. These features are applicable for fabrication of 3-D Ge FETs.

10:20 a.m.
15.4 Gate-All-Around CMOS (InAs n-FET and GaSb p-FET) Based on Vertically-Stacked Nanowires on a Si Platform, Enabled by Extremely-Thin Buffer Layer Technology and Common Gate Stack and Contact Modules, K.-H. Goh, K.-H. Tan*, S. Yadav, Annie, S.-F. Yoon*, G. Liang, X. Gong, Y.-C. Yeo, National University of Singapore, *Nanyang Technological University

We report the first demonstration of a novel vertically stacked structure comprising InAs nanowires and GaSb nanowires, enabled by an extremely-thin (sub-150 nm) III-V buffer technology on a Si platform. This led to the realization of InAs n-FETs and GaSb p-FETs based on the stacked InAs or GaSb nanowires

10:45 a.m.
15.5 Present Status and Future Prospects of Nano-Carbon Interconnect Technologies for LSIs (Invited), Y. Awano, Keio University

Nano-carbon materials have attracted attention as promising materials to replace Cu in the next generation of Si LSI interconnects because of their high electron mobility and high electro-migration tolerance. We report on the advances and on future prospects of carbon nanotube and graphene interconnect technologies in terms of materials, processes, and types of manufacturing.

11:10 a.m.
15.6 High-Performance Photonic BiCMOS Process for the Fabrication of High-Bandwidth Electronic-Photonic Integrated Circuits, D. Knoll, S. Lischke, R. Barth, L. Zimmermann, B. Heinemann, H. Rücker, C. Mai, M. Kroh, A. Peczek, A. Awny, C. Ulusoy, A. Trusch, A. Krüger, J. Drews, M. Fraschke, D. Schmidt, M. Lisker, K. Voigt*, E. Krune*, and A. Mai, IHP, *Technical University Berlin

An advanced photonic BiCMOS process is demonstrated capable, on the receiver side, for 100 Gb/s optical line rate. Key components of this process are integrated waveguide Ge photodiodes showing more than 70 GHz bandwidth and 1 A/W responsivity, and SiGe HBTs with f_T/f_{max} values of 240/290 GHz.

11:35 a.m.
15.7 Application-Oriented Performance of RF CMOS Technologies on Flexible Substrates, J. Philippe, A. Lecavelier, M. Berthomé, J.-F. Robillard, C. Gaquière, F. Danneville, D. Gloria*, C. Raynaud**, and E. Dubois, IEMN, *STMicroelectronics, **CEA-LETI,

Ultimate-thinning-and-transfer-bonding (UTTB) of RF SOI-CMOS chips is demonstrated on plastic, metal and glass substrates. Beyond process simplicity, UTTB can be tailored to meet specific application requirements like ultra mechanical flexibility, heat dissipation, transparency while retaining same f_T/f_{max} performance and improving harmonic rejection when compared to conventional rigid SOI.

Luncheon

Tuesday, December 8, 2:20 p.m.
International Ballroom West

Luncheon Presentation: Pat Tang, VP of Product Integrity, Amazon Lab126

Every consumer electronics device we buy can be considered a bundle of competing failure mechanisms that have each taken years of research to properly risk assess. The reality in consumer electronics is that there are many more unknowns from complex system interactions and we are not afforded years of risk assessment in this highly competitive market. Product Development from concept to market in less than a year is becoming the norm. The appetite for increasing functionality in smaller and lighter devices is insatiable. We are now expecting access to cloud computing in the palm of our hands that can respond to your voice, touch gesture and your very location. What is the correct approach in ensuring reliability for a system that can fail with an unknown multitude of permutations but where engineering cost and schedule are finite?

This talk will examine a product integrity vision based on 3 technical strategies:

1. Working backwards from the customer to physics of failure
2. Design for reliability through simulation tools;
3. Development of customer-use centric standards using stress-strength analysis.

Reliability is rather opaque in the consumer electronics that we buy. This presentation aims to open the path towards a consumer electronics standard to offer integrity and transparency to the customer so that they know what they are getting.

Biography

Pat Tang joined Amazon in 2010 to lead Product Integrity and is responsible for the architectural integrity and product reliability of Amazon's Kindle Fire tablets, e-readers, Fire TV and Fire Phone products. He built teams of architectural simulation and materials testing, product reliability qualification and database field analysis for warranty cost. By using cloud-based simulation to aid design, thin, lightweight and reliable products like Kindle Fire HDX 8.9 and Kindle Paperwhite were realized.

Pat was previously at Apple where he was the reliability manager responsible for the qualification of Mac products: Macbook Pro, Macbook Air, iMac, MacPro, AppleTV and the first prototypes of iPad. Here he introduced large-scale reliability waterfalls to combine different stresses to replicate field use.

With interests in Physics and design Pat has also: designed the sensor pattern in Apple's Magic trackpad; designed and patented a semiconductor sensor for green house gases; designed power amplifier probes to perform RF measurements at wafer level; conducted theoretical and empirical research of semiconductor quantum wells for opto-electronics. Patrick holds a PhD degree in Physics from Imperial College UK and has over 30 publications.

Session 16: Power and Compound Semiconductor Devices – Focus Session – Advances in Wide Bandgap Power Devices

Tuesday, December 8, 2:15 p.m.
International Ballroom Center
Co-Chairs: David Sheridan, Alpha and Omega Semi., Inc.
Matteo Meneghini, University of Padova

2:20 p.m.
16.1 State-of-the-Art GaN Vertical Power Devices (Invited), T. Kachi, Toyota Central R&D Labs, Inc.

Development issues for fabrication of vertical GaN power devices are reviewed. Evaluation of high-quality free standing substrates, epitaxial layers having low carrier concentration and high mobility, effects of surface planarization and resultant vertical GaN power devices with high breakdown voltage will be discussed.

2:45 p.m.
16.2 200mm GaN-on-Si Epitaxy and e-mode Device Technology (Invited), D. Marcon, Y. Saripalli, and S. Decoutere, imec

In this work, three types of high-voltage buffer architectures for GaN-on-200mm Si epitaxy are compared and discussed. Recessed gate MISHEMTs and p-GaN HEMTs for e-mode are discussed. Threshold voltage/output current tuning, threshold voltage stability and possible issues are highlighted. A possible architecture that combines the best of the two approaches is proposed together with some preliminary test results.

3:10 p.m.
16.3 High-K Gate Dielectric Depletion-Mode and Enhancement-Mode GaN MOS-HEMTs for Improved OFF-state Leakage and DIBL for Power Electronics and RF Applications (Invited), H.W. Then, L.A. Chow, S. Dasgupta, S. Gardner, M. Radosavljevic, V.R. Rao, S.H. Sung, G. Yang, and P. Fischer, Intel Corporation

We have fabricated high-K dielectric enhancement- mode GaN MOS-HEMTs which show excellent DIBL and I_{OFF} at V_D=3.5V as the result of the thin T_{oxe}=23Å achieved by removing the AlInN polarization layer from the gate stack. The DIBL-vs-L_G characteristics of the high-K enhancement-mode GaN MOS-HEMT of this work is the best ever reported for a GaN transistor. Consequently, we show that an L_G=90nm e-mode high-K GaN MOS-HEMT is capable of producing a high RF Pout of 0.8W/mm with PAE=70% at V_D=4V, and 0.2W/mm with PAE=50% at low V_D=1.5V. These results make GaN attractive for energy-efficient power electronics applications such as switching voltage regulators (VR), and energy-efficient RF power amplifiers (PA).

3:35 p.m.
16.4 Renovation of Power Devices by GaN-based Materials (Invited) D. Ueda, Kyoto Institute of Technology

The research directions of GaN power devices are discussed by looking back the development history of Si power devices. Two different design approaches are proposed on the requirement of blocking voltage. Namely, scaling-down GaN FET is necessary in low-voltage applications, while resistance-reduction by introducing conductivity modulation is still effective in high-voltage ones.

4:00 p.m.
16.5 From Epitaxy to Converters Topologies what Issues for 200 mm GaN/Si? (Invited), L. Di Cioccio, E. Morvan, M. Charles, P. Perichon*, A. Torres, F. Ayel**, D. Bergogne**, Y. Baines, M. Fayolle, R. Escoffier, W. Vandendaele, D. Barranger, G. Garnier, L. Mendizabal, B. Thollin, and M. Plissonnier, CEA LETI MINATEC, *CEA LITEN, **CEA LIST

Developments of AlGaN/GaN based devices are driven by power switching applications. High quality epitaxial layer growth with GaN on 200 mm silicon substrates are the main challenges, while packaging and innovative topologies are also essential. This paper reviews the developments at CEA in power electronics, with a discussion of the issues for each area.

4:25 p.m.
16.6 Advanced Power Electronic Devices Based on Gallium Nitride (GaN) (Invited), D. Piedra, B. Lu*, M. Sun, Y. Zhang, E Matioli, F. Gao, J. Chung, O. Saadat*, L. Xia*, M. Azize*, and T. Palacios, Massachusetts Institute of Technology, *Cambridge Electronics, Inc.

This paper describes our recent work on GaN-only normally-off transistors with gate voltage swings (+/- 10 V) that make them compatible with standard Silicon gate drivers. In addition, we will discuss several novel technologies that are quickly improving the performance and lowering the cost of vertical GaN devices.

4:50 p.m.
16.7 Increasing the Switching Frequency of GaN HFET Converters (Invited), B. Hughes, R. Chu, J. Lazar, K. Boutros, HRL Laboratories LLC

This paper reviews (1) the design of 600V E-mode GaN HFET with AlN-base insulating gate, (2) the packaging and gate drive to reduce inductance for 1MHz 2.4kW 98% efficiency converter, (3) the potential of GaN power IC for 100 MHz switching.

5:15 p.m.
16.8 SiC- and GaN-based Power Devices: Technologies, Products and Applications (Invited), S. Coffa, M. Saggio, A. Patti, STMicroelectronics

Compound semiconductors (and mainly at the moment SiC and GaN) power devices have practically shown a quantum leap in the performances of power devices and the possibility to enlarge the use of power electronics at very high voltages, high temperature and high power. However, the status of SiC and GaN devices today is much less mature than that of Si power devices in terms of manufacturability, material quality, process control, cost and reliability. In this paper activities on SiC and GaN power devices at STMicroelectronics will be presented and the perspectives of a large adoption of compound semiconductors power devices highlighted.

Session 17: Circuit Device Interaction – Neuromorphic Computing Techniques
Tuesday, December 8, 2:15 p.m.
International Ballroom East
Co-Chairs: Koji Nii, Renesas
Ru Huang, Peking University

2:20 p.m.
17.1 NVM Neuromorphic Core with 64k-cell (256-by-256) Phase Change Memory Synaptic Array with On-Chip Neuron Circuits for Continuous In-Situ Learning, S. Kim, M. Ishii*, S. Lewis, T. Perri, M. BrightSky, W. Kim, R. Jordan***, G.W. Burr**, N. Sosa, A. Ray, J.-P. Han, C. Miller, K. Hosokawa*, and C. Lam, IBM T.J. Watson Research Center, *IBM Tokyo Research Lab, **IBM Research – Almaden, ***Asic North Inc.

We demonstrate a neuromorphic core with 64k-cell phase change memory (PCM) synaptic array (256 axons by 256 dendrites) with 256 on-chip neuron circuits and in-situ learning capability. On-chip neuron circuits perform leaky integration and fire (LIF) and synaptic weight update based on spike- timing dependent plasticity (STDP). 2T-1R PCM unit cell design separates LIF and STDP learning paths and

minimizes the neuron circuit size. The circuit implementation of STDP learning algorithm along with 2T-1R structure enables both LIF and STDP learning to operate asynchronously and simultaneously within a single array avoiding additional complication and power consumption associated with timing schemes. We show hardware demonstration of in-situ learning with large representational capacity enabled by large array size and analog synaptic weights of PCM cells.

2:45 p.m.

17.2 Investigation of the Potentialities of Vertical Resistive RAM (VRRAM) for Neuromorphic Applications, G. Piccolboni, G. Molas, J. M. Portal, R. Coquand, M. Bocquet*, D. Garbin, E. Vianello, C. Carabasse, V. Delaye, C. Pellissier, T. Magis, C. Cagli, M. Gely, O. Cueto, D. Deleruyelle, G. Ghibaudo**, B. De Salvo, and L. Perniola, CEA, LETI, *IM2NP , **IMEP LAHC

In this paper, we investigate for the 1st time the potentiality of the VRRAM concept for various neuromorphic applications, one synapse being emulated by one VRRAM pillar. First, basic functionality of HfO_2 based VRRAM is presented. 20ns switching time, up to 10^7 cycles and stable 200°C retention were demonstrated. Then specific analyses are made on the resistance and switching voltage variability. We demonstrate that a correlation effect exists between adjacent cycles, meaning the filament keeps a memory of its shape in the previous state, leading to reduced cycle to cycle variability. Based on this preliminary study, using compact model and circuit simulations, VRRAM are proposed for cochlea and convolutional neural network applications, showing good reliability with significant area gain with respect to planar approaches.

3:10 p.m.

17.3 Scaling-up Resistive Synaptic Arrays for Neuro-inspired Architecture: Challenges and Prospect (Invited), S. Yu, P.-Y. Chen, Y. Cao, L. Xia*, Y. Wang*, and H. Wu*, Arizona State University, *Tsinghua University

The crossbar array architecture with resistive synaptic devices is attractive for on-chip implementation of weighted sum and weight update in the neuro-inspired learning algorithms. This paper discusses the design challenges on scaling up the array size due to non-ideal device properties and array parasitics. Circuit-level mitigation strategies have been proposed to minimize the learning accuracy loss in a large array. This paper also discusses the peripheral circuits design considerations for the neuro-inspired architecture. Finally, a chip-level macro simulator is developed to explore the design trade-offs and evaluate the overhead of the proposed mitigation strategies and project the scaling trend of the architecture.

3:35 p.m.

17.4 Modeling and Implementation of Firing-Rate Neuromorphic-Network Classifiers with Bilayer $Pt/Al_2O_3/TiO_{2-x}/Pt$ Memristors, M. Prezioso, I. Kataeva*, F. Merrikh-Bayat, B. Hoskins, G. Adam, T. Sota, K. Likharev**, and D. Strukov, University of California, Santa Barbara, *DENSO CORP., **Stony Brook University

Pattern classifiers based on perceptron networks were demonstrated, for the first time, with transistor-free crossbars with integrated metal- oxide memristors. Simulations of much larger, multilayer neural network classifiers, using a data-verified model of memristor switching, showed that their classification fidelity may be on a par with the state-of-the-art software-implemented networks.

4:00 p.m.
17.5 Efficient in-memory Computing Architecture Based on Crossbar Arrays, B. Chen, F. Cai, J. Zhou, W. Ma, P. Sheridan, and W.D. Lu, University of Michigan

A new efficient in-memory computing architecture based on crossbar array is developed. The corresponding basic operation principles and design rules are proposed and verified using emerging nonvolatile devices such as very low-power resistive random access memory (RRAM). To prove the computing architecture, we demonstrate a parallel 1-bit full adder (FA) both by experiment and simulation. A 4-bit multiplier (Mult) is further obtained by a programed 2-bit Mult and 2 bit FA.

4:25 p.m.
17.6 High Density Neuromorphic System with Mo/$Pr_xCa_{1-x}MnO_3$ Synapse and NbO_2 IMT Oscillator Neuron, K. Moon, E. Cha, J. Park, S. Gi*, M. Chu*, K. Baek, B. Lee*, S. Oh, and H. Hwang, Pohang University of Science and Technology (POSTECH), *Gwangju Institute of Science and Techonology (GIST)

We report novel nanoscale synapse and neuron devices for ultra-high density neuromorphic system. By adopting a Mo electrode, the redox reaction at Mo/$Pr_xCa_{1-x}MnO_3$ (PCMO) interface was controlled which in turn significantly improve synapse characteristics such as switching uniformity, disturbance, retention and multi-level data storage under identical pulse condition. Furthermore, NbO_2 based IMT oscillator was developed for neuron application. Finally, we have experimentally confirmed the realization of pattern recognition with high accuracy using the 11k-bit Mo/PCMO synapse array and NbO_2 oscillator neuron.

4:50 p.m.
17.7 Optimized Learning Scheme for Grayscale Image Recognition in a RRAM Based Analog Neuromorphic System, Z. Chen, B. Gao, Z. Zhou, P. Huang, H. Li, W. Ma, D. Zhu, L. Liu, H.-Y. Chen*, X. Liu, and J. Kang, Peking University, *SanDisk

An analog neuromorphic system is developed based on the fabricated resistive switching memory array. A novel training scheme is proposed to optimize the performance of the analog system by utilizing the segmented synaptic behavior and is demonstrated on a grayscale image recognition.

5:15 p.m.
17.8 Gate/Source Overlapped Heterojunction Tunnel FET for non-Boolean Associative Processing with Plasticity, A. Trivedi, R.

Pandey*, H. Liu*, S. Datta*, and S. Mukhopadhyay, Georgia Institute of Technology, *Pennsylvania State University

A gate/source-overlapped HTFET (SO-HTFET) with Gaussian IDS-VGS is presented to design a single transistor distance computing cell for associative processing (AP) with reinforced learning. The application of SO-HTFET based AP to face recognition demonstrates high accuracy at 250× lower power and 100x higher density than digital CMOS based Boolean AP.

Session 18: Sensors, MEMS, and BioMEMS – M/NEMS Resonators, Sensors and Actuators
Tuesday, December 8, 2:15 p.m.
Georgetown Room
Co-Chairs: Debbie Senesky, Stanford University
Maryam Ziaei Moayed, iSono Health

2:20 p.m.
18.1 Energy-Delay Performance Optimization of NEM Logic Relay, C. Qian, A. Peschot, D. Connelly, and T.-J. King Liu, University of California, Berkeley

A methodology for optimizing the energy-delay performance of a nano-electro-mechanical relay is developed. Contrary to popular belief that structural stiffness should be minimized to achieve minimum switching energy, this work shows that the effective spring constant should be relatively large. The optimal energy-delay of an aggressively scaled NEM relay (with 5 nm contact gap as-fabricated) is presented.

2:45 p.m.
18.2 A Two-Gap Capacitive Structure for High Aspect-Ratio Capacitive Sensor Arrays, Y. Tang, and K. Najafi, University of Michigan, Ann Arbor

This paper reports a new device structure and fabrication process for achieving a small sensing gap (<5µm) and very thick (>500µm) silicon structures for high aspect-ratio capacitive sensor arrays. We demonstrate improved sensitivity by a 2-gap process, creating a small gap near the top of thick capacitive accelerometer arrays.

3:10 p.m.
18.3 Polysilicon Nanowire NEMS Fabricated at Low Temperature for Above IC NEMS Mass Sensing Applications, I. Ouerghi, M. Sansa, W. Ludurczak, L. Duraffourg, K. Benedetto, P. Besombes, T. Moffitt*, B. Adams*, D. Larmagnac*, P. Gergaud, C. Poulain, A.-I. Vidana, C. Ladner, J.-M. Fabbri, D. Muyard, G. Rodriguez, G. Rabille, O. Pollet, P. Brianceau, S. Kerdiles, S. Hentz, and T. Ernst, CEA LETI, MINATEC, *Applied Materials

In this work, we demonstrate for the first time the performance of polysilicon NEMS fabricated with a low temperature process compatible with a NEMS above IC 3D integration. Most important figures of merit feature values still competitive in comparison to mono-

crystalline NEMS: Allan deviation, quality factor (Q), Signal-to-Background ratio, Dynamic Range, yield and variability, piezoresistive and elastic properties. We found the best process window (laser annealing conditions and dopant concentration) to optimize poly-Si NEMS with excellent features compared to conventional c-Si NEMS. The goal of this study is to replace c-Si for low cost 3D integration.

3:35 p.m.
18.4 A Reliable CMOS-MEMS Platform for Titanium Nitride Composite (TiN-C) Resonant Transducers with Enhanced Electrostatic Transduction and Frequency Stability, M.-H. Li, C.-Y. Chen, and S.-S. Li, National Tsing Hua University

A reliable CMOS-MEMS platform for on-chip resonant transducer and readout circuit integration is presented in this paper with (i) well-defined etch stops and relaxed release windows for high fabrication yield, (ii) narrow transducer gaps (< 400 nm) for efficient electrostatic transduction, and (iii) novel titanium nitride composite (TiN-C) structure for dielectric charge elimination and temperature compensation. With the proposed platform, MEMS resonant transducers which exhibit low frequency drift over temperature and time, excellent electrostatic coupling, and inherent CMOS circuit integration are successfully demonstrated. Table I summarizes the performance comparison among state-of-the-art CMOS-MEMS technologies.

4:00 p.m.
18.5 Spurious Mode Suppression in SH0 Lithium Niobate Laterally Vibrated MEMS Resonators, Y.-H. Song and S. Gong, University of Illinois at Urbana Champaign

This paper reports on the first development of a spurious mode suppression technique in LN-LVRs that employs the optimized overlapping length between adjacent electrodes. Simultaneously, the device features a very high figure of merit (FoM = 220), among the highest reported for micromechanical resonators.

4:25 p.m.
18.6 Super High Frequency Lithium Niobate Surface Acoustic Wave Transducers up to 14 GHz, M. Ali Mohammad, X. Chen, Q.-Y. Xie, B. Liu, J. Conway*, H. Tian, Y.Yang, and T.-L. Ren, Tsinghua University, *Stanford University

We report superior performance $LiNbO_3$ surface acoustic wave (SAW) transducers with the smallest linewidth (30 nm) and highest resonant frequency (14 GHz). SHF (>3 GHz) SAW devices are systematically studied taking into account various substrate, design, process, and performance considerations. Device metrics are obtained and compared with other state-of-the-art research.

4:50 p.m.
18.7 Output Enhancement of Triboelectric Energy Harvester by Micro-Porous Triboelectric Layer, D. Kim, B.-W. Hwang, J.-W.

Han*, M.-L. Seol, Y. Oh, and Y.-K. Choi, Korea Advanced Institute of Science and Technology (KAIST), *NASA Ames

A micro-porous polymer film is utilized as a triboelectric layer of triboelectric energy harvester. The relationship between porosity of the triboelectric layer and output characteristics is analyzed for the first time. Experiment, modeling, and simulation based on electrodynamics are performed to investigate how the two parameters affect the output performance.

Session 19: Display and Imaging Systems – Focus Session – Flexible Hybrid Electronics
Tuesday, December 8, 2:15 p.m.
Jefferson Room
Co-Chairs: John Kymissis, Columbia University
Tina Ng, PARC Research

2:20 p.m.
19.1 Flexible Electronics for Commercial and Defense Applications (Invited), E. Forsythe, B. Leever*, M. Gordon**, R. Vaia*, D. Morton, M. Durstock*, and R. Woods***, US Army Research Laboratory, *US Air Force Research Laboratory, **Office for the Secretary of Defense and NCAT, ***Defense Threat Reduction Agency

The talk will provide an overview of flexible electronic technology and applications for the Department of Defense. The electronics topics will include the following; manufacturing thin film transistor arrays for flexible digital x-ray technology, integration of electronic components on flexible substrates for applications such as distributed media, and an overview of the flexible hybrid electronics (FHE) that combines the manufacturing integration of electronic components such as Si CMOS and the direct manufacturing of sensors on flexible substrates. FHE DOD applications includes wearable devices, physiological monitoring, medical devices, and ubiquitous sensors, to name a few.

2:45 p.m.
19.2 Materials and Design Considerations for Fast Flexible and Stretchable Electronics (Invited), Z. Ma, Y.H. Jung, J.-H. Seo, T.-H. Chang, S.J. Cho, J. Lee, and W. Zhou*, University of Wisconsin-Madison, University of Texas-Arlington

We demonstrate critical individual active and passive components that are required to form fast flexible and stretchable electronics and discuss the suitable materials and design considerations that must be satisfied in order to form various functional circuits that operate in the very high frequency regime.

3:10 p.m.
19.3 ACF Packaged Ultrathin Si-based Flexible NAND Flash Memory (Invited), D.H. Kim, H.G. Yoo, D. Joe, and K.J. Lee, Korea Advanced Institute of Science and Technology (KAIST), *Korea Institute of Machinery & Materials (KIMM)

ACF packaged ultrathin Si-based flexible NAND flash memory was demonstrated. Electrical interconnection remained stable with mechanical resilience even after the 300,000 cycles of severe repetitive bending. Finally, packaging-completed ultrathin Si-based flexible NAND flash memory was fabricated, showing stable memory operation and reliability even under harsh bending condition.

3:35 p.m.
19.4 Free Form CMOS Electronics: Physically Flexible and Stretchable (Invited), M.M. Hussain, J.P. Rojas, G.A. Torres Sevilla, A.M. Hussain, M.T. Ghoneim, A.N. Hanna, A.T. Kutbee, J.M. Nassar and M. Cruz, King Abdullah University of Science and Technology (KAUST)

We show integration strategy to rationally design materials and processes to transform advanced complementary metal oxide semiconductor (CMOS) electronics into flexible and stretchable one while retaining their high performance, energy efficiency, ultra-large-scale-integration (ULSI) density, reliability and performance over cost benefit to expand its applications for wearable, implantable and Internet-of-Everything electronics.

4:00 p.m.
19.5 Large Area Sensing Surfaces: Flexible Organic Printed Interfacing Circuits and Sensors (Invited), S. Jacob, M. Benwadih, J. Bablet, M. Charbonneau, A. Aliane, A. Plihon, and A.Revaux, University of Grenoble Alpes, CEA, LITEN

Organic Large Area Electronics has been identified as a key enabling technology for smart sensing. This paper presents the last major results on different printed organic interfacing circuits and sensors which have been integrated together to achieve an image sensor on a flexible plastic substrate, demonstrating the potential of our technology for large area sensing surfaces.

4:25 p.m.
19.6 ZnO Thin Film Transistors for More than Just Displays (Invited), H.U. Li, J.I. Ramirez, K.G. Sun, Y. Gong, Y.V. Li, and T. Jackson, Penn State University

We have fabricated ZnO thin film transistors (TFTs) on rigid and flexible substrates with characteristics well suited for displays and more general microelectronic applications. Using weak-reactant plasma enhanced atomic layer deposition (PEALD) we have fabricated single-gate, double-gate, and trilayer ZnO TFTs with good performance and stability. We have also fabricated TFTs and circuits on thin (few microns thick) solution-cast polymeric substrates that can be flexed to small radius for thousands of cycles.

4:50 p.m.
19.7 Organic Thin Film Transistors for Flexible Electronics (Invited), C. Harrison, I. Horne, M. Banach, FlexEnable

OTFTs are fundamentally the most flexible transistor technology available, offering a route to truly flexible electronic devices. OTFTs have shown substantial improvements in performance over the past 25 years with further improvements still to come. FlexEnable has demonstrated flexible, full colour OLCDs build on ultra-low cost TAC substrates. FlexEnable has shown that their OTFTs can exceed the performance of a-Si and show good performance under reliability testing.

5:15 p.m.
19.8 Flexible 2D FETs using hBN Dielectrics (Invited), N. Petrone, X. Cui, J. Hone, T. Chari, K. Shepard, Columbia University

Two-dimensional (2D) materials such as graphene and molybdenum disulfide (MoS_2) are promising for flexible electronics because of their combination of unique electrical properties and mechanical robustness. However, conventional oxides are not well matched as complementary dielectrics for 2D channel materials. We have pioneered the use of a 2D dielectric, hexagonal boron nitride (hBN), as a better alternative. In particular, we have recently demonstrated techniques to encapsulate graphene in hBN and achieve robust contacts at an etched one-dimensional edge.

Session 20: Characterization, Reliability and Yield – Transistors Aging, Variability and the Impact on Circuit Design
Tuesday, December 8, 2:15 p.m.
Lincoln Room
Co-Chairs: Stephen Ramey, Intel Corp.
Guido Sasse, NXP

2:20 p.m.
20.1 Gate-Sided Hydrogen Release as the Origin of "Permanent" NBTI Degradation: From Single Defects to Lifetimes, T. Grasser, M. Waltl, Y. Wimmer, W. Goes, R. Kosik, G. Rzepa, H. Reisinger*, G. Pobegen**, A. El-Sayed***, A. Shluger***, and B. Kaczer^, TU Wien, *Infineon Munich, **KAI, ***UCL, ^IMEC

Negative bias temperature instability (NBTI) in pMOS transistors is typically assumed to consist of a recoverable (R) and a so-called permanent (P) component. While R has been studied in great detail, the investigation of P is much more difficult due to the large time constants involved and the fact that P is almost always obscured by R. As such, it is not really clear how to measure P and whether it will in the end dominate device lifetime. We address these questions by pragmatically defining P, which allows us to collect a large amount of long-term data on both large and nanoscale devices. Our results suggest that P is considerably smaller than R, that P is dominated by oxide rather than interface traps and therefore shows a very similar bias dependence as R, and finally that P is unlikely to dominate device lifetime. Based on these results we argue that the previously suggested hydrogen-release mechanism from the gate-side of the oxide is consistent with our data

and suggest a microscopic model based on density-functional-theory (DFT) data to project the results to operating conditions.

2:45 p.m.

20.2 Off-state Self-heating, Micro-hot-spots, and Stress-induced Device Considerations in Scaled Technologies, S.O. Koswatta, N. Mavilla*, M. Bajaj*, J. Johnson*, S. Gundapaneni*, C. Scott, G. Freeman**, D. Poindexter**, P. McLaughlin**, S. Mittl*, L. Sigal, J. Warnock, N. Zamdmer**, S. Lee*, R. Wachnik**, C.-H. Lin, and E. Nowak*, IBM Research, *IBM Microelectronics, **IBM Semiconductor Research and Development Center

In this paper we show that devices in scaled technologies could undergo self-heating (SH) even in the off-state when subjected to stress conditions that would in turn adversely impact product life-time. We present a detailed methodology in analyzing the impact of off-state SH, thus preventing unintentional overstressing during product stress-screening.

3:10 p.m.

20.3 Fundamental Trade-off Between Short-Channel Control and Hot Carrier Degradation in an Extremely-thin Silicon-on-Insulator (ETSOI) Technology, S. Shin, M.A. Wahab, W. Ahn, A. Ziabari, K. Maize, A. Shakouri, and M.A. Alam, Purdue University

Effective gate control of the MOSFET channel is an essential prerequisite for the sub-20nm technologies, such as FINFET, ETSOI, NWFET, etc. Unfortunately, the short-channel control is obtained at the expense of increased lattice self- heating (T_L), much higher than the substrate temperature $T_{_Sub}$. In addition, electron temperature (T_C) rises with the increasing electric field (E) associated with the shorter channel, L_{ch}. The HCI, now a complex correlated function of T_L and T_C cannot be described by classical theories developed for bulk MOSFETs with T_L~T_{Sub}. Recently, T_L has been carefully characterized for its importance on device performance, however, a new theory of HCI that explicitly correlates HCI to self-heating is urgently needed, but not yet reported. In this paper, we (i) characterize channel and surface self-heating of a ETSOI technology as a function of channel thickness (T_{Si}) and L_{ch} using electrical and optical methods, respectively; (ii) theoretically interpret the trade-off between gate controllability and self-heating effects, (iii) correlate HCI degradation to the degree of self- heating, and (vi) find distinctive universality of HCI degradation (as a function of T_{Si} and L_{ch}) that enables a long term reliability projection. We conclude that the trade-off between HCI and channel control suggests that thinnest channel may not be optimum; and that the universality of HCI degradation would hold once self-heating is accounted for.

3:35 p.m.

20.4 Hot Carrier Aging and its Variation Under Use-Bias: Kinetics, Prediction, Impact on Vdd and SRAM, M. Duan, J. Zhang, A. Manut, Z. Ji, W. Zhang, A. Asenov*, L. Gerrer*, D. Reid***, H. Razaidi*, D. Vigar^, V. Chandra^^, R. Aitken^^, B. Kaczer**, and G.

Groseneken**, Liverpool John Moores University, *University of Glasgow, **IMEC, ***Gold Standard Simulations, ^CSR, ^^Arm

Recent works report the time exponent, 'n', of hot carrier aging (HCA) varies, challenging the lifetime prediction method based on a constant 'n'. A key advance of this work is finding the pitfalls for extracting 'n' and, for the first time, verifying the capability of predicting HCA under use-bias.

4:00 p.m.
20.5 Technology Scaling and Reliability: Challenges and Opportunities (Invited), V. Huard, F. Cacho, X. Federspiel, W. Arfaoui, M. Saliva, D. Angot, STMIcroelectronics

In this anniversary's year of Moore's law [1], CMOS technology scaling is still the fundamental driver of microprocessors industry, as defined within ITRS [2]. Among many hurdles, device reliability is becoming together with the power tremendous showstoppers. To that extent, all foundries are providing Wafer Level Reliability (WLR) measurements which allow evaluating the process capability with respect to pass/fail criteria. The corollary of Moore's law about microprocessor performance and power consumption is known as Dennard's scaling [3]. Product reliability margins are often derived from WLR trials using worst-case, Physics-Of-Failure (POF) approaches. Those margins generate both speed and power performances penalties that are worsening in advanced CMOS nodes. This paper aims to review the reliability challenges and to show that there are also plenty of opportunities to improve margins through accurate reliability modeling. First, the extensive WLR dataset published over the years is used to identify the main reliability hurdles at device level. In a second step, we will discuss the various opportunities that can exist in terms of both modeling and tools to bring up large-scale, industrial framework to manage reliability margins at product level. In a third step, recent results obtained on application cases will be shown to demonstrate the efficiency of bottom-up approach to generate improvement opportunities from existing challenges.

4:25 p.m.
20.6 Considering Physical Mechanisms and Geometry Dependencies in 14nm FinFET Circuit Aging and Product Validations, S. Pae, H.C. Sagong, M.-J. Jin, Y. Kim, C. Liu, S. Choo, J.J. Kim, H. Kim, S.-Y. Yoon, H. Nam, H. Shim, S. Park, J.-K. Park, S. Shin, and J. Park, Samsung Electronics

We report the extensive 14nm FinFET reliability characterization work and provide physical mechanisms and geometry dependencies. BTI, HCI variabilility related to # of Fin used in design along with self-heat considerations are critical for product design and qualifications. We show that along with increased AFs and optimized product HTOL stress conditions, 5-10x more efficiency in time has been achieved. In addition, external mechanical strain on Fin reliability will be discussed.

4:50 p.m.
20.7 Assessing the Impact of RTN on Logic Timing Margin Using a 32nm Dual Ring Oscillator Array, Q. Tang, and C.H. Kim, University of Minnesota

We present a novel method for characterizing the impact of RTN on logic timing margin at sub-0.5V in which a ROSC from the main array is paired with a ROSC having a similar frequency from a second array. Circuit level RTN data was collected from a 32nm test chip.

5:15 p.m.
20.8 Implications of Variability on Resilient Design (Invited), R. Aitken, V. Chandra, V. Chandra, D. Pietromonaco, ARM Research

System-on-chip designs must take into account a large number of sources of variability in order to be manufacturable with suitable yield. These are collectively known as design margins, and, broadly speaking, may be considered on two different axes: speed and span of influence. Designs must be resilient enough to accommodate fast-moving changes (such as power drops or clock jitter), but may adapt to slower moving changes (such as device aging or electromigration). The same approach also allows designs to handle static variations, such as different process corners. A variation's span of influence can be as small as a single transistor or as large as the wafer lot that a chip comes from. For the purposes of this paper, we will confine our discussion to chip level and smaller, and to non- static variations.

Session 21: Process and Manufacturing Technology – Advanced Modules and FinFET Devices
Tuesday, December 8, 2:15 p.m.
Columbia Ballrooms 1, 2, & 5
Co-Chairs: Masao Inoue, Renesas Electronics
Ilgweon Kim, Samsung Electronics Co., Ltd.

2:20 p.m.
21.1 Understanding and Mitigating High-k Induced Device Width and Length Dependencies for FinFET Replacement Metal Gate Technology, T. Ando, T. Yamashita*, S. Fan*, I. Ok*, R. Sathiyanarayanan**, R. Pandey**, S. Khan***, A. Dasgupta***, A. Madan***, Q. Yuan***, M. Chace***, P. DeHaven***, H. Bu*, and V. Narayanan, IBM T.J. Watson Research Center, *IBM Research@Albany Nanotech, **IBM SRDC@Bangalore, ***IBM SRDC @East Fishkill

We identified unique device size dependencies for FinFET Replacement Metal Gate (RMG). Choice of fill metal is important to obtain a flat V_t-W. We clarified the mechanism for V_t-L roll-up in High-k last RMG and demonstrated a flat V_t-L via optimization of High-k and MOL films based on the understanding.

2:45 p.m.
21.2 Variation Improvement for Manufacturable FINFET Technology (Invited), R. Pal, M. Togo, Y. Yong, L. Vanamurthy, S.

Muralidharan, X. Zhang, R. Carter, M. Eller, S. Samavedam, GlobalFoundries

This works examines the sources of electrical variation for FinFET technology based on silicon data from 90nm contacted poly pitch, dual-epitaxy, and RMG transistor. A simple statistical model is used to predict electrical variation based on physical variation that can be measured much earlier in the processing flow. The model is also used to define specification and control limits for physical variation to support the electrical variation specified in SPICE models. Gate stack, Junction, and Gate height variation are identified to be the key contributors to threshold voltage variation for FinFET technology. A case study is also presented on controlling gate height to the desired specification limits by improving across chip, within wafer, wafer to wafer, and lot to lot variation at multiple process steps.

3:10 p.m.
21.3 Enhanced Sub-20 nm FinFET Performance by Stacked Gate Dielectric With Less Oxygen Vacancies Featuring Higher Current Drive Capability and Superior Reliability, Y.-H. Chen, C.-Y. Chen, C.-L. Cho, C.-H. Hsieh, and Y.-C. Wu, K.-S. Chang-Liao, Y.-H. Wu, National Tsing Hua University

HK-2/HK-1 stacked dielectric was proposed as the gate dielectric for sub-20 nm FinFET technology. Compared to single HK-1 dielectric, the stacked gate dielectric exhibits superior performance in terms of improved drive current by 20~22% and increased transconductance by ~22%. The main reason accounting for the better performance, besides the higher gate capacitance by 4%, is the enhanced carrier mobility by ~33% resulting from less remote scattering due to smaller amount of charged oxygen vacancies which was physically confirmed by EELS and XPS. Owing to the reduced oxygen vacancies, from bias temperature instability and lifetime test, the stacked gate dielectric demonstrates augmented reliability as well. Most importantly, HK-1 and HK-2 are common dielectrics completely compatible with typical processes, rendering the stacked dielectric a promising one for next-generation FinFETs technology.

3:35 p.m.
21.4 Self-decomposition of SiO_2 due to Si-chemical Potential Increase in SiO_2 Between HfO_2 and Substrate –Comprehensive Understanding of SiO_2-IL Scavenging in HfO_2 Gate Stacks on Si, SiGe and SiC–, X. Li and A. Toriumi, The University of Tokyo

This work thermodynamically clarifies the scavenging in HfO_2 gate stacks and generalizes it to other substrates. The key is to pay attention to the Si chemical potential in SiO_2 interfacial layer (SiO_2-IL) significantly affected both by Si in substrate and oxygen vacancy (VO) injected from HfO_2. In addition, thanks to the more generalized understanding, we can expect the scavenging is extendable to new channel materials containing Si such as SiGe and SiC with well-controlled high-k gate stacks.

4:00 p.m.

21.5 Preferential Oxidation of Si in SiGe for Shaping Ge-rich SiGe Gate Stacks, C.-T. Chang and A. Toriumi, The University of Tokyo

The oxidation of SiGe is quite different from that of Si or Ge. By paying attention to the oxidation kinetics of SiGe, a gate stack formation guideline for SiGe is proposed. We demonstrate for the first time very good C-V characteristics on SiGe with Si-cap free passivation by direct deposition of a dielectric film, followed by an optimal post-deposition annealing (PDA).

4:25 p.m.

21.6 Ge nFET with High Electron Mobility and Superior PBTI Reliability Enabled by Monolayer-Si Surface Passivation and La-induced Interface Dipole Formation, H. Arimura, S. Sioncke, D. Cott, J. Mitard, T. Conard, W. Vanherle, R. Loo, P. Favia, H. Bender, J. Meersschaut, L. Witters, H. Mertens, J. Franco, L.-A. Ragnarsson, G. Pourtois, M. Heyns, A. Mocuta, N. Collaert, and A. Thean, imec

Monolayer-Si-passivated Ge nFETs with high electron mobility and superior PBTI reliability at 0.95-nm-EOT are demonstrated. The electron mobility is increased by optimizing the Si thickness while significant improvement in PBTI reliability is realized by band engineering using La-induced interface dipole and defect passivation using laser annealing.

4:50 p.m.

21.7 $1.5x10^{-9}$ Ωcm^2 Contact Resistivity on Highly Doped Si:P Using Ge Pre-amorphization and Ti Silicidation, H. Yu, M. Schaekers, E. Rosseel, A. Peter, J.-G. Lee*, W.-B. Song*, S. Demuynck, T. Chiarella, L.-A. Ragnarsson, S. Kubicek, J.-L. Everaert, N. Horiguchi, K. Barla, D. Kim*, A. V.-Y. Thean, N. Collaert, and K. De Meyer, imec, *Samsung

Record-low contact resistivity for n-Si, $1.5x10^{-9}$ $\Omega.cm^2$, is achieved on Si:P epitaxial layer using Ge pre-amorphization + Ti silicidation. In situ doping concentration in Si:P reaches $2x10^{21}$ cm^{-3} and dynamic surface anneal boosts P activation. In addition, low thermal stability of metal-insulator-semiconductor contact is also discussed on Si:P.

5:15 p.m.

21.8 Novel Junction Design for NMOS Si Bulk-FinFETs with Extension Doping by PEALD Phosphorus Doped Silicate Glass, Y. Sasaki, R. Ritzenthaler, Y. Kimura*, D. De Roest*, X. Shi, A. De Keersgieter, M. S. Kim, S. A. Chew, S. Kubicek, T. Schram, Y. Kikuchi, S. Demuynck, A. Veloso, W. Vandervorst, N. Horiguchi, D. Mocuta, A. Mocuta, and A. Thean, imec, *ASM

We demonstrate a NMOS Si Bulk-FinFET with extension doped by Phosphorus doped Silicate Glass (PSG). PSG provides damage free and uniform sidewall doping to fin. On current I_{ON} is improved by 20% for LG in the 30-24 nm range, with similar I_{OFF} and better DIBL compared to P ion implanted reference.

Session 22: Nano Device Technology – Steep Slope Transistors
Tuesday, December 8, 2:15 p.m.
Columbia Ballrooms 3, 4, & 6
Co-Chairs: David Esseni, University of Udine
Andreas Schenk, ETHZ

2:20 p.m.
22.1 Tunneling Field Effect Transistors: Device and Circuit Considerations for Energy Efficient Logic Opportunities (Invited), I. Young, U. Avci, and D. Morris, Intel Corporation

In this paper, N- and P- TFET device design and a survey of experimental TFET data is presented. The III-V hetero-junction TFET is most promising for achieving high TFET I_{ON} and steep SS but has challenges for experimental realization. Through circuit simulation with a TFET model it was shown that the SS must be < 53mV/dec to realize at least 50% EDYN savings vs. CMOS at iso-delay for a FO4 inverter. The TFET's symmetric ID-VDS characteristic also enables ways to improve circuits.

2:45 p.m.
22.2 First Foundry Platform of Complementary Tunnel-FETs in CMOS Baseline Technology for Ultralow-Power IoT Applications: Manufacturability, Variability and Technology Roadmap, Q. Huang, R. Jia, C. Chen, H. Zhu, L. Guo, J. Wang, J. Wang, C. Wu, R. Wang, W. Bu*, J. Kang*, W. Wang*, H. Wu*, S.-W. Lee*, Y. Wang, and R. Huang, Peking University, *Semiconductor Manufacturing International Corporation

We have first successfully manufactured Complementary Tunnel-FETs (C-TFETs) in standard 12- inch CMOS foundry. With abrupt tunnel junction consideration for superior TFET performance, technology of monolithically integrating C-TFET with CMOS is developed. Planar Si C-TFET inverter is also demonstrated, indicating a new electrical isolation requirement between neighboring devices for practical C-TFET integration on the bulk substrate. For high-volume production, the variability of C- TFETs are experimentally investigated, demonstrating an intrinsic trade-off induced by dominant variation source between performance enhancement and variability suppression in traditional TFETs, which is due to the responsible factor of band-to-band tunneling generation area. By new TFET device designs, improved performance and variability simultaneously are experimentally achieved, and the circuit-level implementation shows significant operation speed enhancement (up to 93%) and energy reduction (by 66%) at V_{DD} of 0.4V, as well as remarkably suppressed variation, indicating its great potential for ultralow power applications.

3:10 p.m.
22.3 Novel SiGe/Si Line Tunneling TFET with High I_{on} at Low V_{DD} and Constant SS, S. Blaeser, S. Glass, C. Schulte-Braucks, K. Narimani, N. von den Driesch, S. Wirths, A. Tiedemann, S. Trellenkamp, D. Buca, Q.-T. Zhao, and S. Mantl, Forschungszentrum Jülich

We present a novel SiGe/Si TFET which exploits line tunneling parallel with the gate electric field, using selective and self-adjusted silicidation and a SiGe counter doped pocket at the source, showing constant SS of ~80 mV/dec over 4 orders of magnitude Id and a high Ion = 6.7 µA/µm at V_{DD} = -0.5 V.

3:35 p.m.

22.4 Quantifying the Impact of Gate Efficiency on Switching Steepness of Quantum-Well Tunnel-FETs: Experiments, Modeling, and Design Guidelines, T. Yu, U. Radhakrishna, J.L. Hoyt, D.A. Antoniadis, Massachusetts Institute of Technology Microsystems Technology Laboratories

DC and RF characterization up to 10 GHz from RT to T = 77 K combined with detailed modeling are used for the first time in a comprehensive investigation of the impact of gate efficiency (GE) on the subthreshold swing (SS) in Quantum-well Tunnel-FETs (QWTFETs). Calibrated modeling of experimental InGaAs/GaAsSb QWTFETs based on IV, CV and RF measurements and full quantum-mechanical (QM) simulations suggest that only 55% of the gate voltage contributes to the tunneling current modulation which results in degraded switching steepness. This is due to the coupling of the tunneling junction with the MOS structure, that severely degrades the GE. The proposed model can be adapted to analyze the GE in various TFET designs, and/or to use in circuit simulation. Based on the QM simulations, design guidelines resulting up to 1.4X improved GE to ~78% in our device structure are proposed.

4:00 p.m.

22.5 Prospects for Ferroelectric HfZrOx FETs with Experimentally CET=0.98nm, SS_{for}=42mV/dec, SS_{rev}=28mV/dec, Switch-OFF <0.2V, and Hysteresis-Free Strategies, M.-H. Lee, P.-G. Chen, C. Liu, K.-Y. Chu, C.-C. Cheng, M.-J. Xie, S.-N. Liu, J.-W. Lee, S.-J. Huang, M.-H. Liao*, M. Tang**, K.-S. Li***, and M.-C. Chen***, National Taiwan Normal University, *National Taiwan University, **PTEK, ***NDL

FE-HZO FETs is experimentally demonstrated with CET=0.98nm, small hysteresis window V_T shift<0.1V, SS_{for}=42mV/dec, SS_{rev}=28mV/dec, and switch-off <0.2V. The optimum ALD process leads single monolayer SiO_x for IL and low gate leakage. The FE-HZO FETs is operated at RT and 150K beyond Boltzmann tyranny, and the extracted body factor m=0.67 and m=0.89 are for V_{DS}=0.1 and 0.5V, respectively, to confirm the NC effect. There are two proposed strategies to reach hysteresis-free, including FE-HZO/epi-Ge/Si FETs with experimentally V_T shift 3mV in hysteresis window, and 3nm-thick FE-HZO resulting hysteresis-free and sub-0.2V switching by numerical simulation.

4:25 p.m.

22.6 Sub-60mV-Swing Negative-Capacitance FinFET without Hysteresis, K.S. Li, P.-G. Chen*, T. Y. Lai, C. H. Lin, C.-C. Cheng**, C. C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao*, M. H. Lee**, M. C. Chen, J. M. Sheih, W. K. Yeh, F. L. Yang***, Sayeef Salahuddin^, and

C. Hu^, National Nano Device Laboratories, *National Taiwan University, **National Taiwan Normal University, ***Academia Sinica, ^University of California, Berkeley

We report the first Negative Capacitance FinFET. ALD $Hf_{0.42}Zr_{0.58}O_2$ is added on top of the FinFET's gate stack. The test devices have a floating internal gate that can be electrically probed. Direct measurement found the gate signal amplified by 1.6x maximum at the internal gate in agreement with the improvement factor of the subthreshold swing (from 87 to 55mV/decade). For the first time, we demonstrate that raising HfZrO ferroelectricity, through higher crystallinity by annealing at higher temperature, reduces and eliminates IV hysteresis and increases the voltage gain. These discoveries will guide future theoretical and experimental work.

4:50 p.m.
22.7 Super Steep Subthreshold Slope PN-Body Tied SOI FET with Ultra Low Drain Voltage down to 0.1V, J. Ida, T. Mori, Y. Kuramoto, T. Hori, T. Yoshida, K. Takeda, H. Kasai*, M. Okihara*, Y. Arai**, Kanazawa Institute of Technology, *LAPIS Semiconductor Co., Ltd., **High Energy Accelerator Research Org.

We propose and demonstrate a super steep Subthreshold Slope (SS) new type SOI FET with a PN-body tied structure. It has a symmetry source and drain structure. The device shows a super steep SS (<6mV/dec) over 3 decades of the drain current with an ultralow drain voltage down to 0.1V.

Session 23: Evening Panel
Tuesday, December 8, 8:00 p.m.
International Ballroom Center

Is There a Potential for a Revolution in On-chip Interconnect?

Moderator: *Paul Franzon, North Carolina State Univ.*

The lack of a scaling law for on-chip interconnect has long hampered IC performance and power scaling. The solution to date has been to add additional layers of dual damascene metal, and make most or all metal copper, i.e. add cost and complexity to the process. Have these solutions have run out of scaling head room, especially when faced with the further complexities introduced by multiple patterning? The power attributable to interconnect together with the delay contribution of even medium length wires, make a better solution even more important.

In this panel we explore the scaling headroom for the "conventional solution" as well as alternatives. Can adding layers and using sophisticated design techniques solve the problem? Or is there an emerging nanotechnology enabled solution? Alternatively, putting active devices in the interconnect could lead to substantial relief. Another possible solution is the exploitation of high density monolithic or multilithic 3DIC technologies.

This panel will be conducted “Presidential debate” style, with each candidate making timed opening statements, followed by answering a series of questions with timed responses. And at the end you get to vote!

Candidates:

The Incumbent:
Rod Augur, GlobalFoundries
We can design around it:
John Wilson, nVidia
Nano/novel materials or devices to the rescue:
Azad Naeemi, Georgia Tech
Active Interconnect:
Toshi Sakamoto, NEC
Monotlithic 3D:
Maude Vinet, CEA
Multilithic 3D:
Paul Enquist, Ziptronix

Session 24: Evening Panel
Tuesday, December 8, 8:00 p.m.
International Ballroom East

Emerging Devices – Will They Solve the Bottlenecks of CMOS?

Moderator: *Heike Riel, IBM Research*

Si CMOS is an unprecedented success story of technology – the ability to scale Si CMOS FETs to ever-smaller dimensions has been the primary driver of the tremendous progress in information technology over many years. Si CMOS based technologies have completely disrupted and transformed our lives. Already for a while pure scaling-down of device dimensions has been insufficient, and new innovative solutions such as strain, new materials like high-k gate dielectrics, and new device architectures such as FinFETs have been successfully introduced to further push the limits. Even with these innovations, we are coming closer to the end of our ability to scale Si CMOS, and new solutions are urgently required to solve the power-performance challenge. But what are the most critical bottlenecks Si CMOS faces right now and how can they be solved?

A number of novel materials and switches have been proposed as replacements of Si CMOS FETs and are being investigated in various focused research programs worldwide. Carbon nanotubes and perhaps 2D materials promise to enable scaling FETs to even smaller dimensions, achieving lower operation voltages compared to Si and III-V MOSFETs. A more radical reduction in operation voltage and power consumption requires changing the physics of the underlying devices in a way that directly impacts power dissipation. So-called steep-slope devices such as tunnel FETs, negative capacitance FETs, and devices based on gating of a phase transition potentially offer the desired abrupt switching characteristics. Magnetic and spin-based devices may offer another possibility to greatly reduce the energy dissipation of switching. A lot of research has been already performed in recent years including efforts taken for device benchmarking, and potential benefits and challenges assessed. However, still we are not yet able to decide on the next switch to solve the power-performance problem. Do the new technologies solve that problem? Are we going in the right

direction? Just as importantly, what are the bottlenecks that these new technologies carry with them, some of which are considerable?

The objectives of this panel are to provide a perspective on the following:

1. Are the device physics, device structures, materials, challenges and prospects of the emerging devices sufficiently understood? What is needed to select a winner among the emerging device options?
2. Do the emerging devices solve the real problems Si CMOS is facing today?
3.

The panel will explore some key questions such as:

- What are the most important bottlenecks of CMOS? How can they be solved?
- What are the most promising emerging devices and what is their status?
- Is it a challenge of physics or of device and materials engineering?
- Will the emerging devices really solve the bottlenecks CMOS is facing?
- Which switching device will win and why? Is there a winner already on the horizon?

Panelists:

Supriyo Bandyopadhyay, Virginia Commonwealth Univ.
Wilfried Haensch, IBM Research
Adrian Ionescu, EPFL
Carlo Reita, CEA-LETI
Sayeef Salahudin, UC Berkeley
Frank Schwierz, Technical University of Illmenau

Session 25: Circuit Device Interaction – More than Moore – Value Added Technologies
Wednesday, December 9, 9:00 a.m.
International Ballroom West
Co-Chairs: Maarten Vertregt, NXP
John Hu, nVIDIA

9:05 a.m.
25.1 MTJ Based “Normally-off Processors” with Thermal Stability Factor Engineered Perpendicular MTJ, L2 Cache Based on 2T-2MTJ Cell, L3 and Last Level Cache Based on 1T-1MTJ Cell and Novel Error Handling Scheme, K. Ikegami, H. Noguchi, S. Takaya, C. Kamata, M. Amano, K. Abe, K. Kushida, E. Kitagawa, T. Ochiai, N. Shimomura, D. Saida, A. Kawasumi, H. Hara, J. Ito, and S. Fujita, Toshiba Corporation

MTJ based cache memory is expected to reduce processor power significantly. However, write energy increases rapidly for high speed operation and not suited for upper level cache memory. In this work,

we have developed L2 and L3 cache memory based on thermal stability factor engineered pMTJ with 2T2MTJ and 1T1MTJ memory cell and novel error handling scheme. With these techniques, CPU power and chip area can be reduced 65 % and 37 % compared to conventional SRAM based CPU.

9:30 a.m.

25.2 High Performance Passive Devices for Millimeter Wave System Integration on Integrated Fan-Out (InFO) Wafer Level Packaging Technology, C.-H. Tsai, J.-S. Hsieh, W.-H. Lin, L.-J. Yen, J.-N. Hung, T.-H. Peng, H.-C. Wang, C.-Y. Kuo, I. Huang, W. Chu, Y.-Y. Lei, C.H. Yu, L.C. Sheu, C.-H. Hsieh, C.S. Liu, K.-C. Yee, C.-T. Wang, and D. Yu, Tawain Semiconductor Manufacturing Company

High performance passive devices for millimeter wave (MMW) system, including inductor, ring resonator, power combiner, coupler, balun, transmission line, and antenna, are realized for the first time using Integrated Fan-Out (InFO) wafer level Packaging technology. These devices enable low noise and power MMW system for mobile communication and IoT applications.

9:55 a.m.

25.3 A 3/5 GHz Reconfigurable CMOS Low-Noise Amplifier Integrated with a Four-Terminal Phase-Change RF Switch, R. Singh, G. Slovin, M. Xu, A. Khairi, S. Kundu*, T.E. Schlesinger**, J.A. Bain, and J. Paramesh, Carnegie Mellon University, *Intel Corporation, **John Hopkins University

We present a robust realization of a reconfigurable 3/5 GHz LNA designed and fabricated in a 0.13 μm CMOS process and flip-chip integrated with a four-terminal PC switch fabricated using an in-house process. Detailed measurement results are presented to show minimal performance degradation from the overheads of the flip-chip integration.

10:20 a.m.

25.4 Low-Cost and TSV-free Monolithic 3D-IC with Heterogeneous Integration of Logic, Memory and Sensor Analogy Circuitry for Internet of Things, T.-T. Wu, C.-H. Shen, J.-M. Shieh, W.-H. Huang, H.-H. Wang, F.-K. Hsueh, H.-C. Chen, C.-C. Yang, T.-Y. Hsieh, B.-Y. Chen, Y.-S. Shiao, C.-S. Yang, G.-W. Huang, K.-S. Li, T.-J. Hsueh, C.-F. Chen*, W.-H. Chen*, F.-L. Yang**, M.-F. Chang*, W.-K. Yeh, National Nano Device Laboratories, *National Tsing Hua University, **Academica Sinica

For the first time, a CO_2 far-infrared laser annealing (CO_2-FIR-LA) technology was developed as the activation solution to enable highly heterogeneous integration without causing device degradation for TSV-free monolithic 3DIC. This process is capable to implement small-area-small-load vertical connectors, gate-first high-k/metal gate MOSFETs and non-Al metal inter-connects. Such a far-infrared laser annealing exhibits excellent selective activation capability that enables performance-enhanced stacked sub-40nm UTB-MOSFETs (Ion-enhanced over 50 %). Unlike TSV-based 3D-IC, this 3D Monolithic IC

enables ultra-wide-IO connections between layers to achieve high bandwidth with less power consumption. A test chip with logic circuits, 6T SRAM, ReRAM, sense amplifiers, analog amplifiers, gas sensors was integrated to confirm the superiority in heterogeneous integration of proposed CO_2-FIR-LA technology. This chip demonstrates the most variable functions above reported 3D Monolithic ICs. This CO2-FIR-LA based TSV-free 3D Monolithic IC can realize low cost, small footprint, and highly heterogeneous integration for Internet of Things.

10:45 a.m.
25.5 New Devices for Internet of Things: A Circuit Level Perspective (Invited), W. Dehaene, and A. Verhulst*, KULeuven, *imec

This paper discusses new devices for internet of things circuits from a design point of view. When is a new device a good device for IoT? This question is answered in terms of the energy versus delay trade off inherent to logic circuit design. Also other required features are discussed.

11:10 a.m.
25.6 Robust and Compact Key Generator Using Physically Unclonable Function Based on Logic-Transistor-Compatible Poly-Crystalline-Si Channel FinFET Technology, S. O'uchi, Y. Liu, Y. Hori, T. Irisawa, H. Fuketa, Y. Morita, S. Migita, T. Mori, T. Nakagawa, J. Tsukada, H. Koike, M. Masahara, and T. Matsukawa, AIST

This paper presents a robust and compact SRAM PUF cell using a polycrystalline-Si FinFET, for the first time. The polycrystalline-Si PUF cell improves the intra-PUF hamming distance to 1/3.4 of that of the crystalline-Si cell. A newly defined noise margin for SRAM PUFs is proposed for this analysis.

11:35 a.m.
25.7 An Integrated Silicon Photonics Technology for O-band Datacom, N. Feilchenfeld, F. Anderson, T. Barwicz*, S. Chilstedt, Y. Ding, J. Ellis-Monaghan, D. Gill*, C. Hedges, J. Hofrichter*, F. Horst*, M. Khater*, E. Kiewra*, R. Leidy*, Y. Martin*, K. McLean, M. Nicewicz, J. Orcutt*, B. Porth, J. Proesel*, C. Reinholm*, J. Rosenberg*, W. Sacher*, A. Stricker*, C. Whiting*, C. Xiong*, A. Agrawal*, F. Baker*, C. Baks*, B. Cucci, D. Dang, T. Doan, F. Doany*, S. Engelmann*, M. Gordon, E. Joseph*, J. Maling, S. Shank, X. Tian, C. Willets, J. Ferrario, M. Meghelli*, F. Libsch*, B. Offrein*, W.Green*, and W. Haensch*, IBM Systems & Technology Group, Microelectronics Division, *IBM Research GmbH

We present a manufacturable platform of CMOS, RF and optoelectronic devices, fully PDK-enabled to demonstrate a 4x25 Gb/s reference design. With self-aligned fiber attach, this technology enables low-cost O-band datacom transceivers. In addition, this technology can offer enhanced performance and yield in hybrid-assembly for applications at 25 Gbaud and beyond.

12:00 p.m.

25.8 150 GHz F_{MAX} with High Drain Beakdown Voltage Immunity by Multi Gate Oxide Dual Work-Function (MGO-DWF)-MOSFET, T. Miyata, H. Tanaka, K. Kagimoto, M. Kamiyashiki, M. Kamimura, A. Hidaka, M. Goto, K. Adachi, A. Hokazono, T. Ohguro, K. Nagaoka, Y. Watanabe, S. Hirooka, Y. Ito, S. Kawanaka, and K. Ishimaru, Toshiba Corporation

We propose Multi Gate Oxide Dual Work-Function (MGO- DWF)-MOSFET with asymmetric LV-source/HV-drain junctions. This distinctive structure enables high F_{MAX}, in other words, reducing DC operation currents could be achieved at given operation point compared with Cascode MOSFETs. This result indicates that MGO-DWF-MOSFET is strong candidate for low power AB-class RF PA.

Session 26: Memory Technology – MRAM, DRAM, and SRAM
Wednesday, December 9, 9:00 a.m.
International Ballroom Center
Co-Chairs: Jea-Gun Park, Hanyang University
Hiroki Koike, Tohoku University

9:05 a.m.

26.1 Fully Functional Perpendicular STT-MRAM Macro Embedded in 40 nm Logic for Energy-efficient IOT Applications, Y. Lu, T. Zhong*, W. Hsu, S. Kim, X. Lu, J.J. Kan, C. Park, W.-C. Chen, X. Li, X. Zhu, P. Wang, M. Gottwald, J. Fatehi, L. Seward, J. Kim, N. Yu, G. Jan*, J. Haq*, S. Le*, Y.J. Wang*, L. Thomas*, J. Zhu*, H. Liu*, Y.-J. Lee*, R.Y. Tong*, K. Pi*, D. Shen*, R. He*, Z. Teng*, V. Lam*, R. Annapragada*, T. Torng*, S.H. Kang, P.-K. Wang*, Qualcomm Technologies, Inc., *TDK-Headway Technologies, Inc.

We present a fully functional embedded 40 nm perpendicular STT-MRAM macro (1 Mb, ×32/×64 IO). We achieved 20 ns read access time and 20 ns write cycle time. The full macro was switched reliably with a 6 ns write pulse at ~ 3.2 µW/Mbps, the lowest eNVM write power reported.

9:30 a.m.

26.2 Systematic Optimization of 1 Gbit Perpendicular Magnetic Tunnel Junction Arrays for 28 nm Embedded STT-MRAM and Beyond, C. Park*, J. Kan*, C. Ching, J. Ahn, L. Xue, R. Wang, A. Kontos, S. Liang, M. Bangar, H. Chen, S. Hassan, M. Gottwald*, X. Zhu*, S. Kang*, and M. Pakala, Applied Materials, Inc, *Qualcomm Technologies Inc.

This paper demonstrates the co-optimization of all critical device parameters of perpendicular magnetic tunnel junctions (pMTJ) in 1 Gbit arrays with an equivalent bitcell size of 22 F^2 at the 28 nm logic node for embedded STT-MRAM. Through thin film tuning and advanced etching of sub-50 nm (diameter) pMTJ, high device performance and reliability were achieved simultaneously, including TMR = 150 %, H_c > 1350 Oe, H_{off} < 100 Oe, Δ = 85, I_c (35 ns) = 94

μA, $V_{breakdown}$ = 1.5 V, and high endurance (> 1E12 write cycles). Reliable switching with small temporal variations (< 5 %) was obtained down to 10 ns. In addition, tunnel barrier integrity and high temperature device characteristics were investigated in order to ensure reliable STT-MRAM operation.

9:55 a.m.
26.3 STT-MRAM with Double Magnetic Tunnel Junctions, G. Hu, J. H. Lee*, J.J. Nowak, J.Z. Sun, J. Harms, A. Annunziata, S. Brown, W. Chen, Y. H. Kim*, G. Lauer, L. Liu, N. Marchack, S. Murthy, E. J. O'Sullivan, J. H. Park*, M. Reuter, R. P. Robertazzi, P. L. Trouilloud, Y. Zhu**, and D.C. Worledge, IBM-Micron MRAM Alliance, *IBM-Samsung MRAM Alliance, **IBM TJ Watson Research Center

We report 2x improvement of switching efficiency in perpendicularly magnetized Spin-Transfer Torque MRAM devices with double tunnel barriers, compared to single tunnel barrier stacks. Switching efficiency up to 10 $k_BT/\mu A$ was observed. A large operating window, $V_{breakdown}$-V_{c10ns} ~ 0.7 V was achieved compared to 0.2V in single tunnel barrier devices.

10:20 a.m.
26.4 Solving the Paradox of the Inconsistent Size Dependence of Thermal Stability at Device and Chip-level in Perpendicular STT-MRAM, L. Thomas, G. Jan, S. Le, Y.-J. Lee, H. Liu, J. Zhu, S. Serrano-Guisan, R.-Y. Tong, K. Pi, D. Shen, R. He, J. Haq, Z. Teng, R. Annapragada, V. Lam, Y.-J. Wang, T. Zhong, T. Torng, and P.-K. Wang, TDK Headway Technologies Inc

We report that data retention of perpendicular STT-MRAM chips exhibits substantial size dependence for devices between 55 and 100 nm, contrary to the widespread belief that thermal stability depends weakly on diameter above ~30 nm. We show that the conventional method of measuring thermal stability is inaccurate at these sizes.

10:45 a.m.
26.5 20nm DRAM: A New Beginning of Another Revolution (Invited), J. Park, Y.S. Hwang, S.-W. Kim, S.Y. Han, J.S. Park, J. Kim, J. W Seo, B.S. Kim, S.H. Shin, C.H. Cho, S.W. Nam, H.S. Hong, K.P. Lee, G.Y. Jin, and E.S. Jung, Samsung Electronics Co.

For the first time, 20nm DRAM has been developed and fabricated successfully without EUV lithography using the honeycomb structure and the air-spacer technology. These low-cost and reliable schemes are promising key technologies for 20nm technology node and beyond.

11:10 a.m.
26.6 Gate-first High-k/Metal Gate DRAM Technology for Low Power and High Performance Products, M. Sung, S.-A. Jang, H. Lee, Y.-H. Ji, J.-I. Kang, T.-O Jung, T.-H. Ahn, Y-I. Son, H.-C. Kim, S.-W. Lee, S.-M. Lee, J.-H. Lee, S.-B. Baek, E.-H. Doh, H.-J. Cho, T.-Y. Jang, I.-S. Jang, J.-H. Han, K.-B. Ko, Y.-J. Lee, S.-B. Shin, J.-S. Yu, S.-H. Cho, J.-H. Han, D.-K. Kang, J. Kim, J.-S. Lee, K.-D. Ban, S.-J.

Yeom, H.-W. Nam, D.-K. Lee, M.-M. Jeong, B. Kwak, J. Park, K. Choi, S.-K. Park, N.-J. Kwak, and S.-J. Hong, SK hynix

Fully integrated and functioned DRAM using High-K Metal Gate technology at peripheral transistor is implemented for the first time. Several processes were used for cost effective DRAM technology. Optimized DRAM high-k metal gate peripheral transistors show Iop gain of 65%/55% for NMOS and PMOS, respectively.

11:35 a.m.
26.7 A Novel Bi-stable 1-Transistor SRAM for High Density Embedded Applications, J.-W. Han, B. Louie, N. Berger, V. Abramzon, S. Lai, Z. Or-bach, P. Lee*, R. Chang*, W. Lee*, Y. Nishi**, Y. Widjaja, Zeno Semiconductor, *Marvell Seemiconductor, Inc., **Stanford University

A 1-transistor SRAM on bulk substrate is presented. The device is fabricated in 28 nm foundry baseline process with an additional buried N-well (BNWL) implant. The unit cell consists of a lateral MOS for access and intrinsic vertical open-base bipolar structures for self-latch function. The bit cell operation and the disturb immunity are verified at high temperature. Using 28 nm design rules, a cell size of 0.025 μm^2 is achieved, offering 80% cell size reduction over 6T-SRAM and providing comparable power and performance.

12:00 p.m.
26.8 Evidence of Single Domain Switching in Hafnium Oxide Based FeFETs: Enabler for Multi-Level FeFET Memory Cells (Late News), H. Mulaosmanovic, S. Slesazeck, J. Ocker, M. Pesic, S. Müller, S. Flachowsky***, J. Müller*, P. Polakowski*, J. Paul***, S. Jansen***, S. Kolodinski***, C. Richter, S. Piontek, T. Schenk, A. Kersch^, C. Künneth^, R. van Bentum***, U. Schröder, T. Mikolajick**, NaMLab gGMBH, *Fraunhofer IPMS-CNT, **IHM TU-Dresden, ***GlobalFoundries, ^HAW-München, ^^ NaMLab gGMBH and Politecnico Di Milano

Recent discovery of ferroelectricity in HfO_2 thin films paved the way for demonstration of ultra-scaled 28 nm Ferroelectric FETs (FeFET) as non-volatile memory (NVM) cells [1]. However, such small devices are inevitably sensible to the granularity of the polycrystalline gate oxide film. Here we report for the first time the evidence of single ferroelectric (FE) domain switching in such scaled devices. These properties are sensed in terms of abrupt threshold voltage (V_T) shifts leading to stable intermediate V_T levels. We emphasize that this feature enables multi-level cell (MLC) FeFETs and gives a new perspective on steep subthreshold devices based on ferroelectric HfO_2.

Session 27: Nano Device Technology – Focus Session – Layered 2D Materials and Devices: From Growth to Applications
Wednesday, December 9, 9:00 a.m.
International Ballroom East
Co-Chairs: Aaron Franklin, Duke University
Joerg Appenzeller, Purdue University

9:05 a.m.

27.1 The Challenging Promise of 2D Materials for Electronics (Invited), G. Fiori and G. Iannaccone, University de Pisa

In this work we will critically discuss the advantages and the drawbacks of two-dimensional materials (2DMs) for applications in electronics. We will show that 2DMs hold promises for end-of-the-roadmap devices. Many open questions still remain open, which can be addressed through detailed atomistic device simulations.

9:30 a.m.

27.2 Epitaxial CVD Growth of High-Quality Graphene and Recent Development of 2D Heterostructures (Invited), H. Ago, Y. Okagawa, K. Kawahara, Y. Ito, B. Hu, C. Orofeo, P. Fernández, H. Endo, H. Hibino*, S Mizuno, K. Tsukagoshi**, and M. Tsuji, Kyushu University, *Kwansei Gakuin University and NTT-Research Laboratory, **National Institute for Materials Science (NIMS)

The concept and results of our original "epitaxial CVD" approach are presented. By using Cu(111) on sapphire, the orientation of the hexagonal lattice of graphene is controlled. Influences of grain structure and grain boundaries on the transport property are discussed. Integration with other 2D materials will also be presented.

9:55 a.m.

27.3 2D Layered Materials: From Materials Properties to Device Applications (Invited), P. Zhao, S. Desai, M. Tosun, T. Roy, H. Fang, A. Sachid, M. Amani, C. Hu, and A. Javey, University of California, Berkeley

With an ever growing interest in the layered 2D semiconductors, the research community has extensively explored the optical, material, and electronic aspects of these materials and their application towards devices. Here, we present an overview of 2D electronic devices with emphasis on the relevant material properties for device applications such as heterostructure band alignments, unique device architectures, and scaling advantages. In addition, important advancements in doping, contact engineering, strain, high performance FETs, all-2D FETs, heterostructures, and novel tunneling devices are summarized.

10:20 a.m.

27.4 High-frequency Scaled MoS_2 Transistors (Invited), D. Krasnozhon, S. Dutt, C. Nyffeler, Y. Leblebici, and A. Kis, École Polytechnique Fédérale de Lausanne (EPFL)

We present scaled high-frequency trilayer MoS_2 FETs with improved characteristics. It has been shown that for 2D graphene based devices f_T exhibits a 1/L trend, while f_{MAX} has a nonmonotonic behavior with the decreasing channel length, reaching a peak value around 200 nm. In contrast to graphene, MoS_2 has a bandgap which makes it easier to reach current saturation. As a consequence, for both f_T and f_{MAX} we are able to see the typical 1/L behavior down to 40 nm. In addition, the

existence of the band gap in MoS_2 FETs allows us to observe voltage gain for all our devices.

10:45 a.m.
27.5 Bandgap Engineering in 2D Layered Materials (Invited), T. Chu, and Z. Chen*, GlobalFoundries Advanced Technology, *Purdue University

Bandgap engineering to design new semiconductors through growth process is an important technique for the optoelectronic field. Here, we demonstrate widely tunable bandgaps by electric field in 2D layered materials. A bandgap of 200meV is opened in bilayer graphene and the same can be largely reduced in bilayer MoS_2.

11:10 a.m.
27.6 van der Waals Junctions of Layered 2D Materials for Functional Devices (Invited), T. Machida, R. Moriya, M. Arai, Y. Sata, T. Yamaguchi, N. Yobuki, S. Morikawa, S. Masubuchi, and K. Ueno*, University of Tokyo, *Saitama University

We demonstrate that van der Waals junctions of graphene and 2D materials work as functional devices: (i) Graphene/MoS_2/metal vertical FET with large current modulation exceeding 10^5 ON-OFF current ratio simultaneously with a large ON current density of 10^4 A/cm^2; (ii) $Fe_{0.25}TaS_2$/$Fe_{0.25}TaS_2$ vdW magnetic tunnel junctions; (iii) $NbSe_2$/$NbSe_2$ vdW Josephson junctions.

11:35 a.m.
27.7 Roll-to-Roll Synthesis and Patterning of Graphene and 2D Materials (Invited), T. Choi, S.J. Kim, S. Park, T. Hwang*, Y. Jeon*, and B.H. Hong, Seoul National University, *Samsung-Electro Mechanics

Graphene has been intensively studied due to their outstanding electrical, mechanical and optical properties, such as high electrical conductivity, mechanical flexibility, and optical transmittance. The key challenges to make commercially viable graphene-based electronic devices are enabling large-area production of high quality graphene and subsequently patterning graphene into desirable structures. With the recent advances in chemical vapor deposition (CVD), large-area growth of graphene by CVD on Cu substrates was successfully demonstrated for industrial applications. However, reliable methods are still required to transfer the large-area graphene sheet to the application substrate and pattern for the desired applications without damaging or leaving undesired residues on the graphene surface. As for the graphene transfer, the wet transfer method using a support layer such as poly(methyl methacrylate) (PMMA) is typically used but generally difficult to scale up, and the surface tension experienced by the floating graphene at the air-water interface causes rippling, rolling, and break of the films during transfer. The complete removal of PMMA residues is also problematic and most of flexible substrates are either dissolved in acetone or cannot withstand the annealing temperature; thus, graphene can only be transferred to a limited number of flexible substrates. On the other hands, the transfer method using a thermal release tape (TRT)

is easy to transfer large-area graphene onto flexible or rigid substrates, but inevitably contaminates the transferred graphene with the adhesive from the TRT film. The adhesion of polymer supports (i.e., PMMA and TRT) to the graphene mainly depends on the chemical adhesion of the polymer film. The residual PMMA or adhesive left on the graphene surface is inevitable. Unlike the adhesive-based transfer mechanism such as PMMA or TRT, a dispersive adhesion-based transfer methods have been demonstrated including the work by Allen, M. J. et al. using a soft PDMS stamp. The transfer mechanism there was based on the difference in dispersive adhesion at the PDMS-graphene and graphene-substrate interfaces. For most materials, the PDMS interface is weaker than the substrate interface, due to the extremely low surface energy of PDMS.

Session 28: Modeling and Simulation – Compact Modeling
Wednesday, December 9, 9:00 a.m.
Georgetown Room
Co-Chairs: Denis Rideau, STMicroelectronics
Chung-Cheng Wu, TSMC

9:05 a.m.
28.1 Transport Mechanism in sub 100ºC Processed High Mobility Polycrystalline ZnO Transparent Thin Film Transistors, P.B. Pillai, and M.M. De Souza, University of Sheffield

We demonstrate high performance ZnO TFTs with record field effect mobility >62 cm^2/V.s, on/off ratio exceeding 10^7 (limited only by our simple device structure) and sub threshold swing (S) <150 mV/dec, surpassing the performance of many reported amorphous Indium Gallium Zinc Oxide (a- IGZO) thin film transistors.[1,2] The tail state distribution of the density of states (DOS) in ZnO extracted via 2D numerical simulations matched to experiment, demonstrates unequivocally a similar mobility mechanism that underpins all Transparent Conducting Oxides (TCOs)-whether amorphous or not. The upper bound of the characteristic Temperature of ZnO averaged over the data from different four devices is found to be 379±14 K and the tail state density of states (DOS) is (3.8±0.35) $\times 10^{20} cm^{-3} eV^{-1}$.

9:30 a.m.
28.2 Physical-based Analytical Model of Flexible a-IGZO TFTs Accounting for Both Charge Injection and Transport, M. Ghittorelli, F. Torricelli, J.L. Van Der Steen*, C. Garripoli**, A. Tripathi*, G. Gelinck*, E. Cantatore**, Z. Kovacs-Vajna, University of Brescia, *Holst Centre, TNO, **Eindhoven University of Technology

We show a new physical-based analytical model of a-IGZO TFTs. TFTs scaling from L=200µm to L=15µm and fabricated on plastic foil are accurately reproduced with a unique set of parameters. The model is used to design a zero-VGS inverter. It is a valuable tool for circuit design and technology characterization.

9:55 a.m.
28.3 Predictive Compact Modeling of Random Variations in FinFET Technology for 16/14nm Node and Beyond, X. Jiang, X.

Wang*, R. Wang, B. Cheng**, A. Asenov*, and R. Huang, Peking University, *University of Glasgow, **Gold Standard Simulations (GSS) Ltd.

Predictive compact models for two key variability sources in FinFET technology, the gate edge roughness (GER) and Fin edge roughness (FER), are proposed for the first time, and integrated into industry standard BSIM-CMG core model. Excellent accuracy and predictivity is verified through atomistic TCAD simulations. The inherent correlations between the variations of device electrical parameters are well captured. In addition, an abnormal non-monotonous dependence of variations on Fin-width is observed, which can be explained with the newly found correlation between random variations and electrostatic integrity in FinFETs. The impacts of GER and FER on circuits are efficiently predicted for 16/14nm node and beyond, providing helpful guildlines for variation-aware design and technology process development.

10:20 a.m.
28.4 A New Surface Potential Based Physical Compact Model for GFET in RF Applications, L. Wang, S. Peng, Z. Zong, L. Li, W. Wang, G. Xu, N. Lu, Z. Ji, Z. Jin, and M. Liu, Chinese Academy of Sciences

In this work, we develop a surface potential based physical compact model of GFET for RF applications. The model results closely match the measurements. Furthermore, Ring Oscillator and Mixer circuit are stimulated and a mixer with high conversion gain and IIP3 can be obtained, which is instructive to RF circuit design.

10:45 a.m.
28.5 Physics-based Compact Modeling Framework for State-of-the-Art and Emerging STT-MRAM Technology, N. Xu, J. Wang, Y. Lu, H.-H. Park, B. Fu, R. Chen, W. Choi, D. Apalkov, S. Lee*, S. Ahn*, Y. Kim*, Y. Nishizawa**, K.-H. Lee, Y. Park, E.S. Jung*, Samsung Semiconductor Inc, *Samsung Electronics, **Samsung R&D Institute Japan

A physics-based compact model framework including both charge transport and magnetic dynamics has been developed in order to capture the feature of state-of-the-art STT-MRAM technology. After validation with numerical simulations and 15nm-MRAM experiments, simulation studies are performed on evaluating the various transistor/MRAM cell designs. SOT-assisted MRAMs are found to provide significant benefits in minimizing switching delays and variability as compared to conventional STT-MRAMs.

11:10 a.m.
28.6 Physics-based Compact Modeling of Charge Transport in Nanoscale Electronic Devices (Invited), S. Rakheja, and D. Antoniadis*, New York University, *Massachusetts Institute of Technology

Physics-based compact models of transistors play two complementary roles. First, they establish an analytical mathematical description of the device, which helps interpret measurements or detailed simulations and make predictions; second, they form the basis of models used in circuit simulators. More recently, as silicon MOSFETs started approaching quasi-ballistic (QB) operation and new channel materials have emerged, interest has shifted back to physics-based models for exploring the limits of nanoscale FET performance. In this paper, we argue that the key to the usefulness of physics-based compact models is strict minimization of the number of model parameters, while still maintaining the capability to embed the model in a circuit simulator. We do this by using the Virtual Source compact model for FETs and its adaptation to materials beyond silicon as example.

Session 29: Sensors, MEMS, and BioMEMS – Devices for In Vitro Bioanalytics and In Vivo Monitoring
Wednesday, December 9, 9:00 a.m.
Jefferson Room
Co-Chairs: Carlotta Guiducci, Ecole Poly. Fédérale de Lausanne
Theresa Mayer, Penn State

9:05 a.m.
29.1 Field-Effect Control of Ions Beyond Debye-Screening Limit in Nanofluidic Transistors, Q. Ran, Y. Liu*, and R.W. Dutton, Stanford University, *Zhejiang University

We investigate the field-effect control of ions in nanofluidic transistors (NFTs) with characteristic channel size (~100nm) significantly larger than the system's Debye length (~10nm). These 100nm NFTs achieve an ionic current modulation ratio of ~2.5, demonstrating better performance than the state-of-the- art 20nm NFTs. The result attests a new operating regime beyond the Debye-screening limit. The relaxed constraint on channel size offers advantages in device manufacturing, testing, and reliability. It also opens up new applications in biological sensing and sample preparation.

9:30 a.m.
29.2 High Performance Dual-Gate ISFET with Non-ideal Effect Reduction Schemes in a SOI-CMOS Bioelectrical SoC, Y.-J. Huang, C.-C. Lin, J.-C. Huang, C.-H. Hsieh, C.-H. Wen, T.-T. Chen, L.-S. Jeng, C.-K. Yang, J.-H. Yang, F. Tsui, Y.-S. Liu, S. Liu, and M. Chen, Taiwan Semiconductor Manufacturing Company

A SOI-CMOS dual-gate ion-sensitive FET which enables non-ideal effect reduction and detection sensitivity boosting is presented. Through an innovative scheme using the bottom-gate transistor instead of the fluidic-gate transistor for sensing, the signal-to-noise ratio is improved by 155x, time drift is reduced by 53x, and hysteresis is reduced by 3.7x.

9:55 a.m.
29.3 1.3 Mega pixels CCD pH Imaging Sensor with 3.75 µm Spatial Resolution (Invited), Y. Edo, Y. Tamai, S. Yamazaki, Y. Inoue, Y. Kanazawa, Y. Nakashima, T. Yoshida, T. Arakawa, S. Saitoh, M. Maegawa, M. Ohnishi, M. Kitao, T. Nakahashi, Y. Suzuki, F. Dasai*, J. Nakai, H. Kawanishi, N. Awaya, and S. Sawada*, Sharp Corporation, *Toyohashi University of Technology

We have demonstrated for the first time a megapixel CCD pH imager featuring a flash-injection-of-signal-electrons scheme. With a spatial resolution of 3.75µm and pH resolution of 0.16pH at 27.5fps we believe this is a promising device technology for applications such as high throughput DNA sequencing and label-free cell measurement system with sub-cell-size spatial resolution and real-time response.

10:20 a.m.
29.4 A Microfabricated Electronic Microplate Platform for Low-cost Repeatable Bio-sensing Applications, M. Zia, T.Chi, C. Zhang, P. Thadesar, T. Hookway*, J. Gonzalez, T. McDevitt*, H. Wang, and M. Bakir, Georgia Institute of Technology, *Gladstone Institute of Cardiovascular Disease

A disposable 'electronic microplate' 3D IC platform allowing reusability of a CMOS biosensor thereby reducing cost and increasing throughput is presented. The electronic microplate utilizes mechanically-flexible interconnects and through- silicon-vias to electrically connect the electrodes on the CMOS biosensor to the electrodes on the electronic microplate, while maintaining a physical separation.

10:45 a.m.
29.5 High Density Optrode-electrode Neural Probe using Si_xN_y Photonics for In Vivo Optogenetics, L. Hoffman, M. Welkenhuysen, A. Andrei, S. Musa, Z. Luo, S. Libbrecht*, S. Severi, P. Soussan, V. Baekelandt*, S. Haesler*, G. Gielen, R. Puers, and D. Braeken, IMEC, *KULeuven

Moore's law in neural sciences. We present a probe with the highest integration density of optrodes-electrodes using a CMOS process platform and 193 nm lithography. We designed, developed, and packaged an ultrathin (30 µm) neural probe, co- integrating silicon nitride (Si_xN_y) photonics and biocompatible titanium nitride (TiN) electrodes. Functionality was verified in vivo by optically evoking and electrically recording neuronal activity in a mouse brain.

11:10 a.m.
29.6 An Ultra Thin Implantable System for Cerebral Blood Volume Monitoring Using Flexible OLED and OPD, Y. Kim, C. Choi, E. Chen, A. Daniel*, A. Masurkar, T. Schwartz*, H. Ma*, and I. Kymissis, Columbia University, *Weill Cornell Medical College

We fabricate and demonstrate an ultra-thin (5µm) implantable system using organic light emitting diodes and organic photodetectors into a reflectivity monitoring system suitable for hemodynamic measurement

of the brain. This system is the first of its kind to record in-vivo measurements of cerebral blood volume and seizure-related activity.

11:35 a.m.
29.7 An Ultraflexible Microbubble Blood Pressure Sensor for Interventional Treatment, L.J. Tang, J. Liu, and B. Yang, Shanghai Jiao Tong University

We report an ultraflexible microbubble blood pressure sensor employs a micro blood bubble for transduction. Micro blood bubble was generated spontaneously by capillary forces. Hydrostatic pressure measurement was demonstrated in rat blood. The sensor was finally mounted on an acupuncture needle (0.38mm diameter) to assemble into a pressure wire.

Session 30: Display and Imaging Systems – Advanced Imagers and Photodetectors
Wednesday, December 9, 9:00 a.m.
Columbia Ballrooms 1, 2, & 5
Co-Chairs: Rihito Kuroda, Tohoku University
Ching-Chun Wang, TSMC

9:05 a.m.
30.1 Multi-storied Photodiode CMOS Image Sensor for Multiband Imaging with 3D Technology, Y. Takemoto, K. Kobayashi, M. Tsukimura, N. Takazawa, H. Kato, S. Suzuki, J. Aoki, T. Kondo, H. Saito, Y. Gomi, S. Matsuda, and Y. Tadaki, Olympus Corporation

We demonstrated multiband imaging with a multi- storied photodiode CMOS image sensor comprising two semiconductor layers that function individually for optimized performance. The sensor captures a wide variety of multiband images, including visible RGB images taken with a Bayer filter and invisible infrared images, at the same time without color degradation.

9:30 a.m.
30.2 First Demonstration of 0.9 µm Pixel Global Shutter Operation by Novel Charge Control in Organic Photoconductive Film, M. Takase, Y. Miyake, T. Yamada, T. Tamaki, M. Murakami and Y. Inoue, Panasonic Corporation

This paper introduces new charge generation and extraction operation in organic photoconductive film sensor. By spatial and temporal control of electric field in organic photoconductive film, high speed global shutter operation in sub-micron pixel, electrical iris control without ND filter, phase difference detective autofocusing are demonstrated.

9:55 a.m.
30.3 Color Image Sensor with Organic Photoconductive Films (Invited), T. Sakai, H. Seo, T. Takagi, M. Kubota, H. Ohtake, and M. Furuta*, NHK Science and Technology Research Laboratories, *Kochi University of Technology

A color image sensor with three-stacked organic photoconductive films (OPFs) and transparent readout circuits for high-resolution, high-sensitive, compact color video cameras is described. The sensor separates and simultaneously detects the three primary colors. We fabricated test image sensors and confirmed the feasibility of a color video camera with three-stacked OPFs.

10:20 a.m.
30.4 Optical Performance Study of BSI Image Sensor with Stacked Grid Structure, Y.-W. Cheng, T.-H. Tsai, C.-H. Chou, K.-C. Lee, H.-C. Chen, and Y.-L. Hsu, Taiwan Semiconductor Manufacturing Company

Stacked grid structure is implemented into BSI image sensors and device performance for various grid dimension and height has been investigated. Simulated angular response shows less QE degradation in large incident angle and SNR-10 has a ~10% improvement for devices with stacked grid structure.

10:45 a.m.
30.5 Avalanche Photodiode Featuring Germanium-Tin Multiple Quantum Wells on Silicon: Extending Photodetection to Wavelengths of 2 µm and Beyond, Y. Dong, W. Wang, S.Y. Lee*, D. Lei, X. Gong, W. Khai Loke*, S.-F. Yoon*, G. Liang, Y.-C. Yeo, National University of Singapore, *Nanyang Technological University

We report the world's first demonstration of a $Ge_{0.9}Sn_{0.1}$ multiple quantum wells on Si avalanche photodiode ($Ge_{0.9}Sn_{0.1}$ MQW/Si APD), achieving a cutoff wavelength λ above 2 µm. A high optical responsivity of 0.33 A/W is achieved at λ = 2003 nm due to the internal avalanche multiplication.

11:10 a.m.
30.6 High Dose Efficiency, Ultra-high Resolution Amorphous Selenium/CMOS Hybrid Digital X-ray Imager, C.C. Scott, A. Parsafar, A. El-Falou, P.M. Levine, K.S. Karim, University of Waterloo

We demonstrate high dose efficiency from a high- resolution 5.6 µm×6.25 µm pixel pitch amorphous selenium/CMOS hybrid X-ray imager that could radically accelerate bioengineering research by enabling lab-based in vivo pre-clinical imaging. Compared to existing scintillator-based imagers, our approach enables 100× gains in dose efficiency at spatial frequencies of 20-60 cycles/mm.

11:35 a.m.
30.7 Stacked Image Sensor Using Chlorine-doped Crystalline Selenium Photoconversion Layer Composed of Size-controlled Polycrystalline Particles, S. Imura, K. Kikuchi, K. Miyakawa, H. Ohtake, M. Kubota, T. Okino*, Y. Hirose*, Y. Kato*, and N. Teranishi**, NHK Science and Technology Research Laboratories, *Panasonic Corporation, **University of Hyogo

We demonstrate a stacked CMOS image sensor overlaid with a chlorine (Cl)-doped crystalline selenium (c-Se) photoconversion layer. The size of the polycrystalline particles of c-Se, which is strongly related to the fixed pattern noise, is perfectly controlled by Cl doping to c-Se; hence, the resulting device provides clearer images.

Session 31: Power and Compound Semiconductor Devices – III-V: FETs, Photonics, Si Integration
Wednesday, December 9, 9:00 a.m.
Columbia Ballrooms 3, 4, & 6
Co-Chairs: Mark Rodwell, Univ. of CA, Santa Barbara
Lukas Czornomaz, IBM Zurich Research

9:05 a.m.
31.1 Gate-All-Around InGaAs Nanowire FETS with Peak Transconductance of 2200 µS/µm at 50nm Lg using a Replacement Fin RMG Flow, N. Waldron, S. Sioncke, L. Nyns, A. Vais**, X. Zhou, H.C. Lin, G. Boccardi, J.W. Maes*, Q. Xie*, M. Givens*, F. Tang*, X. Jiang*, E. Chiu**, A. Opdebeeck, C. Merckling, F. Sebaai, D. van Dorp, L. Teugels, A. Sibaja Hernandez, K. de Meyer***, K. Barla, N. Collaert, Y.-V. Thean, imec, *ASM, **Poongsan Inc., ***KU Leuven

We report record results for III-V devices fabricated on 300mm Si wafers. A g_m of 2200 µS/µm with an SS_{SAT} of 110 mV/dec is achieved for an Lg=50nm device using a newly developed gate stack interlayer material deposited by ALD. In addition it is shown that high pressure annealing can further improve device performance with an average increase in g_m of 22% for a 400 °C anneal.

9:30 a.m.
31.2 Self-Aligned, Gate-Last Process for Vertical InAs Nanowire MOSFETs on Si, M. Berg, K.-M. Persson, O.-P. Kilpi, J. Svensson, E. Lind, and L.-E. Wernersson, Lund University

A self-aligned, gate-last, process is developed for vertical nanowire MOSFETs that allows for thin intrinsic channels regions and thicker doped contacts using digital etching. The highest performance in terms of $g_{m,max}$ and SS for any vertical nanowire MOSFET, with $g_{m,max}$ reaching 1.29 mS/µm and SS of 90 mV/dec is demonstrated.

9:55 a.m.
31.3 Quantum-size Effects in sub 10-nm fin Width InGaAs FinFETs, A. Vardi, X. Zhao, and J. del Alamo, Massachusetts Institute of Technology

InGaAs FinFETs with sub-10 nm fin widths were fabricated for the first time using precision dry etching and digital etch. We find that the threshold voltage, V_T, becomes highly sensitive to the fin width, W_f, in the sub-10 nm W_f range. We attribute this to quantization effects. We also show that in the quantum regime, a sidewall slope less than 85 degree significantly mitigates V_T variation.

10:20 a.m.
31.4 Single Suspended InGaAs Nanowire MOSFETs, C. Zota, L.-E. Wernersson, and E. Lind, Lund University

We report on $In_{0.85}Ga_{0.15}As$ nanowire MOSFETs utiziling a single selectively grown nanowire suspended above the substrate as the channel. Devices exhibit record-high g_m = 3.3 mS/µm for any transistor, SS = 118 mV/dec at V_{DS} = 0.5 V, and DIBL = 40 mV/V. The quality factor Q = g_m/SS is 28, the highest for non-planar III-V FETs.

10:45 a.m.
31.5 CMOS Photonics Technologies Based on Heterogeneous Integration of SiGe/Ge and III-V on Si (Invited), M. Takenaka, Y. Kim, J. Han, J. Kang, Y. Ikku, Y. Cheng, J. Park, S. Kim and S. Takagi, The University of Tokyo
We present CMOS photonics technologies for electronic- photonic integration on the Si platform. Heterogeneous integration of SiGe/Ge/III-V on Si enables monolithic integration of high-performance MOSFETs and waveguide- based photonics on common platforms, which will be indispensable for extending functionalities of future Si chips including off-chip and on-chip optical interconnections and bio/medical sensors.

11:10 a.m.
31.6 An InGaSb p-channel FinFET, W. Lu, J.F. Kim*, J.F. Klem*, S.D. Hawkins*, and J. A. del Alamo, Massachusetts Institute of Technology, *Sandia National Laboratories

We demonstrate the first InGaSb p-channel FinFET with promising performance. Towards this goal, we develop a fin dry-etch technology which yields fins as narrow as 15 nm with vertical sidewalls and low sidewall interface state density. We also realize Si-compatible ohmic contacts with ultra- low contact resistivity of $3.5 \cdot 10^{-8}$ $\Omega \cdot cm^2$.

11:35 a.m.
31.7 Record Performance InGaAs Homo-junction TFET with Superior *SS* Reliability over MOSFET, A. Alian, J.Franco, A. Vandooren, Y. Mols, A. Verhulst, S. El Kazzi, R. Rooyackers, D. Verreck, Q. Smets, A. Mocuta, N. Collaert, D. Lin, and A. Thean, imec

InGaAs planar TFETs with 70% In content are fabricated and characterized. The increase of the In content of the 8 nm channel from 53% to 70% is found to significantly boost the performance of the device. Record performance I_{on}=4 µA/µm at I_{off} = 100 pA/µm, V_{dd}=0.5V and V_d=0.3 V with minimum sub-threshold swing (SS_{min}) of 60 mV/dec at 300K is obtained for a homo-junction InGaAs device. Reliability assessment shows that the TFET SS and transconductance (g_m) are more immune to PBTI stress than its equivalent MOSFET device.

Entrepreneurs Luncheon

Wednesday, December 9, 12:30 p.m.
Lincoln Room

Speaker: Abbie Gregg, President, Abbie Gregg, Inc. (AGI)

AGI was founded in 1985 and has extensive experience in nanotechnology, biotechnology, photovoltaic, wafer fab, assembly, multichip module, disc drive, flat panel display and flexible electronics start-up planning, process engineering and operations. AGI has gained global industry recognition for the depth of excellence our services provide. To date AGI has completed over 800 projects on 5 continents.

Biography

Abbie Gregg started Abbie Gregg, Inc. in September 1985 and just celebrated the company's 30th anniversary, a remarkable milestone in the company's history!
Abbie Gregg is an industry expert and cleanroom consultant with many years of experience in engineering consulting specializing in microelectronics process analysis and the design, startup and operations of clean laboratories and manufacturing facilities. Her interests and skills are comprised of process engineering and analysis, facility layout and design, site selection and strategic planning, yield enhancement, quality assurance, manufacturing operations management, equipment selection and qualification, factory/product cost modeling, and nanotechnology.

As President of AGI, she has completed over 826 projects worldwide, spanning five continents for industrial, government, and university clients. These projects have included Nanotechnology, Wafer Fab, MEMS, Flexible Electronics, Imaging, Photovoltaics, Disc Drive, Bio/Pharma, and FPD Projects. Abbie has also developed a database and software system for computer aided layout, utility load analysis, and design of cleanrooms, advanced laboratories and characterization/imaging areas. She has done extensive turn-around consulting, assisting technical operations with project management, and implementing continuous improvement methods.

Abbie holds a Bachelor of Science in Metallurgy and Material Science and Engineering from Massachusetts Institute of Technology, and studied Electrical Engineering at the University of Maine.

Session 32: Nano Device Technology – Beyond CMOS Technologies
Wednesday, December 9, 1:30 p.m.
International Ballroom East
Co-Chairs: Zoran Krivokapic, GlobalFoundries
Matthias Passlack, TSMC

1:35 p.m.
32.1 High-Frequency Prospects of 2D Nanomaterials for Flexible Nanoelectronics from Baseband to sub-THz Devices, S.

Park, W. Zhu, H.-Y. Chang, M.N. Yogeesh, R. Ghosh, S. Banerjee, and D. Akinwande, The University of Texas at Austin

2D materials are ideal for flexible electronics owing to their optimum electrostatics, transparency and mechanical compliance. Here, we present the state-of-the-art sub-μm RF transistors operating in the velocity saturation regime for maximum transport. We realize high-frequency TMD, phosphorene and graphene flexible transistors with cut-off frequencies ranging from GHz to sub-THz.

2:00 p.m.
32.2 TMD FinFET with 4 nm Thin Body and Back Gate Control for Future Low Power Technology, M.-C. Chen, K.-H. Li, L.-J. Li*, A.Y. Lu*, M.-Y. Li*, Y.-H. Chang***, C.-H. Lin, Y.-J. Chen, Y.-F. Hou, , C.-C. Chen, B.-W. Wu, C.-S. Wu, I. Yang, Y.-J. Lee, J.-M. Shieh, W.-K. Yeh, J.-H. Shih, P.-C. Su***, A. Sachid, T. Wang***, F.-L. Yang**, and C. Hu^, National Nano Device Laboratories, *King Abdullah University of Sci. and Technology, **Academia Sinica, ***National Chiao Tung University, ^University of California, Berkeley

A 4 nm thin transition-metal dichalcogenide (TMD) body FinFET with back gate control is proposed and demonstrated for the first time. The TMD FinFET channel is deposited by CVD. Hydrogen plasma reduction of TMD is employed to lower the series resistance for the first time. The 2nm thin back gate oxide enables 0.5V of V_{th} shift with 1.2V change in back bias for correcting device variations and dynamically configuring a device as a high-performance or low power device. TMD can potentially provide sub-nm thin mono-layer body needed for 2nm node FinFET.

2:25 p.m.
32.3 Enhancement-Mode Single-layer CVD MoS_2 FET Technology for Digital Electronics, L. Yu, D. El-Damak, S. Ha, X. Ling, Y. Lin, A. Zubair, Y. Zhang, Y.-H. Lee*, J. Kong, A. Chandrakasan, T. Palacios, Massachusetts Institute of Technology, *National Tsing-Hua University,

2D nanoelectronics based on single-layer(SL) MoS_2 offers great advantages for ubiquitous electronics.This paper presents highly uniform E-mode FET using SL CVD MoS_2 with positive V_T, large mobility, excellent subthreshold swing, enabling the design and fabrication of multistage combinational and sequential circuits.

2:50 p.m.
32.4 Efficient Metallic Carbon Nanotube Removal for Highly-Scaled Technologies, M. M. Shulaker, G. Hills, T.F. Wu, Z. Bao, H.-S. Philip Wong, and S. Mitra, Stanford University

We demonstrate a VLSI-compatible method for removing metallic CNTs that: (a) removes >99.99% of metallic CNTs, (b) limits inadvertent removal of semiconducting CNTs to <1%, (c) scales to any arbitrary contacted gate pitch, and (d) can be applied to high CNT

densities (>200 CNTs/µm, required for high performance CNFET digital systems).

3:15 p.m.
32.5 Spintronic Majority Gates (Invited), I. P. Radu, O. Zografos, A. Vaysset, F. Ciubotaru, J. Yan, J. Swerts, D. Radisic, B. Briggs, B. Soree, M. Manfrini, M. Ercken, C. Wilson, P. Raghavan, S. Sayan, C. Adelmann, A. Thean, L. Amaru*, P.-E. Gaillardon*, G. De Micheli*, D.E. Nikonov**, S. Manipatruni**, and I.A. Young**, IMEC, *EPFL, **Intel Corp.

Beyond CMOS devices are being intensively studied to expand functionally for future technology nodes. Spin logic devices can enable a) non- volatility; b) ultra-low power operation; and c) improved circuit efficiency. We focus on majority gates as they could revolutionize circuit design. Physics of spin devices is naturally amenable for majority logic operation. Several proposals for spintronic majority gates exist. Here we compare spin torque majority gates (STMG) and spin wave majority gates (SWMG) and summarize our work on these concepts.

3:40 p.m.
32.6 Spintronic Logic Circuit and Device Prototypes Utilizing Domain Walls in Ferromagnetic Wires with Tunnel Junction Readout, J.A. Currivan-Incorvia, S. Siddiqui, S. Dutta, E.R. Evarts*, C. Ross, and M. Baldo, Massachusetts Institute of Technology, *National Institute of Standards and Technology

We present switch prototypes that encode information in a magnetic domain wall. We develop a model which predicts the device, circuit, and scaling behavior. We build prototypes showing a device can perform AND/NAND, one device can drive two subsequent devices, and information can propagate in a circuit of three flip-flops.

Session 33: Sensors, MEMS, and BioMEMS – Emerging Nanodevices and Nanoarrays
Wednesday, December 9, 1:30 p.m.
Jefferson Room
Co-Chairs: Dimitrios Peroulis, Purdue University
Naigang Wang, IBM T.J. Watson Research Ctr.

1:35 p.m.
33.1 High Performance and Reliable Silicon Field Emission Arrays Enabled by Silicon Nanowire Current Limiters, S. Guerrera, A. Akinwande, Massachusetts Institute of Technology

We report a high current density ($J > 100$ A/cm^2) cold cathode based on silicon field emitter arrays that operates at low voltage ($V_{GE} < 60$ V), and has long lifetime. A unique device architecture regulates electron flow to each field emitter tip with a silicon nanowire current limiter.

2:00 p.m.

33.2 Eliminating Proximity Effects and Improving Transmission in Field Emission Vacuum Microelectronic Devices for Integrated Circuits, E. Radauscher, K. Gilchrist*, S. Di Dona, Z. Russell, J. Piascik*, C. Parker, B. Stoner*, and J. Glass, Duke University, *RTI International

This work evaluates crosstalk and transmission efficiency in integrated field emission vacuum microelectronic devices (FE-VMDs). Experimental evidence was used to show proximity effects cannot be neglected. Simulations were used to understand the root cause, design structural solutions, and improve overall device performance. New design features are proposed for improved integration.

2:25 p.m.
33.3 A New Plasma Device Operated in Liquids for Biological Applications, M. Egawa, S. Imai, Y. Sakaguchi, A. Odagawa, Panasonic Corporation

We propose a new MEMS device generating planar plasma in liquids for biological applications. The device was designed with 10 mm distances between via-holes with 2D-FEM. Electric double layer formed by aging at high voltages reduces any resistance variations. Ignored these variations, our device can generate plasmas at nine via-holes.

2:50 p.m.
33.4 Artificially Intelligent Nanoarrays for Disease Detection via Volatolomics (Invited),
R. Vishinkin, and H. Haick, Technion – Israel Institute of Technology

According to recent reports, more than 15 million deaths occur annually due to infectious diseases[1] and approximately 57 million deaths occurred in 2008 from non-communicable diseases including cancer[2]. The spectrum of currently available medical methods does not enhance detection of many diseases, primarily due to technology limitations and their complexities, causing a delay in diagnosis.[1-3] For this reason, there is an urgent need for inexpensive and minimally invasive technology that would allow efficient early detection, stratifying the population for a personalized therapy, and for rapid bed-side assessment of treatment efficacy. An emerging approach that has a high potential to fulfill these needs is based on the so-called "volatolomics", viz. chemical processes involving profiles of highly volatile organic compounds (VOCs) which are by-products of metabolic and pathological processes and are emitted from various body fluids including breath, skin, urine, blood, and others. [3-6]

3:15 p.m.
33.5 Flexible Graphene Hall Sensors with High Sensitivity, L. Huang, Z. Zhang, B. Chen, and L.-M. Peng, Peking University

Graphene has an extremely-thin body and high mobility and is thus an outstanding material for constructing ultra-sensitive Hall sensors. In this work, we massively fabricated graphene Hall elements (GHEs)

with sensitivity up to 2300 V/T, and demonstrated flexible GHEs with high linearity and high stability against bending.

3:40 p.m.
33.6 Suspended AlGaN/GaN Membrane Devices with Recessed Open Gate Areas for Ultra-low-Power Air Quality Monitoring, P. Offermans, A. Si-Ali, G. Brom-Verheyden, K. Geens*, S. Lenci*, M. Van Hove*, S. Decoutere*, and R. van Schaijk, imec/Holst Centre, *IMEC

We have developed a novel gas sensor platform for ultra-low-power air quality monitoring based on suspended AlGaN/GaN membranes fabricated on 8 inch Si(111) wafers. The device shows excellent sensitivity to NO_2 with exceptionally little humidity interference. We show extension of the platform to NH_3, H_2 and CO_2 detection.

Session 34: Modeling and Simulation – Modeling of III-V and Ge Materials and Alternative CMOS Device Architecture
Wednesday, December 9, 1:30 p.m.
Columbia Ballrooms 1, 2, & 5
Co-Chairs: Roza Kotlyar, Intel
Katsumi Eikyu, Renesas

1:35 p.m.
34.1 CMOS Performance Benchmarking of Si, InAs, GaAs, and Ge Nanowire n- and pMOSFETs with L_G=13 nm Based on Atomistic Quantum Transport Simulation Including Strain Effects, R. Kim, U.E. Avci, and I.A. Young, Intel Corp.

As MOSFET scaling continues, new n- and p-channel materials are being actively explored to deliver performance targets better than Si. In this paper, we present CMOS performance benchmarking results for Si, InAs, GaAs, and Ge nanowire (NW) n- and pMOSFETs with L_G=13 nm based on atomistic quantum transport simulation including strain effects. Uniaxial tensile/compressive strain mostly increases nMOS/pMOS drive current and vice versa, but results may be different for low power (LP) operation because strain may also affect the leakage current. We also discuss the threshold voltage sensitivity to strain, which may have an impact on the device variation. Finally, we compare current, capacitance, and CV/I delay (gate or interconnect loading) metrics across different n-channel (Si, InAs, GaAs, Ge) and p-channel (Si, Ge) materials considering extrinsic parasitic components (RSD, C_{fringe}) for different supply voltages. We project that Ge CMOS (using <110> NWs) with S/D doping density optimized depending on the operating condition (high performance (HP) or LP) may deliver the best drive current and CV/I while it would also benefit from the homogeneous material integration. For low capacitance (power consumption), III-V-Ge hybrid CMOS is most advantageous.

2:00 p.m.
34.2 Effects of Free-carriers on Rigid Band and Bond Descriptions in Germanium - Key to Designing and Modeling in Ge Nano-devices, S. Kabuyanagi and A. Toriumi, University of Tokyo

This paper discusses intrinsic properties of Ge films in terms of phonon and electronic structures. The gate bias-dependent Raman and Photoluminescence (PL) spectroscopies have been investigated by using back-biased GeOI FETs. The present results indicate that both phonon and electronic structures are dependent on carrier-density at a fixed doping concentration. The results provide not only fundamental knowledge on semiconductor physics but also critical parameter for the device modeling.

2:25 p.m.
34.3 Replacement Metal Gate Resistance in FinFET Architecture: Modelling, Validation and Extendibility, R. Bao, B. Greene, U. Kwon, S. Lee, J. Bruley, W. Wang, K. Zhao, P. DeHaven, Z. Li, K. Wong, S. Grunow, R. Divakaruni, C.-H. Lin, S. Krishnan, and V. Narayanan, IBM

We demonstrate a model to simulate the W film resistivity and gate resistance. The prediction that TiN fill offers the lower gate resistance than TiN/W fill for highly scaled gate lengths is validated by experimental data. We observe that TiN fill provides ~6.4 % performance improvement for real FinFET devices.

2:50 p.m.
34.4 Process Variation Effect, Metal-Gate Work-Function Fluctuation and Random Dopant Fluctuation of 10-nm Gate-All-Around Silicon Nanowire MOSFET Devices, H.-T. Chang, C.N. Lai, P.-J. Chao, C.-Y. Chen, and Y. Li, National Chiao Tung University

In this work, process variation effect, work function fluctuation, and random dopant fluctuation on 10-nm high-k/metal gate gate-all-around silicon nanowire MOSFET devices using full-quantum- mechanically validated and experimentally calibrated device simulation are studied. The small aspect ratio device has greater immunity of RDF, while suffers from PVE and WKF.

3:15 p.m.
34.5 Study of TFET Non-ideality Effects for Determination of Geometry and Defect Density Requirements for Sub-60mV/dec Ge TFET, U.E. Avci, B. Chu-kung, A. Agrawal, G. Dewey, V.H. Le, R. Rios, D.H Morris, S. Hasan, R. Kotlyar, J. Kavalieros, and I.A. Young, Intel Corp.

We show a clear separation of the requirements to achieve a sub-60mV/dec TFET for i) geometry, ii) semiconductor's BTBT characteristics, iii) semiconductor defects and iv) oxide interface defects. Multi-temperature characterization of experimental Ge diodes is used to separate bulk from the interface effects, calibrating all models: BTBT, TAT and SRH. An experimental semiconductor material's BTBT characteristic is as important as defects, showing even zero-defect TFET using the calibrated Ge material requires thin body and thin oxide. Bulk SRH/TAT is found to be a less critical for small body TFETs whereas interface defect density ~$10^{12}cm^{-2}$ is low enough to realize intrinsic BTBT characteristics.

3:40 p.m.
34.6 InAs-GaSb/Si Heterojunction Tunnel MOSFETs: An Alternative to TFETs as Energy-Efficient Switches? H. Carrillo-Nuñez, M. Luisier, and A. Schenk, ETH Zürich

Quantum transport simulations of InAs-GaSb double- gate ultra-thin-body and InAs-Si gate-all-around nanowire tunneling MOSFETs with realistic dimensions are reported for the first time. Different gate lengths, body thicknesses, and diameters are compared. Results suggest that thicker devices offer a favorable playground for steeper subthreshold slopes and higher ON-currents than conventional TFETs.

Session 35: Power and Compound Semiconductor Devices – GaN Material and Device Interactions
Wednesday, December 9, 1:30 p.m.
Columbia Ballrooms 3, 4, & 6
Co-Chairs: Michael Uren, University of Bristol
Alex Kalnitsky, TSMC

1:35 p.m.
35.1 Design Space and Origin of Off-State Leakage in GaN Vertical Power Diodes, Y. Zhang, H.-Y. Wong*, M. Sun, S. Joglekar, L. Yu, N. Braga*, V. Mickevicius*, and T. Palacios, Massachusetts Institute of Technology, *Synopsys

Variable-range-hopping through dislocations was identified as the main off-state leakage mechanism for GaN vertical diodes on different substrates, by experiments and TCAD simulations. Designed GaN vertical diodes demonstrate 2-4 orders of magnitude lower leakage current while supporting 3-5 times higher electric field, compared to GaN lateral, Si and SiC devices.

2:00 p.m.
35.2 Impact of Buffer Leakage on Intrinsic Reliability of 650V AlGaN/GaN HEMTs, P. Moens, A. Banerjee, M.J. Uren*, M. Meneghini**, S. Karboyan*, I. Chatterjee*, P. Vanmeerbeek, M. Cäsar, C. Liu, A. Salih, E. Zanoni**, G. Meneghesso**, M. Kuball*, M. Tack, ON Semiconductor, *University of Bristol, **University of Padova

This paper reports on the correlation between the off-state vertical leakage of 650V rated GaN-on-Si power devices and the dynamic Ron. The role of buffer traps (identified as CN acceptors through current DLTS) for both mechanisms is investigated. It is found that the dynamic Ron is strongly voltage-dependent, due to the interplay between the dynamic properties of the CN traps and the presence of space-charge limited current components. This results in a complete suppression of dynamic Ron and static Ron degradation under HTRB conditions between 420V and 850V.

2:25 p.m.
35.3 III-Nitride Transistors with Photonic-Ohmic Drain for Enhanced Dynamic Performances, X. Tang, B. Li, Y. Lu, H. Wang,

C. Liu, J. Wei, and K.J. Chen, Hong Kong University of Science and Technology

We demonstrate a power FET with photonic-ohmic drain (PODFET) using HEMT-compatible process on a conventional AlGaN/GaN-on-Si power electronics platform. Photons are synchronously generated with the switching channel current, and they are capable of effectively pumping electrons from deep surface/bulk traps. Consequently, the device dynamic performance is significantly enhanced.

2:50 p.m.
35.4 The Physical Mechanism of Dispersion Caused by AlGaN/GaN Buffers on Si and Optimization for Low Dispersion, S. Stoffels, M. Zhao, R. Venegas, P. Kandaswamy, S. You, Y. Saripalli, M. Van Hove, S. Decoutere, and T. Novak*, imec, *ON Semiconductor

The goal of this work was to advance the physical understanding of buffer dispersion, to understand how different parts of the buffers contribute to the observed current collapse and to use these learnings to design buffers with low buffer induced dispersion in the two dimensional electron gas (2DEG) channel. For this end we have done an extensive design of experiments (DOE) and have compared three fundamentally different buffers, namely stepped buffers, low temperature AlN interlayer buffers (I.L.) and superlattice buffers (S.L).

3:15 p.m.
35.5 Modification of "Native" Surface Donor States in AlGaN/GaN MIS-HEMTs by Fluorination: Perspective for Defect Engineering, M. Reiner, P. Lagger, G. Prechtl, P. Steinschifter, R. Pietschnig*, D. Pogany**, and C. Ostermaier, Infineon Technologies AG, *University of Kassel, **Vienna University of Technology

We report on AlGaN/GaN MIS-HEMTs with a chemically very stable fluorine-passivated dielectric/AlGaN interface causing a modification of the "native" surface donors and leading to a fundamentally different device and defect behavior. The feasibility of III-N surface defect modifications shows a new direction for reducing VTh drifts or defect engineered devices.

3:40 p.m.
35.6 Steep Subthreshold Swing Tunnel FETs: GaN/InN/GaN and Transition Metal Dichalcogenide Channels (Invited), A. Seabaugh, S. Fathipour, W. Li, H. Lu, J.H. Park*, A. Kummel*, D. Jena**, S. Fullerton-Shirey***, P. Fay, University of Notre Dame, *University of California, San Diego, **Cornell University, ***University of Pittsburgh

As the understanding of tunnel field-effect transistors (TFET) evolves, new transistor approaches are being advanced to provide higher on-currents, lower off-currents, lower defect density tunnel junctions, and to increase the current at which the subthreshold swing becomes 60 mV/decade (I_{60}). This paper shows why nitride- and transition- metal-dichalcogenide (TMD)-based materials are being considered for TFETs. First experimental results not included here will be presented.

In the TMD materials, WSe_2 TFETs with junctions formed using ion doping with Cs^+ and ClO_4^- in polyethylene oxide (PEO) are being yielded. Record low leakage currents in atomic layer deposited Al_2O_3 gate stacks on WSe_2 has been demonstrated. WSe_2 TFETs are shown with transfer characteristics that are substantially independent of temperature and consistent with tunneling transport.

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