Session 37: Memory Technology - 1S1R Arrays and Select Devices
Wednesday, December 5, 1:30 PM
Continental Ballroom 4
Co-Chairs: C. Petti, Western Digital Corp.
T. Yamaguchi, Toshiba Memory Corporation

1:35 PM - 2:00 PM
37.1 High-performance, cost-effective 2z nm two-deck cross-point memory integrated by self-align scheme for 128 Gb SCM, *T. Kim, H. Choi, M. Kim, J. Yi, D. Kim, S. Cho, H. Lee, C. Hwang, E.-R. Hwang, J. Song, S. Chae, Y. Chun, J.-K. Kim, SK-Hynix*

We demonstrate a high-performance and cost-effective cross-point memory (CPM) technology for two-deck 128 Gb storage class memory (SCM). The unit MAT size is 16 Mb consisting of a 2z nm 1S1M (one selector one memory) structure that is patterned by only two ArF-i steps per deck for a low cost per bit. The formidable task of self-align etch is enabled by the use of state-of-the-art etching and integration technology, which otherwise easily leads to hard fail or poor cell characteristics and reliabilities. New phase change materials (N-PCMs) are developed to have a large Vt window and a uniform Vt distribution for a sufficient read window margin (RWM) and a corresponding low raw bit error rate (RBER). New chalcogenide selectors (NCSs) are also developed to provide low Vt instability and very low leakage current. The new CPM is able to provide a sufficient RWM for 16 Mb MATs with very low latencies of write (set $\leq$ 300 ns) and read ($\leq$ 100 ns). We also demonstrate its decent write disturbance and high reliabilities such as endurance and thermal retention.

2:00 PM - 2:25 PM
37.2 A Highly Efficient and Scalable Model for Crossbar Arrays with Nonlinear Selectors, *A. Chen, IBM Reseach Division*

A scalable crossbar array model is proposed to solve arrays with various sizes and device characteristics. Computation is accelerated over 1000X by array reduction, enabling array scaling analysis and extensive design space exploration. Computation error can be reduced by extrapolation from calculations with different array reduction ratios. The impact of selectors on array performance is analyzed with this model, which can be applied to nonlinear, threshold switch, and rectifying selectors.

2:25 PM - 2:50 PM
37.3 Ultra-High Endurance and Low I_{OFF} Selector based on AsSeGe Chalcogenides for Wide Memory Window 3D Stackable Crosspoint Memory, *H. Y. Cheng, W. C. Chien, I. T. Kuo, C. W. Yeh, L. Gignac*, W. Kim*, E. K. Lai, Y. F. Lin, R. L. Bruce*, C. Lavoie*, C. W. Cheng*, A. Ray*, F. M. Lee, F. Carta*, C. H. Yang, M. H. Lee, H. Y. Ho, M. BrightSky* and H. L. Lung, IBM/Macronix PCRAM Joint Project, Macronix International Co., Ltd., *IBM T. J. Watson Research Center*

New selector materials with very-low IOFF and optimum Vth based on As-Se-Ge chalcogenides are studied. An optimized composition is proposed, which achieves a good trade-off between thermal stability and cycling endurance and it is successfully integrated with PCM in a 3D stackable pillar structure. SET/RESET operation are demonstrated with ~2V memory window. Selector is able to deliver 1mA ON current (7.9 MA/cm2) and fast speed (10 ns). More than 1E12 read cycling endurance is achieved in 1S1R (OTS+PCM) device due to the excellent endurance of the selector.

2:50 PM - 3:15 PM
37.4 Optimized Reading Window for Crossbar Arrays Thanks to Ge-Se-Sb-N-based OTS Selectors, *A. Verdy, M. Bernard, J. Garrione, G. Bourgeois, M. C. Cyrille, E. Nolot, N. Castellani, P. Noé, C. Socquet-Clerc, T. Magis, G. Sassine, G. Molas, G. Navarro and E. Nowak, CEA, LETI*

In this paper, we investigate the impact of Ovonic Threshold Switching (OTS) selector electrical parameters, such as the threshold and the holding current, on the reliability of the reading operation in 1S1R memory devices. Through physico chemical analysis and electrical characterization of Se rich Ge Se based OTS selectors, performed up to 400 °C, we demonstrate the possibility to reduce the fire voltage as well the leakage current thanks to N and Sb doping. Moreover, we describe the correlation that exists between the leakage current and the threshold current in OTS devices. We highlight the subsequent trade off between the reading window and the array size in an OTS-based Memory Crossbar Array, evaluated up to an operating temperature of 150 °C. Finally, thanks to OTS engineering, we demonstrate how the reading window can be optimized for a target array size and application.

3:15 PM - 3:40 PM

37.5 Forming-free Mott-oxide threshold selector nanodevice showing s-type NDR with high endurance (> 10^{12} cycles), excellent V_{th} stability (< 5%), fast (< 10 ns) switching, and promising scaling properties, *T. Hennen, D. Bedau*, J. A. J. Rupp, C. Funck, S. Menzel**, M. Grobis*, R. Waser, and D. J. Wouters, RWTH Aachen University, *Western Digital San Jose Research Center, **Forschungszentrum Jülich GmbH*

Thin film (10 nm) $(V_{1-x}Cr_x)_2O_3$ Mott-oxide based nano-devices show volatile threshold switching. Fast (< 10 ns) and very stable (< 5% variation, > 10^12 cycles) switching is obtained. Thickness and area dependence of the NDR curves are consistent with uniform volume switching and are explained with a thermal feedback model.