Session 35: Process and Manufacturing Technology - Advanced Channel and Contact Technologies
Wednesday, December 5, 1:30 PM
Grand Ballroom B
Co-Chairs: Y. Zhao, Zhejiang University
T. Yamaguchi, Renesas

1:35 PM - 2:00 PM
35.1 Toward High Performance SiGe Channel CMOS: Design of High Electron Mobility in SiGe nFinFETs Outperforming Si, *C. H. Lee, R. G. Southwick III, S. Mochizuki, J. Li, X. Miao, M. Wang, R. Bao, I. Ok, T. Ando*, P. Hashemi*, D. Guo, V. Narayanan*, N. Loubet, and H. Jagannathan, IBM Research and *IBM T. J. Watson Research Center*

For the first time, high electron mobility in tensile-strained SiGe channel nFinFETs outperforming Si is reported to explore the feasibility of high performance SiGe CMOS. To examine the electron mobility behaviors in SiGe channel, a series of tensile-strained SiGe nFinFETs are fabricated on various strain relaxed buffer layers by taking into account the minimum threading dislocation density and strain engineering. For SiGe (Ge >20%) nFinFETs, we identify the existence of additional electron trapping site close to the conduction band edge in IL/HK, leading to the abnormal Vt shift, PBTI degradation, and low electron mobility. We also fabricated short-channel SiGe nFinFETs, which exhibit excellent cut-off behavior and electrostatics (SS ~65mV/dec and DIBL ~18mV at VDD=0.7V). In addition, the dynamic performance of tensile-strained SiGe CMOS against Si CMOS is evaluated by TCAD simulation based on experimental data.

2:00 PM - 2:25 PM
35.2 Advanced Arsenic Doped Epitaxial Growth for Source Drain Extension Formation in Scaled FinFET Devices, *S. Mochizuki, B. Colombeau*, L. Yu, A. Dube*, S. Choi, M. Stolfi*, Z. Bi, F. Chang*, R. A. Conti, P. Liu*, K. R. Winstel, H. Jagannathan, H.-J. Gossmann*, N. Loubet, D. F. Canaperi, D. Guo, S. Sharma*, S. Chu*, J. Boland*, Q. Jin*, Z. Li*, S. Lin*, M. Cogorno*, M. Chudzik*, S. Natarajan*, D. C. McHerron and B. Haran, IBM Research, *Applied Materials*

In this paper, we demonstrate a novel Source Drain Extension (SDE) approach to enable NMOS device scaling along with improved performance. For the first time, SDE formation with epitaxially grown As doped Si (Si:As) has been examined and compared to the current state-of-the-art SDE formation in FinFET at 10nm logic ground rules. It is found that a Si:As layer based SDE provides a clear improvement in the short channel effect and a significant device performance increase. It is also shown that a careful co-optimization of the Si:As layer and Source / Drain (S/D) lateral recess is required to achieve the optimum device gain. This paves the way for the ultimate nSDE formation for current and next generation CMOS devices.

2:25 PM - 2:50 PM
35.3 External Resistance Reduction by Nanosecond Laser Anneal in Si/SiGe CMOS Technology, *O. Gluschenkov, H. Wu, K. Brew, C. Niu*, L. Yu, Y. Sulehria, S. Choi, C. Durfee, J. Demarest, A. Carr, S. Chen*, J. Willis*, T. Thanigaivelan*, F.-L. Lie, W. Kleemeier*, and D. Guo, IBM Research, *GLOBALFOUNDRIES Inc., **ULTRATECH*

Significant pFinFET external resistance reduction (~40%) was achieved by nanosecond laser annealing of S/D structures. Selective melting of S/D elements is responsible for this improvement. Short channel characteristics are not degraded within the identified process window. Contacted gate pitch and fin number dependence of the process window is assessed.

2:50 PM - 3:15 PM

35.4 Parasitic Resistance Reduction Strategies for Advanced CMOS FinFETs Beyond 7nm, *H. Wu, O. Gluschenkov, G. Tsutsui, C. Niu, K. Brew, C. Durfee, C. Prindle, V. Kamineni, S. Mochizuki, C. Lavoie, E. Nowak, Z. Liu, J. Yang, S. Choi, J. Demarest, L. Yu, A. Carr, W. Wang, J. Strane, S. Tsai, Y. Liang, H. Amanapu, I. Saraf , K. Ryan, F. Lie, W. Kleemeier, K. Choi, N. Cave, T. Yamashita, A. Knorr, D. Gupta, B. Haran, D. Guo, H. Bu, and M. Khare, IBM Semiconductor Technology Research*

This work thoroughly investigates the external parasitic resistance in advanced FinFET technology. The optimization of the parasitic resistance is systematically examined in terms of 1) source/drain epi resistance, 2) contact resistance and 3) middle of line metal stud resistance. Various resistance reduction knobs have been experimentally explored in these three aspects and low contact resistivity of 1×10^{-9} and 7×10^{-10} Ωcm2 have been demonstrated on transistor level for NFET and PFET. By combining all the parasitic resistance reduction strategies, more than 70% and 60% reductions in external parasitic resistance have been realized on NFET and PFET, respectively.

3:15 PM - 3:40 PM

35.5 Sub-10-9 Ω-cm2 Specific Contact Resistivity on P-type Ge and GeSn: *In-situ* Ga Doping with Ga Ion Implantation at 300 ºC, 25 ºC, and -100 ºC, *Y. Wu, L.-H. Chua*, W. Wang, K. Han, W. Zou*, T. Henry*, and X. Gong, National University of Singapore (NUS), *Applied Materials-Varian Semiconductor Equipment*

For the first time, Ga ion implantation (Ga I/I) on in-situ Ga-doped Ge (Ge:Ga) and GeSn (GeSn:Ga) films at various temperatures (300 ºC, 25 ºC, and -100 ºC) was investigated. It is found that cryogenic (-100 ºC) and room temperature (RT, 25 ºC) Ga I/I retains strain and the high quality of the GeSn layer after Ga activation while hot Ga I/I (300 ºC) degrades the crystalline quality due to the implantation-induced defects. An ultra-low specific contact resistivity ρ_c of 8×10^{-10} Ω-cm^2 is achieved for Ti/p+-GeSn contact by in-situ Ga doping followed by cryogenic or RT Ga I/I while ρ_c increases to 2.3×10^{-9} Ω-cm^2 using hot Ga I/I. An ultra-low ρ_c of 9×10^{-10} Ω-cm^2 is also demonstrated for in-situ Ga-doped Ge followed by RT Ga I/I. This is the first realization of sub-10^{-9} Ω-cm^2 ρ_c on non-laser-annealed p-type Ge. The sub-10^{-9} Ω-cm^2 ρ_c is thermally stable up to an annealing temperature of 500 ºC.

3:40 PM - 4:05 PM

35.6 Selective Fin Trimming after Dummy Gate Removal as the Local Fin Width Scaling Approach for N5 and Beyond, *T. Miyashita, S. Sun, S.Mittal, M. S. Kim, A. Pal, A. Sachid, K. Pathak, M. Cogorno, and N. S. Kim, Applied Materials Inc.*

Selective fin trimming after dummy gate removal is proposed as the local fin width scaling approach for further FinFET extension. TCAD simulation shows that the local fin trimming can improve electrostatics, while also providing the benefits of lower S/D resistance and PMOS high channel stress. Although, fin height reduction and parasitic capacitance increases are penalty, overall gate delay is improved due to strong Ion-Ioff boost. SelectraTM etch fin trimming is also presented demonstrating good fin width controllability and smaller variations without any critical fin damages.