Session 33: Modeling and Simulation - Device, Process and Reliability Modeling
Wednesday, December 5, 9:00 AM
Plaza A
Co-Chairs: S. Cea, Intel
W. Vandenberghe, University of Texas, Dallas

9:05 AM - 9:30 AM
33.1 Transport models based on NEGF and empirical pseudopotentials: a computationally viable method for self-consistent simulation of nanoscale devices., *M. G. Pala, O. Badami* and D. Esseni*, Univ. Paris-Sud, Universit´e Paris-Saclay, *University of Udine*

We present new theoretical developments and applications concerning Non-Equilibrium Green's Functions (NEGF) based transport modelling with an Empirical Pseudopotential (EP) Hamiltonian. We have extended the methodology to include arbitrary crystal orientations and strain conditions, and have reformulated quantum confinement and spatial discretization to improve the computational efficiency.

9:30 AM - 9:55 AM
33.2 First Principles Simulation of Energy efficient Switching by Source Density of States Engineering (Invited), *F. Liu, C. Qiu, Z. Zhang, L.-M. Peng, J. Wang*, Z. Wu**, and H. Guo, Peking University, *The University of Hong Kong, ** Institute of Microelectronics, Chinese Academy of Sciences*

Achieving sub-60 mV/decade FET switching is critical for reducing power dissipation in integrated circuits. Here we propose and theoretically investigate steep slope switching made possible by a “cold source” that suppresses “hot” electrons at the thermal tail of the Fermi distribution. We show sub-60 mV/decade switching with: (i) using gapless/gapped graphene as injection source, (ii) introducing a band gap in the source of Si FET. The feasibility and design of the cold source are investigated by first principles on different metals, pocket doping and disorder.

9:55 AM - 10:20 AM
33.3 Universal Swing Factor Approach For Performance Analysis Of Logic Nodes, *M. A. Pourghaderi, A.-T. Pham*, S. Kim, H. Chung, Z. Jiang*, H. Ilatikhameneh*, H.-H. Park*, S. Jin*, J. Kim, W.-Y. Chung, U. Kwon, W. Choi*, D. S. Kim and S. Maeda, Samsung Electronics, *Samsung Semiconductor Inc.*

Deterministic Boltzmann-transport solver has been integrated in performance analysis of logic cells. Employing universal-swing-factor (USF) approach, our setup accurately entails quasi-ballistic transport effects. The injection current and carrier mean free path (MFP) have been extracted for various channel dimensions and interface qualities. The resulting database is used to study candidate architecture for logic nodes. In particular, performance of ring oscillator (RO) with tapered FinFET is presented. For a given junction profile and contact-poly-pitch (CPP), the optimum gate-length (Lg), spacer thickness and contact-CD (CCD) are evaluated. The feasible gain by lowering the spacer k-value and contact resistance is also reported.

10:20 AM - 10:45 AM
33.4 Multi-domain process modeling for advanced logic and memory devices: from equimpments to materials (Invited), *I. Jang, H. Ko, A. Schmidt, S.-J. Kim, M. Cha, H. Ahn, H. Park, D. S. Kim, and H.-K. Kang, Samsung Electronics Co. Ltd.*

For modern semiconductor devices, the level of details which we should investigate for predictive simulation is going extreme. Not only the atomistic simulation is required but equipment and transistor scale simulation is also needed to understand the formation of atomic scale feature. In this paper, practical

applications of multi-domain simulations are introduced for advanced S/D process in logic, interface engineering in DRAM cell and cell stack ALD process of flash memory devices.

10:45 AM - 11:10 AM

33.5 Entire Bias Space Statistical Reliability Simulation By 3D-KMC Method and Its Application to the Reliability Assessment of Nanosheet FETs based Circuits, *W. Chen, Y. Li, L. Cai, P. Chang, G. Du and X. Liu, Peking University*

The trap behaviors based 3D-Kinetic Monte Carlo (KMC) simulator is developed for statistical reliability assessment over the entire bias space. The main features include (i) physical insight into trap charging/discharging, coupling and generation/recombination behaviors for tracking trap-induced degradation of MOSFETs with multilayer gate dielectrics in the entire bias space. (ii) simulation of statistical reliability for the MOSFETs biased under arbitrary mixed stress conditions. (iii) assessment of reliability degradation in circuit operations with various Vg/Vd stress patterns and self-heating. The statistical reliability in nanosheet (NS) FETs and corresponding circuits are investigated. The impacts of the initial interface state and bulk trap density on the threshold voltage shift during the stress and relaxation phases are also analyzed.

11:10 AM - 11:35 AM

33.6 A Physics-based Thermal Model of Nanosheet MOSFETs for Device-Circuit Co-design, *L. Cai, W. Chen, P. Chang, G. Du, X. Zhang, J. Kang and X. Liu, Peking University*

A physics-based thermal model is developed to describe the self-heating effects (SHE) on nanosheet MOSFETs. Three stages of transient temperature response due to the anisotropic heat dissipation and asymmetrical temperature distribution are well understood by the thermal RC network model, providing the physical insight into frequency-dependent SHE in AC operation. The proposed model is further implemented into SPICE simulator for high-efficient thermal assessment in circuit level by the flexible BEOL. Layout design in inverter cell correlated with thermal behavior is investigated for static and transient operation downwards 3nm CMOS node. The SHE and thermal-aware reliability in inverter-based ring oscillator are predicted. The thermal model can be used as a device-circuit co-design tool to assess the thermal behavior accurately and efficiently.