Session 28: Circuit and Device Interaction - Advanced CMOS Technology for Computing in the Nanoscale Era
Wednesday, December 5, 9:00 AM
Grand Ballroom B
Co-Chairs: S. Rakheja, New York University
W. Hafez, Intel Corporation

9:05 AM - 9:30 AM
28.1 System Performance: From Enterprise to AI (Invited), *A. Kumar, L. Chang, G.E. Tellez, L.A. Clevenger, and J.L. Burns, IBM Research*

System performance has shown many decades of continuous improvement. After first reviewing historical trends and the current outlook, in this paper we discuss the challenges and opportunities in future computing systems due to the disruptive confluence of stalled scaling and emerging AI workloads. Heterogeneous integration is highlighted as a key means to future systems performance growth.

9:30 AM - 9:55 AM
28.2 Design-Technology Co-Optimization of Standard Cell Libraries on Intel 10nm Process, *X. Wang, R. Kumar, S. Bangalore Prakash, P. Zheng, T.-H. Wu, Q. Shi, M. Nabors, S. C. Gadigatla, S. Realov, C.-H. Chen, Y. Zhang, K. Mistry, A. Yeoh, I. Post, C. Auth, A. Madhavan, Intel Corporation*

This paper highlights the co-optimization of process technology, std. cell library offerings and block-level TFM on Intel 10nm node to enable unprecedented scaling opportunity for products ranging from high performance client/server to low power mobile/IoT segments. The 10nm short height library enables 2.7x transistor density scaling going from 14nm counterpart. The taller height libraries are optimized to meet performance and reliability requirements of Intel's leading edge client/server products. PPA trade-offs are analyzed both at std. cell level and block level on an industry standard Core IP design.

9:55 AM - 10:20 AM
28.3 An Accurate FinFET's Vmin Estimation Method for Extreme Low Operation Voltage Design, *H. W. Choi, S. K. Kim, H. Jung, D. R. Chang, S. Park and Y. Yasuda-Masuoka, and J.S. Yoon Foundry Business, Samsung Electronics Co. Ltd.*

In this paper, the minimum operating voltage (Vmin) estimation methodology for advanced FinFET technology is newly proposed with a manufacturability consideration. The experiment depicts that key factors to determine Vmin are the sum of threshold voltages of n-FET/p-FET, beta-ratio (n/p-FET strength ratio), and random variation. The new equation successfully captures the key electrical features, which is verified by both Monte-Carlo simulation and advanced 11nm/8nm FinFET experimental data. Based on the new model, the paper also provides the guideline for threshold voltage and local mismatch strategy for future advanced FinFET Vmin improvement.

10:20 AM - 10:45 AM
28.4 Tackling Fundamental Challenges of Carrier Transport and Device Variability in Advanced Si *n*FinFETs for 7nm Node and Beyond, *M.-H. Lin, V. S. Chang, J.-H. Lu, S.-H. Wang, and S.-H. Yang, Taiwan Semiconductor Manufacturing Company*

We report that the S/D long-range Coulomb interactions and gate-corner work-function roll-up can be mitigated by S/D epitaxy and HK/MG RPG optimizations, paving the way for 7nm node and beyond. These techniques feature larger Idsat enhancements than that of Idlin. Their signatures and influences on transport parameters are investigated comprehensively.

10:45 AM - 11:10 AM

28.5 Extendable and Manufacturable Volume-less Multi-Vt Solution for 7nm Technology Node and Beyond, *R. Bao, H. Zhou, M. Wang, D. Guo, B. S Haran, V. Narayanan, R. Divakaruni, IBM Semiconductor Technology Research*

We demonstrated more than 3 pairs of threshold voltage (Vt) devices by volume-less multiple Vt (multi-Vt) scheme plus dual work function metals (WFM) without performance and reliability degradation on 20nm gate length FinFET CMOS devices. Vt shifts over 200 mV were achieved for both nFET and pFET. The volume-less nature of this multi-Vt scheme relieves replacement metal gate (RMG) challenges and opens the path to offer multi-Vt solution for future highly scaled technologies.

11:10 AM - 11:35 AM

28.6 Channel Geometry Impact and Narrow Sheet Effect of Stacked Nanosheet, *C. W. Yeung, J. Zhang, R. Chao, O. Kwon*, R. Vega, G. Tsutsui, X. Miao, C. Zhang, C.-W. Sohn*, B. K. Moon**, A. Razavieh**, J. Frougier**, A. Greene, R. Galatage**, J. Li, M. Wang, N. Loubet, R. Robison, V. Basker, T. Yamashita, D. Guo, IBM, *Samsung Electronics, **GLOBALFOUNDRIES*

The characteristics of Stacked Nanosheet are investigated, focusing on channel geometry. For the first time, “narrow sheet effect” on carrier transport is observed. By comparing measured electron and hole mobilities, and the n-type/p-type opposite transconductance (gm) trends versus sheet width (Wsheet), we show that the mobility dependency on Wsheet, is attributed to reduced (100) plane conduction contribution as Wsheet shrinks.

11:35 AM - 12:00 PM

28.7 3nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications (Late News), *G. Bae, D.-I. Bae, M. Kang, S.M. Hwang, S.S. Kim, B. Seo, T.Y. Kwon, T.J. Lee, C. Moon, Y.M. Choi, K. Oikawa, S. Masuoka, K.Y. Chun, S.H. Park, H.J. Shin, J.C. Kim, K.K. Bhuwalka, D.H. Kim, W.J. Kim, J. Yoo, H.Y. Jeon, M.S. Yang, S.-J. Chung, D. Kim, B.H. Ham, K.J. Park, W.D. Kim, S.H. Park, G. Song, Y.H. Kim, M.S. Kang, K.H. Hwang, C.-H. Park, J.-H. Lee, D.-W. Kim, S-M. Jung, H.K. Kang, Samsung Electronics*

As the most feasible solution beyond FinFET is successfully technology, a gate-all-around Multi-Bridge-Channel MOSFET (MBCFET) technology demonstrated including a fully working high density SRAM. MBCFETs are fabricated using 90% or more of FinFET processes with only a few revised masks, allowing easy migration from FinFET process. Not only on-target but also multiple Vt is achieved in challengingly limited vertical spacing between channels. Also, reliability of MBCFETs is shown to be comparable to that of FinFETs. Three representative superior characteristics of MBCFET compared to FinFET have been demonstrated — better gate control with 65 mV/dec sub-threshold swing (SS) at short gate length, higher DC performance with a larger effective channel width (Weff) at reference footprint, and design flexibility with variable nanosheet (NS) widths. The optimization of the standard cell design by using variable NS width is evaluated. The usefulness of MBCFET as a multi-purpose performance provider is proven by the modulation of effective capacitance (Ceff), effective resistance (Reff) and frequency by Weff control. Finally, mass production feasibility with MBCFET is proven through a fully working high density SRAM circuit.