Session 25: Characterization, Reliability, and Yield - Emerging Memory Reliability
Tuesday, December 4, 2:15 PM
Plaza B
Co-Chairs: D. Varghese, Texas Instruments
H. Park, SK Hynix

2:20 PM - 2:45 PM
25.1 Deconvoluting charge trapping and nucleation interplay in FeFETs: Kinetics and Reliability, *M. Pesic, A. Padovani, S. Slesazeck, T. Mikolajick*, and L. Larcher**, MDLSoft Inc, *TU Dresden, **University of Modena and Reggio Emilia*

Discovery of ferroelectric (FE) behavior in HfO2 removed the compatibility roadblocks between the state-of-the-art CMOS and FE memories. Even though FE FETs (FeFETs) are scaled into 22 nm nodes and beyond, the limits of the technology as well as the physical mechanisms and reliability are still under research. In this paper we successfully developed a multiscale modeling platform to understand the interplay between the FE switching and charge trapping. Starting from the nucleation theory and rigorous charge transport modeling we present for the first time a self-consistent modeling framework we used for investigation of reliability and variability in FeFETs.

2:45 PM - 3:10 PM
25.2 Impact of self-heating on reliability predictions in STT-MRAM, *S. Van Beek*, B. J. O'Sullivan, P. J. Roussel, R. Degraeve, E. Bury, J. Swerts, S. Couet, L. Souriau, S. Kundu, S. Rao, W. Kim, F. Yasin, D. Crotti, D. Linten and G. Kar, imec, *also at KU Leuven*

At breakdown conditions, large current flows in STT-MRAM devices. We experimentally show that this large current causes significant self-heating of 200-300°C, which impacts the reliability extrapolation to operating conditions. By measuring and analyzing breakdown at various temperatures and on different MgO thickness, we successfully incorporate self-heating into the breakdown model. We find that the 10 year lifetime is underestimated by a factor 10^3 at 63-percentile, to even 10^7 when applying percentile scaling to 1 ppm.

3:10 PM - 3:35 PM
25.3 Investigating the Statistical-Physical Nature of MgO Dielectric Breakdown in STT-MRAM at Different Operating Conditions, *J.H. Lim, N. Raghavan, A. Padovani**, J.H. Kwon*, K. Yamane*, H. Yang*, V.B. Naik*, L. Larcher***, K.H. Lee* and K.L. Pey, Singapore University of Technology and Design (SUTD), *GLOBALFOUNDRIES Singapore Pte. Ltd., **MDLSoft Inc., ***Università di Modena e Reggio Emilia*

We carry out a comprehensive study on dielectric breakdown in ultra-thin MgO for STT-MRAM application. Pulse voltage, polarity dependence and temperature have been used to study the breakdown distribution in MgO, which follows defect clustering model. Field-induced mechanical strain at the MgO interface during pulsed stress affects TDDB lifetime significantly.

3:35 PM - 4:00 PM
25.4 Trap Reduction and Performances Improvements Study after High Pressure Anneal Process on Single Crystal Channel 3D NAND Devices, *A. Subirats, A. Arreghini, R. Delhougne, E. Rosseel, A. Hikavyy, L. Breuil, S. Vadakupudhu Palayam, G. Van den bosch, D. Linten and A. Furnémont, imec*

We study the impact of HPAP on SCC 3D NAND devices. We show that the process can reduce trap density but is leaving trap impact on devices VT unaffected. It is also shown, both by simulations and measurements, that further scaling could lead to the increase of single trap impact. Finally, we measure that

despite largely improving devices electrical parameter, HPAP has no effect on memory performances (Program/Erase) or could slightly degrade it (Retention).