Session 22: Nano Device Technology - 2D CMOS and Memory Devices
Tuesday, December 4, 2:15 PM
Continental Ballroom 6
Co-Chairs: M. Shrivastava, Indian Institute of Science
W.-C. Chien, Macronix

2:20 PM - 2:45 PM
22.1 2D materials: roadmap to CMOS integration (Invited), *C. Huyghebaert, T.Schram, Q. Smets, T. Kumar Agarwal, D.Verreck, S.Brems, A.Phommahaxay, D.Chiappe*, S. El Kazzi, C.Lockhart de la Rosa, G. Arutchelvan ,D. Cott, J. Ludwig, A. Gaur, S. Sutar, A. Leonhardt, D. Marinov, D. Lin, M. Caymax, I. Asselberghs, G. Pourtois and I.P. Radu, imec, *currently @ ASM Europe*

To keep Moore's law alive, 2D materials are considered as a replacement for Si in advanced nodes due to their atomic thickness, which offers superior performance at nm dimensions. In addition, 2D materials are natural candidates for monolithic integration which opens the door for density scaling along the 3rd dimension at reasonable cost. This paper highlights the obstacles and paths to a scaled 2D CMOS solution. The baseline requirements to challenge the advanced Si nodes are defined both with a physical compact model and TCAD analysis, which allows us to identify the most promising 2D material and device design. For different key challenges, possible integrated solutions are benchmarked and discussed. Finally we report on the learning from our first lab to fab vehicle designed to bridge the lab and IMEC's 300mm pilot line.

2:45 PM - 3:10 PM
22.2 First Demonstration of WSe_2 Based CMOS-SRAM, *C.-S. Pang, N. Thakuria1, S. K. Gupta, and Z. Chen, Purdue University*

In this work, we demonstrate a CMOS static random-access-memory (SRAM) using WSe2 as a channel material for the first time, providing comprehensive DC analyses for transition metal dichalcogenide (TMD) material-based memory applications. A tri-gate design is adopted for the n-type MOSFET, while an air-stable, oxygen plasma induced doping scheme is introduced to implement the p-type MOSFET. DC measurements of SRAM cells demonstrate a unique dynamic tunability enabled by modulating the n-FET doping level through electrostatically gating the extended source/drain regions. Furthermore, with various read/write assist techniques, SRAM operation at low VDD of 0.8V is achieved. Our low power demonstration and its 2D ultra-thin material nature suggest promising applications of WSe2 for flexible electronics and Internet of Things (IoT).

3:10 PM - 3:35 PM
22.3 Steep Slope p-type 2D WSe_2 Field-Effect Transistors with Van Der Waals Contact and Negative Capacitance, *J. Wang, X. Guo, Z. Yu*, Z. Ma**, Y. Liu, M. Chan**, Y. Zhu, X. Wang* and Y. Chai, Hong Kong Polytechnic University, *Nanjing University, **The Hong Kong University of Science and Technology*

We fabricated Steep-slope p-type 2d WSe2 NCFET using van der Waals Pt contact and HZO/Al2O3 dielectric. The van der Waals contact is free from disorder and Fermi level pinning and decreases the sub-threshold slope. The NCFET shows minimum SS of 18.2 mV/dec and negligible hysteresis in the sub-threshold region.

3:35 PM Coffee Break

4:00 PM - 4:25 PM

22.4 Toward High-mobility and Low-power 2D MoS_2 Field-effect Transistors (Invited), *Z. Yu, Y. Zhu, W. Li, Y. Shi, G. Zhang*, Y. Chai and X. Wang, Nanjing University, *The Hong Kong Polytechnic University*

2D semiconductors are promising candidates for future electronic device applications due to their immunity to short-channel effects (SCE), but many issues regarding mobility, contact, interface and power consumption still remain (Fig. 1). We develop a low-field model to calculate the mobility of monolayer MoS2 FETs. Guided by the model, high carrier mobility of 150 cm2/Vs and saturation current over 450 μm are realized in long-channel monolayer MoS2 FETs, through a series of interface optimization by high-$\boldsymbol{k}$ dielectric and thiol chemical treatment. For low-power applications, we demonstrate hysteresis-free MoS2 negative capacitance FETs (NCFETs) using ferroelectric HfZrOx(HZO) as gate dielectric, achieving sub-60mV/dec subthreshold slope (SS) over 6 orders of ID, minimum SS of 24 mV/dec and 10^7 on/off ratio under Vdd=0.5V. We further study the high frequency performance and show that sub-60mV/dec is maintained at least to 10 kHz without signs of degradation. Finally, by performing different gate sweeps we conclude that the steep slope is indeed due to NC effects rather than ferroelectric switching of HZO.

4:25 PM - 4:50 PM
22.5 3D Monolithic Stacked 1T1R cells using Monolayer MoS_2 FET and hBN RRAM Fabricated at Low (150°C) Temperature, *C.-H. Wang, C. McClellan, Y. Shi*, Xin Zheng, V. Chen, M. Lanza*, E. Pop and H. -S. P. Wong, Stanford University, * Soochow University*

We demonstrate 3D monolithic integrated two-level stacked 1-transistor/1-resistor (1T1R) memory cells with processing temperature < 150 ºC. CVD monolayer MoS2 transistors are employed to switch few layer CVD hBN RRAMs with programming voltage < 1 V. The 1T1R cell resistance change linearity can be improved by controlling the gate voltage.

4:50 PM - 5:15 PM
22.6 Atomristors: Memory Effect in Atomically-thin Sheets and Record RF Switches, *R. Ge, X. Wu, M. Kim, P.-A. Chen, J. Shi**, J. Choi, X. Li, Y. Zhang**, M.-H. Chiang*, J. C. Lee and D. Akinwande, University of Texas at Austin, *National Cheng Kung University, **Peking University*

Non-volatile resistive switching (NVRS) has been recently observed with synthesized monolayer molybdenum disulfide (MoS2) as the active layer and termed atomristors [1]. In this paper, we demonstrate the fastest switching speed (<15 ns) among all crystalline two-dimensional (2D) related NVRS devices to the best of our knowledge. For the first time, ab-initio simulation results of atomristors elucidate the mechanism revealing favorable substitution of specific metal ions into sulfur vacancies during switching. This insight combined with area-scaling experimental studies indicate a local conductive-bridge-like nature. The proposed mechanism is further supported by sulfur annealing recovery phenomenon. Moreover, exfoliated MoS2 monolayer is demonstrated to have memory effect for the first time, expanding the materials beyond synthesized films. State-of-the-art non-volatile RF switches based on MoS2 atomristors were prepared, featuring 0.25 dB insertion loss, 29 dB isolation (both at 67 GHz), and 70 THz cutoff frequency, a record performance compared to emerging RF switches. Our pioneering work suggests that memory effect maybe present in dozens or 100s of 2D monolayers similar to MoS2 paving the path for new scientific studies for understanding the rich physics, and engineering research towards diverse device applications.

5:15 PM - 5:40 PM
22.7 An Ultra-fast Multi-level $MoTe_2$-based RRAM, *F. Zhang, H. Zhang*, P.R. Shrestha*, Y. Zhu, K. Maize, S. Krylyuk*, A. Shakouri, J.P. Campbell**, K.P. Cheung**, L.A. Bendersky**, A.V. Davydov** and J. Appenzeller, Purdue University, *Theiss Research, Inc., **National Institute of Standards and Technology*

We report multi-level MoTe2-based resistive random-access memory (RRAM) devices with switching speeds of less than 5 ns due to an electric-field induced 2H to 2Hd phase transition. Different from conventional RRAM devices based on ionic migration, the MoTe2-based RRAMs offer intrinsically better reliability and control. In comparison to phase change memory (PCM)-based devices that operate based on a change between an amorphous and a crystalline structure, our MoTe2-based RRAM devices allow faster switching due to a transition between two crystalline states. Moreover, utilization of atomically thin 2D materials allows for aggressive scaling and high-performance flexible electronics applications. Multi-level stable states and synaptic devices were realized in this work, and operation of the devices in their low-resistive, high-resistive and intrinsic states was quantitatively described by a novel model.