Session 21: Process and Manufacturing Technology - Advanced Gate All Around Process
Tuesday, December 4, 2:15 PM
Continental Ballroom 5
Co-Chairs: S. Yang, Qualcomm
C.-W. Liu, Taiwan University

2:20 PM - 2:45 PM
21.1 Ge CMOS gate stack and contact development for Vertically Stacked Lateral Nanowire FETs, *M.J.H. van Dal, G. Vellianitis, G. Doornbos, B. Duriez, M.C. Holland, T. Vasen, A. Afzalian, E. Chen*, S.K. Su*, T.K. Chen*, T.M. Shen*, Z.Q. Wu*, C.H. Diaz*, TSMC Corporate Research, *TSMC*

We present (i) a novel, thermally stable Atomic Layer Deposition (ALD) high-k dielectric stack that, for the first time, has the potential to meet all gate stack requirements for both n- and p-channel Ge FETs, (ii) record low contact resistivity for n Ge/metal contacts using an implant-free contact scheme with successful implementation into a single nanowire (NW) Ge nFET baseline, (iii) single NW Ge pFETs with short-channel effect (SCE) immunity down to 24 nm physical gate length, of which electrical data show excellent agreement with calibrated models and (iv) demonstration of Ge-channel vertically stacked lateral NW FETs using a 300 mm VLSI compatible platform.

2:45 PM - 3:10 PM
21.2 Advantage of NW structure in preservation of SRB-induced strain and investigation of off-state leakage in strained stacked Ge NW pFET, *H. Arimura, G. Eneman, E. Capogreco, L. Witters, A. De Keersgieter, P. Favia, C. Porret, A. Hikavyy, R. Loo, H. Bender, L.-Å. Ragnarsson, J. Mitard, N. Collaert, D. Mocuta, N. Horiguchi, imec*

Nanowires (NW) and nanosheets (NS) are promising device architectures for future technology nodes as they can offer better electrostatics than FinFETs. In this paper, we show another advantage of strained Ge NW pFET over strained Ge FinFET, which lies in the preservation of Strain-Relaxed-Buffer (SRB)-induced strain through fin cut and S/D recess. This benefit comes from the presence of the sacrificial SiGe layers. Lowering the Ge concentration in the SiGe sacrificial layer is a way to further suppress the strain loss. Furthermore, a comparison of Ge NW pFETs integrated on Ge SRB and SiGe SRB reveals that SiGe SRB provides a huge advantage not only in the strain engineering but also in IOFF control. These are key enablers in maximizing the performance while minimizing the IOFF of strained Ge NW pFETs.

3:10 PM - 3:35 PM
21.3 Tunability of Parasitic Channel in Gate-All-Around Stacked Nanosheets, *S. Barraud, B. Previtali, V. Lapras, C. Vizioz, J.-M. Hartmann, S. Martinie, J. Lacord, M. Cassé, L. Dourthe, V. Loup, G. Romano*, N. Rambal, Z. Chalupa, N. Bernier, G. Audoit, A. Jannaud**, V. Delaye, V. Balan, O. Rozeau, T. Ernst, M. Vinet, CEA-LETI, and Univ. Grenoble Alpes, * STMicroelectronics, **SERMA Technologies*

For the first time, a comprehensive study going from the integration of 3D stacked nanosheets Gate-All-Around (GAA) MOSFET devices to SPICE modeling is proposed. Devices have been successfully fabricated on SOI substrates using a replacement high- metal gate process and self-aligned-contacts. Back-biasing is herein efficiently used to highlight a drastic improvement of electrostatics in the upper GAA Si channels. Advanced electrical characterization of these devices enabled us to calibrate a new version of physical compact model (LETI-NSP) in order to assess the performance of ring oscillators for different configurations of GAA FETs integrating up to 8 vertically stacked Si channels.

3:35 PM Coffee Break

4:00 PM - 4:25 PM

21.4 Voltage Transfer Characteristic Matching by Different Nanosheet Layer Numbers of Vertically Stacked Junctionless CMOS Inverter for SoP/3D-ICs applications, *P.-J. Sung, C.-Y. Chang*, L.-Y. Chen**, K.-H. Kao**, C.-J. Su, T.-H. Liao***, C.-C. Fang***, C.-J. Wang, T.-C. Hong*, C.-Y. Jao***, H.-S. Hsu***, S.-X. Luo**, Y.-S. Wang**, H.-F. Huang**, J.-H. Li**, Y.-C. Huang*, F.-K. Hsueh, C.-T. Wu, Y.-M. Huang, F.-J. Hou, G.-L. Luo, Y.-C. Huang, Y.-L. Shen, W. C.-Y. Ma***, K.-P. Huang+, K.-L. Lin, S. Samukawa++, Y. Li*, G.-W Huang, Y.-J. Lee,*, J. -Y. Li, W.-F. Wu, J.-M. Shieh, T.-S. Chao*, W. -K. Yeh, Y.-H. Wang***, National Nano Device Laboratories, **National Chiao Tung University, **National Cheng Kung University, ***National Sun Yat-sen University, +Industrial Technology Research Institute, ++Tohoku University*

For the first time, CMOS inverters with different numbers of vertically stacked junctionless (JL) nanosheets (NSs) are demonstrated. All fabrication steps were below 600 °C, and 8-nm thick poly-Si NSs with smooth surface roughness were formed by a dry etching process. Compared to single channel devices, stacked n/p-channel FETs exhibit higher on-current with low leakage current. Furthermore, a common-gate process was performed for the fabrication of CMOS inverters. By adjusting the NS layer numbers for n/pFETs, respectively, the voltage transfer characteristics (VTCs) of the CMOS inverter can be matched much better to reduce the noise margin due to on-current matching without area penalty. This work experimentally demonstrates a new configuration of CMOS inverters on stacked NSs, which is promising for System-on-Panel (SoP) and 3D-ICs applications.

4:25 PM - 4:50 PM

21.5 Vertically Stacked Gate-All-Around Si Nanowire CMOS Transistors with Reduced Vertical Nanowires Separation, New Work Function Metal Gate Solutions, and DC/AC Performance Optimization, *R. Ritzenthaler, H. Mertens, V. Pena*, G. Santoro*, A. Chasin, K. Kenis, K. Devriendt, G. Mannaert, H. Dekkers, A. Dangol, Y. Lin*, S. Sun*, Z.Chen**, M. Kim*, J. Machillot*, J. Mitard, N. Yoshida*, N. Kim*, D. Mocuta, N. Horiguchi, imec, *Applied Materials*

We report on vertically stacked gate-all-around (GAA) Si nanowire (NW) MOSFETs, integrated in a CMOS dual Work Function Metal Replacement Metal Gate (RMG) flow. The integration of a lower temperature STI module and a SiN liner, designed to mitigate the oxidation-induced NW size loss and improve the width/height aspect ratio and NW controllability, is validated electrically. Additionally, Si GAA devices with reduced vertical nanowire spacing are demonstrated. The challenges in terms of Work Function Metal thickness scaling are highlighted, and a thinner nMetal process with low VTH capability and no JG/PBTI lifetime penalty is proposed. Electrically, these process innovations lead to a large improvement of ION/IOFF performance and short channel margin. Finally, a ring oscillator circuit demonstration is shown, with a improvement of gate delay from 24ps down to 10ps at matched VDD demonstrated.