Session 6 (Focus): Nano Device Technology - Quantum Computing Devices
Monday, December 3, 1:30 PM
Continental Ballroom 5
Co- Chairs: I. Radu, imec
W. Taylor, GLOBALFOUNDRIES

1:35 PM - 2:00 PM
6.1 Device challenges for near term superconducting quantum processors: frequency collisions (Invited), *M. Brink, J. M. Chow, J. Hertzberg, E. Magesan, S. Rosenblatt, IBM T.J. Watson Research Center*

The outstanding progress in experimental quantum computing with superconducting Josephson-junction based qubits over the past few decades has pushed coherence times many orders of magnitude above that of the first measured. We are also in the midst of scaling towards complex architectures of multi-qubit processors where maintaining very low gate error rates at the limits supported by coherence times is extremely important. Here we will review some of the critical materials and device challenges for superconducting qubits from the perspective of improved coherence and improved error rates. In particular we will focus on the problem of frequency allocations in order to target multi-qubit lattices for fixed-frequency microwave-based gates.

2:00 PM - 2:25 PM
6.2 Scalable quantum computing with ion-implanted dopant atoms in silicon (Invited), *A. Morello, G. Tosi, F.A. Mohiyaddin, V. Schmitt, V. Mourik, T. Botzem, A. Laucht, J.J. Pla, S. Tenberg, R. Savytskyy, M. Madzik, F. Hudson, A.S. Dzurak, K.M. Itoh*, A.M. Jakob**, B.C. Johnson**, J.C. McCallum** and D.N. Jamieson**, UNSW Sydney, *Keio University, ** University of Melbourne,*

We present a scalable strategy to manufacture quantum computer devices, by encoding quantum information in the combined electron-nuclear spin state of individual ion-implanted phosphorus dopant atoms in silicon. Our strategy allows a typical pitch between quantum bits of order 200 nm, and retains compatibility with the standard fabrication processes adopted in classical CMOS nanoelectronic devices. We theoretically predict fast and high-fidelity quantum logic operations, and present preliminary experimental progress towards the realization of a “flip-flop” qubit system.

2:25 PM - 2:50 PM
6.3 Qubit Device Integration Using Advanced Semiconductor Manufacturing Process Technology (Invited), *R. Pillarisetty, N. Thomas, H.C. George, K. Singh, J. Roberts, L. Lampert, P. Amin, T.F. Watson, G. Zheng, J. Torres, M. Metz, R. Kotlyar, P. Keys, J.M. Boter*, J.P. Dehollain*, G. Droulers*, G. Eenink*, R. Li*, L. Massa*, D. Sabbagh*, N. Samkharadze*, C. Volk*, B. P. Wuetz*, A.-M. Zwerver*, M. Veldhorst*, G. Scappucci*, L.M.K. Vandersypen*, J.S. Clarke Intel Corporation, *TU Delft*

Quantum computing’s value proposition of an exponential speedup in computing power for certain applications has propelled a vast array of research across the globe. While several different physical implementations of device level qubits are being investigated, semiconductor spin qubits have many similarities to scaled transistors. In this article, we discuss the device/integration of full 300mm based spin qubit devices. This includes the development of (i) a 28Si epitaxial module ecosystem for growing isotopically pure substrates with among the best Hall mobility at these oxide thicknesses, (ii) a custom 300mm qubit testchip and integration/device line, and (iii) a novel dual nested gate integration process for creating quantum dots

2:50 PM Coffee Break

3:15 PM - 3:40 PM

6.4 Silicon Isotope Technology for Quantum Computing (Invited), *S. Miyamoto, K. Itoh, Keio University*

We present isotopically engineered Si-28/SiGe heterostructures for development of silicon-based quantum computers using a standard silicon CMOS integration technology. Our Si-28 quantum-wells are well-strained and demonstrate high electron mobility and large valley-splitting. These properties provide promising platforms for realization of highly integrated spin qubits working together with silicon CMOS circuits.

3:40 PM - 4:05 PM

6.5 Towards scalable silicon quantum computing (Invited), *M. Vinet, L. Hutin, B. Bertrand, S. Barraud, J.-M. Hartmann, Y.-J. Kim, V. Mazzocchi, A. Amisse, H. Bohuslavskyi, L. Bourdet*, A. Crippa*, X. Jehl*, R. Maurand*, Y.-M. Niquet*, M. Sanquer*, B. Venitucci*, B. Jado**, E. Chanrion**,P.-A. Mortemousque**, C. Spence**, M. Urdampilleta**, S. De Franceschi* and T. Meunier**, Université Grenoble Alpes, *CEA, LETI, **CNRS*

We report the efforts and challenges dedicated towards building a scalable quantum computer based on Si spin qubits. We review the advantages of relying on devices fabricated in a thin film technology as their properties can be in situ tuned by the back gate voltage, which prefigures tuning capabilities in scalable qubits architectures.

4:05 PM - 4:30 PM

6.6 Majorana QuBits (Invited), *L. Kouwenhoven, Delft University of Technology*

Abstract- We present an overview of Majorana qubits based on one-dimensional semiconducting nanowires partially covered with a conventional superconductor. Majorana zero modes emerge at the wire ends when this hybrid system transitions from a conventional superconducting phase to a topological phase, in general occurring on increasing a magnetic field. For sufficiently long wires different Majoranas are fully independent and Majorana-based qubit states become topologically protected, which make them insensitive to local sources of noise. We present qubit designs, materials and device development and ongoing experimental efforts.