

Session 5 (Focus): Characterization, Reliability, and Yield - Interconnects to Enable Continued Scaling

Monday, December 3, 1:30 PM

Continental Ballroom 4

Co- Chairs: T. Oates, TSMC

T. Nigam, GLOBALFOUNDRIES

1:35 PM - 2:00 PM

5.1 Interconnect Design and Technology Optimization for Conventional and Emerging Nanoscale Devices: A Physical Design Perspective (Invited), D. Prasad, A. Naeemi*, Arm Inc., *Georgia Institute of Technology

Interconnect parasitics severely limit the performance and power dissipation in modern circuits at the advanced process technology nodes. Hence, device-level advances must be complemented with appropriate interconnect technology and design innovations for effective enablement at the circuit and system levels. This paper highlights the impact of device technologies on the optimal interconnect design. The studies for FinFET and Tunnel-FETs are conducted on fully placed-and-routed physical designs. The impact of device and interconnect technology co-optimization on circuit performance, power, and variability is shown for a range of emerging devices.

2:00 PM - 2:25 PM

5.2 Mechanisms of Electromigration Damage in Cu Interconnects (Invited), C.-K. Hu, L. Gignac*, G. Lian, C. Cabral*, K. Motoyama, H. Shobha, J. Demarest, Y. Ostrovski, C. M. Breslin*, M. Ali**, J. Benedict**, P. S. McLaughlin, J. Ni, X. H. Liu, IBM Research at Albany, *IBM T. J. Watson Research Center, **IBM Systems**

Mechanisms of electromigration (EM) damage in Cu interconnects through various CMOS nodes are reviewed. Pure Cu and Cu alloy interconnects that were used down to 14 nm node can no longer satisfy the electrical current used for 10 nm node and beyond in high-performance ICs. Cu interconnects with a metal cap should be used. Cu interface diffusivity with EM activation energy of 1.6 eV was found to be the dominate EM factor in Cu lines with a Co liner and cap. The median lifetime of 7 or 10 nm node Cu with TaN/Co liner and Co cap is predicted to be over ten thousand years at 140oC with $1.5 \times 10^7 \text{A/cm}^2$. However, the resistivity size effect and the difficulty of scaling barrier/liner layer without defects can limit the Cu BEOL roadmap below the 7 nm node.

2:25 PM - 2:50 PM

5.3 Interconnect metals beyond copper: reliability challenges and opportunities (Invited), K. Croes, Ch. Adelman, C.J. Wilson, H. Zahedmanesh, O. Varela Pedreira, C. Wu, A. Lesniewsak, H. Oprins, S. Beyne, I. Ciofi, D. Kocaay, M. Stucchi and Zs. Tokei, imec

Reliability challenges of candidate metal systems to replace traditional Cu wiring in future interconnects are discussed. From a reliability perspective, a key opportunity is electromigration improvement: due to their high melting point and slower self-diffusion kinetics, higher current carrying capabilities are possible. Also, the higher cohesive energy and better resistance to oxidation of some metals potentially allows for barrierless integration, although adhesion properties must be carefully optimized. Besides avoiding small grain pinning and enabling high aspect ratio trench fill, the main processing challenges are identified to be a) avoiding seam voids, b) adhesion, c) CMP and d) disruptive metal etch. Main reliability challenges are related to higher mechanical stresses and higher joule heating which could lead to delamination during further processing and packaging and to enhanced electromigration in nearby metal lines.

2:50 PM - 3:15 PM

5.4 Microstructure Evolution and Effect on Resistivity for Cu Nanointerconnects and Beyond (Invited), S. Hu, P. S. Ho, University of Texas at Austin

In this paper, we investigate the microstructure evolution in Cu, Co and Ru nanointerconnects and the scaling effect on resistivity. The scaling effect on microstructure of Cu interconnects was analyzed to the 24 nm linewidth for the 14 nm node using a high-resolution TEM precession microdiffraction technique. The TEM study was supplemented by a Monte Carlo simulation to investigate grain growth in nanointerconnects based on local energy minimization. The scaling effect on electrical resistivity was analyzed for Cu, Ru and Co nanointerconnects, taking into account the contributions from surface and grain boundary scatterings. The results for Cu and Co are consistent with recent experiments.

3:15 PM *Coffee Break*

3:40 PM - 4:05 PM

5.5 Integrating Graphene into Future Generations of Interconnect Wires (Invited), L Li, H.-S. Philip Wong, Stanford University

The escalating RC delay and diminishing reliability of Cu interconnect present immense challenges for integrated circuits performance improvement. This paper reviews the use of single-layer graphene as the diffusion barrier and capping layer to extend scaling of Cu into future generations of interconnects. With graphene barrier/capping layer, processor core simulations predict an 8% speed boost or 12% energy saving, plus higher tolerance for process variations. Single-layer graphene (3.35 Å thick) provides 3.3× longer barrier lifetime than 2 nm TaN. Barrier reliability is expected to further improve with transfer-free and single-crystalline graphene. In-situ low-temperature grown graphene (<0.7 nm thick) improves Cu electromigration lifetime by 10× than Cu with 2 nm CoWP. For interconnect scaling beyond Cu, we discuss the potential benefits and challenges of employing multilayer graphene as a Cu replacement. Multi-layer graphene shows better resistivity scaling trend with FeCl₃ doping and higher immunity to electromigration. Replacing Cu with multi-layer graphene, processor cores achieve 9% higher speed or 16% less energy consumption. Spin-on-glass encapsulated multi-layer graphene shows two times longer electromigration lifetime than CoWP capped Cu.

4:05 PM - 4:30 PM

5.6 Interconnect Trend for Single Digit Nodes (Invited), M. Naik, Applied Materials Inc.

Transistor performance continues to improve with density scaling and move to FinFET architectures. However, feature size reduction increases parasitic contact and interconnect resistance. This degrades the power-performance equation. To address the resistance bottleneck; new materials, new fill technologies and new integration schemes are in play. This paper reviews metallization trends for contact and interconnect as the industry prepares for 7nm node production and looks towards developing 5 and 3nm nodes.